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A 0.6-V 41.3-GHz Power-Scalable Sub-Sampling PLL in 55-nm CMOS DDC

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SUMMARY A power-scalable sub-sampling phase-locked loop (SS-PLL) is proposed for realizing dual-mode operation; high-performance mode with good phase noise and power-saving mode with moderate phase noise. It is the most efficient way to reduce power consumption by lowering the supply voltage. However, there are several issues with the low-supply millimeter-wave (mmW) SSPLL. This work discusses some techniques, such as a back-gate forward body bias (FBB) technique, in addition to employing a CMOS deeply depleted channel process (DDC).

key words: *sub-sampling PLL, low-supply-voltage, power-scalable, millimeter-wave, CMOS deeply depleted channel (DDC)*

1. Introduction

From 2020, the fifth generation (5G) wireless systems were widely used worldwide. In addition to them, 5G applications employing millimeter-wave (mmW) frequency bands (i.e., Frequency Range 2 (FR2, 24.26–52.5 GHz)) are ready to be used by users. They will make higher-data-rate wireless communications collaborating with beamforming/tracking abilities.

Meanwhile, it is one of the significant challenges to reduce the power consumption of such mmW devices for base stations or users with realizing sufficient phase noise features for high-order modulation data transmission. One of the most efficient ways is to lower the power supply voltages for those devices. Moreover, a power-saving option, such as a power-scalable characteristic of a certain RF system, is needed, especially for user devices. However, it is not so easy for the phase-locked loops (PLLs) because there are many sub-components consisting of them. In addition, there are trade-offs between phase noise and power consumption [1]. There are numerous works to lower the supply voltage of the sub-sampling PLLs (SSPLLs), which show good phase noise characteristics [2]–[4]. However, the design methodology to lower the supply voltage was not cleared for mmW PLLs.

In this work, we employ two methods to realize low-supply voltage power-scalable mmW SSPLL with moderate phase-noise performances; one is to use a CMOS deeply depleted channel (DDC) process, which shows the low threshold voltage and high operation frequency (i.e., f_{max}) [5]–[8]. Moreover, a back-gate forward-body-bias (FBB) technique is applied to reduce the threshold voltage furthermore [2] since there is a performance limitation under low-supply voltage for some components, such as an injection-locked frequency divider (ILFD) and a charge pump (CP).

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2. Proposed Sub-Sampling PLL

Figure 1 shows a proposed SSPLL. In general, the SSPLL requires a frequency-locked loop, such as a conventional charge-pump PLL (CPPLL) [9], [10], which consists of a phase/frequency detector (PFD) with a phase-insensitive dead zone (DZ), a CP, a loop filter (LF), a divider (e.g., total division ratio: N), and a VCO. For mmW SSPLLs, wide-lock-range ILFDs are required [11]. After the frequency locking with the CPPLL operation, a sub-sampling operation starts phase locking using a sub-sampling phase detector (SSPD) with a pulser and a sub-sampling charge pump (SSCP). Due to the sub-sampling operation, the SSPLL can achieve lower in-band phase noise than conventional PLLs, since the generated SSPD/SSCP noise characteristics are not multiplied by N^2 [9].

In Fig. 1, two pairs of SSPD/pulser/SSCP are employed to compensate for amplitude and phase mismatches of high-frequency VCO outputs and leakage canceling via the SSPD transistors [11]. An input buffer amplifies the input signal and generates differential clocks from the single-end input. In addition, a voltage doubler (VD) is applied to double the input amplitude of the clocks for SSPDs. It helps the on-resistance of the sampling transistor of the SSPD lower.

Figure 2 (a) depicts a cross-coupled VCO, which employs transmission lines (characteristic impedance: $Z_0 \approx$

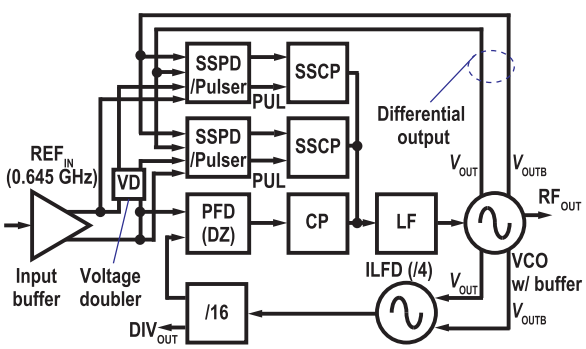

Fig. 1 Proposed sub-sampling PLL.

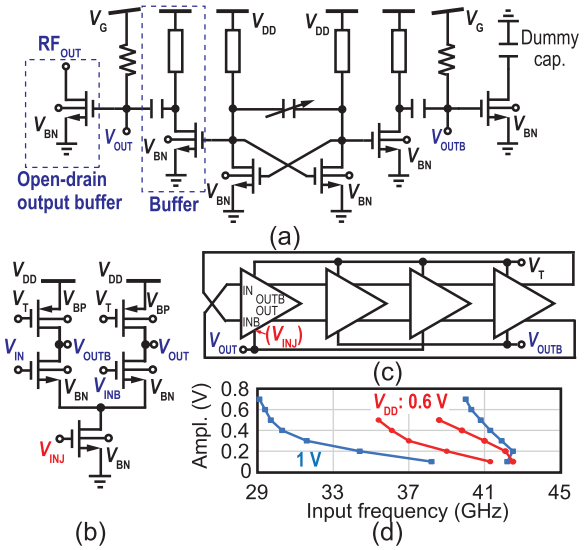

Fig. 2 (a) VCO topology with buffers, (b) delay cell, (c) 4-stage ILFD with a differential injection, and (d) simulated lock-range results of the ILFD when V_{DD} =1 V/0.6 V.

50Ω). It is based on nMOS common-source amplifiers for low-supply-voltage operation. It also includes common-source output buffers to drive sub-components such as an ILFD, and SSPDs. For measurement, an open-drain nMOS buffer is used. For fine frequency tuning, an nMOS-type varactor is employed. A back-gate FBB technique can be applied to nMOS transistors. From the post-layout simulation results, the tuning range was 41.13–41.68 GHz and 40.57–41.12 GHz under the supply voltage of 1 V (V_G =0.5 V) and 0.6 V (V_G =0.3 V), respectively. The range was not matched because of the lack of coarse tuning capability.

Figures 2 (b)–(d) shows the circuit topology of a 40-GHz input divide-by-4 ILFD and its post-layout simulation results. The four-stage ILFD using differential injection from the VCO is employed to maximize the lock range when the division ratio is 4. In Fig. 2 (d), the lock range, when the input voltage amplitude was 0.3 V, was 31.6–41.9 GHz and 37.0–41.0 GHz under the supply voltage of V_{DD} =1 V (V_G =0.5 V, V_T =0.3 V) and 0.6 V (V_G =0.3 V, V_T =0.17 V), respectively. The back-gate FBB technique was applied to nMOS and pMOS transistors.

Figures 3 (a) and (b) depict a pseudo-frequency-doubled SSPD/CP (FD-SSPDCP), including two pairs of SSPD/pulser/SSCP. In the SSPD, the parasitic capacitance of the transistors (SSCPs) is used for sample and hold operation. Ground-biased nMOSs cancel leakage from VCO outputs in hold operation [2], [11]. In Fig. 3 (b), the circuit topology of the SSCP is indicated. From the post-layout simulation results in Figs. 3 (c) and (d), it shows the operation range (versus the tuning voltage V_{TUNE}). The SSCP can be operated due to the back-gate FBB technique under the low-supply voltage of 0.6 V, as shown in Fig. 3 (d).

Figure 4 (a) shows the circuit topology of the conventional voltage doubler, which consists of two capacitors and nMOS/pMOS transistors [12]. When the input clock fre-

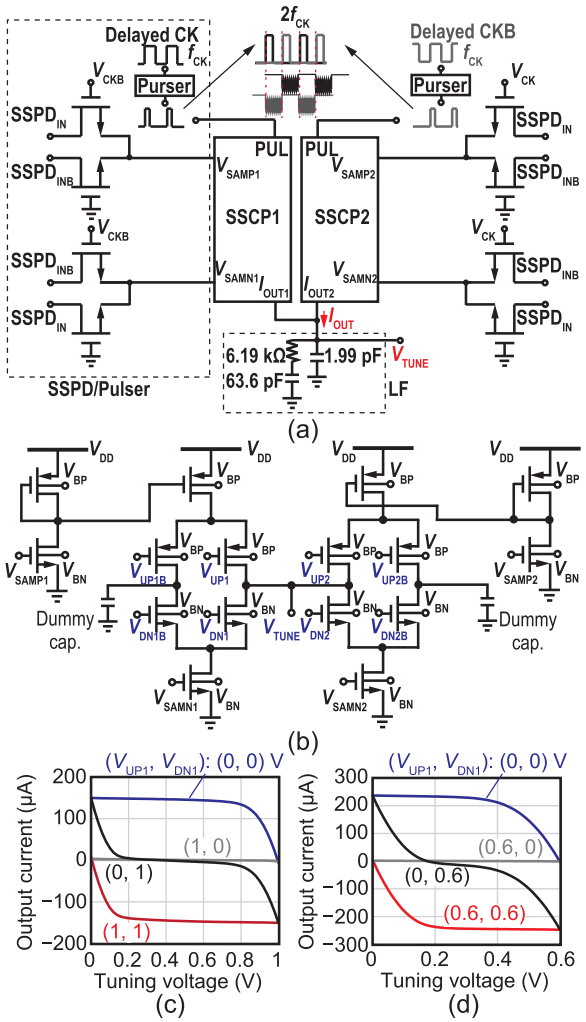

Fig. 3 (a) Pseudo frequency-doubled SSPD/CP (FD-SSPDCP) [11], (b) SSCP topology (i.e., SSCP1, SSCP2). Simulated output current results of the SSCP (V_{SAMN1} = V_{SAMN2} = V_{SAMP1} = V_{SAMP2} = $V_{DD}/2$, V_{UP2} = V_{UP2B} = V_{DD}, and V_{DN2} = V_{DN2B} = 0) when (c) V_{DD} =1 V and (d) V_{DD} =0.6 V.

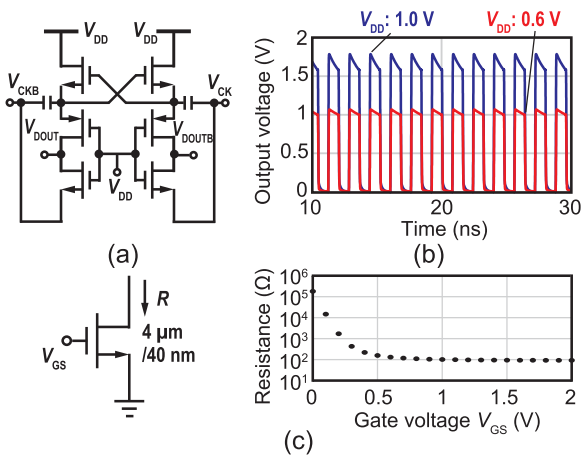

Fig. 4 (a) Voltage doubler topology and (b) simulated time-domain results when V_{DD} =1 V/0.6 V. (c) On/off resistance of an nMOS transistor for the SSPD and simulated resistance results of the transistor versus V_{GS}.

quency was 625 MHz, it can amplify the input amplitude of the clocks, as shown in the post-layout simulation results (Fig. 4 (b)). Figures 4 (c) and (d) indicate the on/off resistance of an nMOS transistor for the SSPD [3], [4]. Generally, the ratio between on/off resistance should be higher for an ideal sample and hold operation since the amplitude of output swing from SSPD affects in-band phase noise oriented from both the SSPD and the SSCP [4]. When V_{GS} =0 V, the off resistance of R was 181 kΩ. When V_{GS} =0.6 V and 1 V, the on-resistance of R were 132 and 101 Ω, respectively. By employing the voltage doubler, they can be reduced to 99.0 and 92.9 Ω, respectively (when V_{GS} =1.1 V and V_{GS} =1.8 V).

3. Measurement Results

Figure 5 (a) depicts a chip micrograph of the SSPLL, which was fabricated using a 55-nm CMOS DDC process. The total chip size, including RF and DC pads, is 1.42×0.800 mm^2. Figure 5 (b) shows an on-wafer measurement system. The chip was measured using a signal generator (SG), spectrum analyzers (SAs), and a signal source analyzer (SSA). The back-gate forward body biases of V_{BP} =0 V, and V_{BN} =0.6 V were employed under the supply voltage of 0.6 V, though they were not enabled when the power supply was 1 V. The total power consumption under the supply voltage of 0.6 V was 20.0 mW (52.6 mW when V_{DD} =1 V), including that of the ILFD (power consumption of 13.2 mW and 18.2 mW under 0.6 V and 1 V, respectively). The chip also consumed 12.4 mW to enable the frequency lock loop (excluding the ILFD).

Figures 6 (a) and (b) show the measured spectra of the SSPLL output (RF_{OUT}) at 41.3 GHz under the 1-V and 0.6-V supply voltages, respectively. Due to employing the proposed FD-SSPDCP, the spurs of −49.2 dB and −39.8 dB at $2 \times f_{REF}$ have occurred, respectively.

Figure 6 (c) indicates the measured phase noise in the free-running mode (V_{TUNE} =0 V) and the SSPLL mode, in addition to that of the reference signal (645 MHz). They were degraded at about 2 MHz owing to the external noise of the measurement system. The proposed SSPLL presents a 100-kHz-offset phase noise of −92.0 dBc/Hz, and a 705-fs RMS jitter (integrated from 1 kHz to 40 MHz) when V_{DD} =0.6 V, while a 224-fs RMS jitter was achieved when V_{DD} =1 V. By rejecting the external noise at about 2 MHz, the measured RMS jitter was 399 fs and 195 fs under 0.6 V and 1 V, respectively.

Table 1 gives a performance summary and comparison with other PLLs operating above 25 GHz. The proposed SSPLL shows good in-band phase noise characteristics compared with them of other PLLs and power scalability.

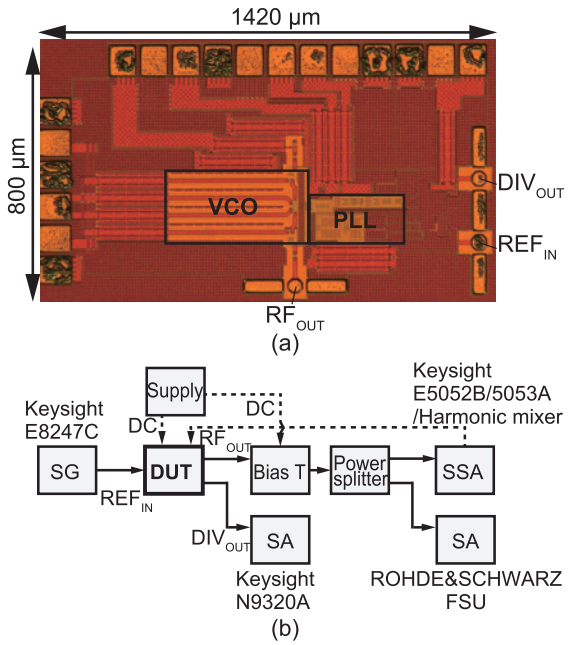

Fig. 5 (a) Chip microscope and (b) on-wafer measurement system.

Table 1 Performance summary and comparison of PLLs above 25 GHz.

Ref.	Tech.	V_{DD} (V)	f_{out} (GHz)	f_{ref} (GHz)	N	$PN_{in-band}$ (dBc/Hz)	IPN† (dBc)	J_{RMS}† (fs)	P_{DC} (mW)	FoM‡ (dB)	Area (mm^2)
This work	55 nm CMOS DDC	0.6 (w/ FBB)	41.3	0.645	64	−92.0 @100 kHz	−17.8 (1 k-40 M)	705 (1 k-40 M)	20.0 (w/o FLL)	−230.0	0.784▽
		1.0	41.3	0.646		−99.3 @100 kHz	−27.7 (1 k-40 M)	224 (1 k-40 M)	52.6 (w/o FLL)	−235.8	
[11]	40 nm CMOS	0.65, 0.9	45.0	1.41	32	−98.7 @100 kHz	−40.5 (0.1 k-40 M)	47.4 (0.1 k-40 M)	114.6	−245.9	0.4 (core)
[13]	250 nm BiCMOS	3.3	40.0	0.050	800	−92.5 @100 kHz	−34.7 (1 k-100 M)	104 (1 k-100 M)	323	−236.2	0.45 (core)
[14]	65 nm CMOS	1.0	40.5	0.1	405	−96△ @200 kHz	−26.8 (10 k-100 M)	228 (10 k-100 M)	8.8	−243.3	0.6 (core)
[15]	40 nm CMOS	0.9,1	62.6	0.04	1566	−89.7 @200 kHz	−23.9 (1 k-100 M)	230 (1 k-100 M)	42	−236.5	0.15 (core)
[16]	65 nm CMOS	1	60.5	0.040	1512	−78.5 @100 kHz	−28.8 (10 k-40 M)	290 (10 k-40 M)	32	−235.7	1.43▽
[17]	65 nm CMOS	1.1△	29.3	2.25	13	−92.8 @100 kHz	−39.1 (1 k-100 M)	85.6 (1 k-100 M)	24.3	−247.5	0.47▽

† Integrated phase noise (IPN), RMS jitter (J_{RMS}). ‡FoM = $20\log_{10}(J_{RMS}/1\,s) + 10\log_{10}(P_{DC}/1\,mW)$. ▽Chip area excluding pads. △Estimated from measured results.

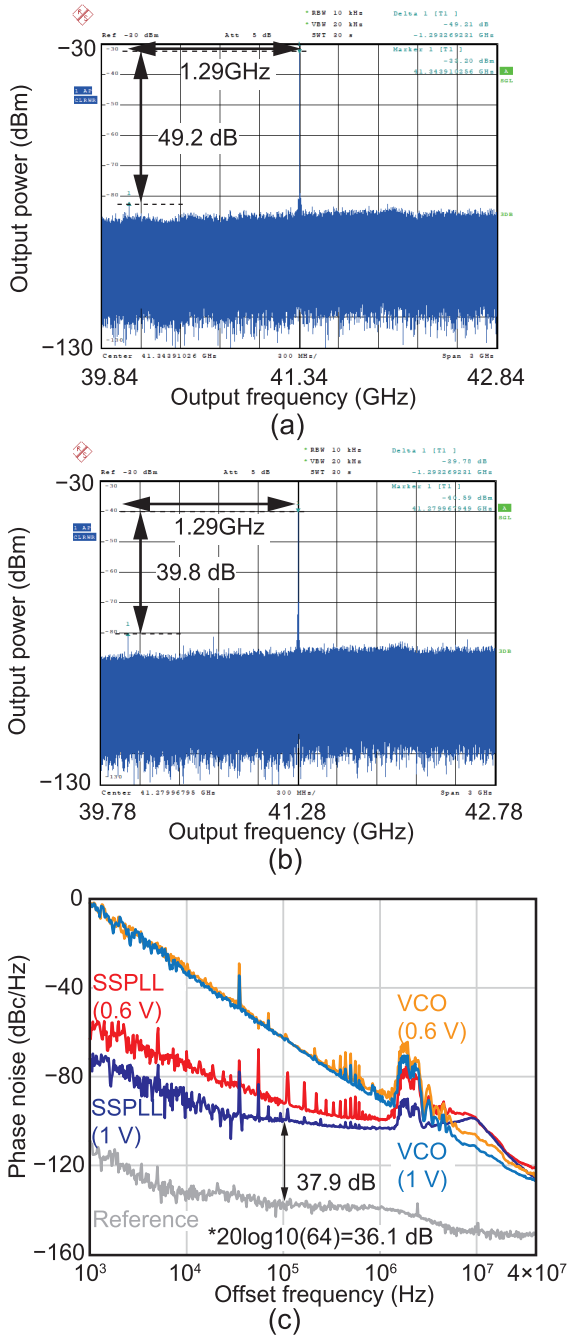

Fig. 6 Measured frequency spectra (a) when V_{DD} =1 V and (b) V_{DD} =0.6 V. (c) Measured phase noise of the 0.645-GHz reference, the free-running VCO, and the SSPLL when V_{DD} =1 V and V_{DD} =0.6 V.

4. Conclusion

This work presented a 0.6-V/1.0-V supply power-scalable SSPLL, which employed the back-gate FBB technique and the CMOS DDC process. Furthermore, the voltage doubler was applied to the SSPD to reduce the on-resistance of the transistor. Thanks to them, we demonstrated the SSPLL operation at 41.3 GHz with 62%-reduced power consumption and the 705-fs RMS jitter (228-fs RMS jitter when V_{DD} =1 V) under the supply voltage of 0.6 V. In the future, such a dual-mode power-scalable PLL must be required for 5G mmW applications; a power-saving PLL with lower than 5 mW (e.g., under the supply voltage of 0.6 V) for 64QAM data transmission and a high-performance PLL (e.g., under 1 V) for 256QAM data transmission.

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