FOREWORD

Special Section on Analog Circuits and Their Application Technologies

The concept of IoT (Internet of Things) can be recognized as a technology to build an intellectual society enabled with over 50billion sensing objects connected to internet, and it becomes fundamental in the current and future information and communication systems along with the data analysis technologies by machine learning. The total market of IoT is expected over 2 trillion dollars in 2025, and its economical ripple effect has strong impacts to IC industries especially in analog products for sensing, such as amplifiers, filters, and AD converters (ADC), and wireless/wireline communications. The productization of current systems including steps of PoC (proof of concept) and PoB (proof of business) strongly demands the short TAT (turn-around-time) development for electronics systems, and consequently, design approach using off-the-shelf devices is becoming more important. By taking account of this technology trend, the editorial committee has changed the title of the special section from "Analog Circuits and Related SoC Integration" to "Analog Circuits and Their Application Technologies" to encourage submissions designed by various application-oriented approaches including the off-the-shelf designs.

Here, we are happy to publish this special section illustrating analog circuit innovations in the fields of IoT, medical/bioelectronics and high-speed wireless communications. This year's special section includes two invited papers and ten submitted papers. The first invited paper, entitled "The design challenges of IoT: from system technologies to ultra-low power circuit," illustrates the transforming of economy and society by IoT and describes an IoT system model and associated design challenges. As a case study, authors introduce an ultra-low power multi-standard wireless transceiver SoC design in order to optimize architecture and circuits for the longest battery life. The second invited paper, entitled "Stimulator design of retinal prosthesis," discusses a two-dimensional electric neuro-stimulator system for artificial retina, and proposes stimulator circuits with biphasic current and charge balance to avoid electrolysis as well as a CMOS-based stimulator electrode array.

The ten submitted papers present various aspects in analog circuit design. The seven regular papers include subjects of a spur-cancelled clock generator for wireless SoCs, a current-mode low-pass filter with cutoff frequency of 1GHz, a 200MSps delta-sigma time-to-digital converter, a 500MHz bandwidth voltage-to-time converter with a two-step transition inverter, a 20GHz push-push VCO for 60GHz frequency synthesizer, a physical-weight based ADC measurement methodology and a beacon transmitter operating with PV film harvester designed with the off-the-shelf devices. Three briefs present various bioelectronics circuit techniques, such as a CMOS-based electrophoresis method for biomolecule manipulation, a current-mode ADC for biosensor array, and an amperometric sensor for bacteria counting.

On behalf of the editorial committee of this special section, I would like to express our sincere appreciation to all the authors of the submitted papers. I would also like to thank all the reviewers and all the committee members of this special section for their significant contributions to the editorial work. Finally, I would like to thank professor Kiichi Niitsu and Dr. Takeshi Ueno for their extensive work as guest editors.

Shoichi Masui, Guest Editor-in-Chief

Shoichi Masui *(Member)* received his B.S. and M.S. degrees from Nagoya University in Nagoya, Japan in 1982 and 1984, respectively. He received a Ph.D. degree from the Tokyo Institute of Technology in 2006. From 1994 to 1999, he was employed by Nippon Steel Corporation, where he was engaged in research on SOI devices and circuit design, and subsequently became responsible for nonvolatile memory circuit design and its application to radio frequency identification (RFID) tag ICs. From 1990 to 1992, he was a Visiting Scholar at Stanford University in Stanford, California, where he was involved in research on substrate-coupling noise in mixed-signal ICs. In 1999, he joined Fujitsu Limited; from 2000 to 2007, he was with Fujitsu Laboratories Ltd., where he was engaged in designing ferroelectric random access memory (FeRAM) for smart cards and RFIDs, reconfigurable logic LSIs for security applications, and low-power RF transceiver circuits. In 2001, he was a Visiting Scholar at the University of Toronto in Toronto, Ontario, Canada. From 2007 to 2012, he was a professor of the Research Institute of Electrical Communication at Tohoku University, where he conducted researches including RF/analog circuit design, its methodology for multi-standard radios, and its applications. Since 2012, he is with Fujitsu Laboratories Ltd. where he has been working on ultra-low-power wireless transceiver design, wireless sensing front-end for IoT as well as machine-learning technologies. Dr. Masui is a recipient of a commendation from the Minister of Education, Culture, Sports, Science, and Technology in Japan in 2004 for his FeRAM research achievements.