IEICE TRANS. ELECTRON., VOL.E101–C, NO.5 MAY 2018

INVITED PAPER *Special Section on Innovative Superconducting Devices Based on New Physical Phenomena*

Recent Progress on Reversible Quantum-Flux-Parametron for Superconductor Reversible Computing

Naoki TAKEUCHI[†,††a)], **Yuki YAMANASHI**[†,†††], ***and*** **Nobuyuki YOSHIKAWA**[†,†††], ***Members***

SUMMARY We have been investigating reversible quantum-flux-parametron (RQFP), which is a reversible logic gate using adiabatic quantum-flux-parametron (AQFP), toward realizing superconductor reversible computing. In this paper, we review the recent progress of RQFP. Followed by a brief explanation on AQFP, we first review the difference between irreversible logic gates and RQFP in light of time evolution and energy dissipation, based on our previous studies. Numerical calculation results reveal that the logic state of RQFP can be changed quasi-statically and adiabatically, or thermodynamically reversibly, and that the energy dissipation required for RQFP to perform a logic operation can be arbitrarily reduced. Lastly, we show recent experimental results of an RQFP cell, which was newly designed for the latest cell library. We observed the wide operation margins of more than 4.7 dB with respect to excitation currents.
key words: *reversible computing, adiabatic logic, QFP*

1. Introduction

The continuous miniaturization of complementary metal–oxide–semiconductor (CMOS) device has significantly contributed to the improvement in the performance and energy efficiency of microprocessors over several decades. The switching energy (energy dissipation per switching event) of a single CMOS gate is expected to reach $100\,k_BT$, where k_B is the Boltzmann's constant and T is temperature, by reducing the feature size to approximately 5 nm [1]. However, since $100\,k_BT$ switching energy is a thermal limit for normal (non-adiabatic) CMOS logic [1], [2], it is not practical to achieve even smaller switching energy via device miniaturization. One possible solution to go beyond this limit is to adopt reversible computing [3], [4]. In reversible computing, logic gates can operate in a thermodynamically reversible manner and thus energy dissipation becomes zero in the quasi-static limit. Reversible logic gates have been proposed using several logic devices, which include adiabatic CMOS [5], nanomagnetic logic [6], [7], nano electro mechanical system (NEMS) [8], and superconductor logic [9].

In a previous study [10], we proposed a superconductor reversible logic gate using adiabatic quantum-flux-parametron (AQFP) [11], which is an adiabatic superconductor logic based on quantum-flux-parametron (QFP) [12]. The proposed reversible gate, which is designated as reversible QFP (RQFP), has a symmetrical structure and is bijective, which indicates the thermodynamic and logical reversibility of RQFP. We numerically demonstrated that RQFP can perform logic operations with an energy dissipation even below the Landauer bound [13] or $k_BT\ln 2$. Moreover, we fabricated and tested RQFP gates in the liquid He, so as to show that RQFP is a practical reversible logic gate. We also studied the mechanism of energy dissipation in irreversible logic gates [14], which helps to understand the relationship between reversibility and energy dissipation.

In this paper, we review the recent progress of RQFP toward realizing superconductor reversible computers. In Chapter 2, we explain briefly the operation principle of AQFP and adiabatic switching. In Chapters 3 and 4, based on our previous studies [10], [14], we review the difference between irreversible logic gates and RQFP in light of time evolution and energy dissipation using numerical calculation. We show that RQFP is thermodynamically, as well as logically, reversible. In Chapter 5, we show measurement results of an RQFP cell, which is newly designed for the current cell library. We found that the RQFP cell works with wide operation margins and is compatible with latest AQFP cells, which ensures the use of the RQFP cell to logic circuit design.

2. Adiabatic Quantum-Flux-Parametron (AQFP)

Figure 1 shows the equivalent circuit of an AQFP gate, which is composed of two superconductor loops including a Josephson junction. Depending on the polarity of the input current I_{in}, one of the Josephson junctions J_1 and J_2 switches, when the ac excitation current I_x is increased and excitation fluxes are applied to the gate through the mutual inductance $M = k(L_xL)^{0.5}$, where we assumed that AQFP is symmetrical; $k = k_1 = k_2$, $L_x = L_{x1} = L_{x2}$, and $L = L_1 = L_2$. As a result, a single-flux-quantum (SFQ) is stored in the gate, and the output current I_{out} is generated through the load inductor L_q. The polarity of I_{out} shows its logic state; a positive I_{out} represents logic 1, and a negative I_{out} represents logic 0. The typical circuit parameters are shown in the caption, where I_c is the critical current of J_1 and J_2. Figure 2 represents a transient analysis of AQFP [15]. The figure indicates that I_{out} is generated when $2MI_x$ reaches approximately Φ_0, and that the polarity of I_{out} or the logic state is determined by the direction of I_{in}. Since an AQFP gate must

Manuscript received September 28, 2017.
Manuscript revised January 9, 2018.
[†]The authors are with Institute of Advanced Sciences, Yokohama National University, Yokohama-shi, 240–8501 Japan.
[††]The author is with PRESTO, Japan Science and Technology Agency, Kawaguchi-shi, 332–0012 Japan.
[†††]The authors are with the Department of Electrical and Computer Engineering, Yokohama National University, Yokohama-shi, 240–8501 Japan.
a) E-mail: takeuchi-naoki-kx@ynu.jp
DOI: 10.1587/transele.E101.C.352

be reset before the next input data comes, I_x is an ac current with trapezoidal or sinusoidal profiles.

Figure 3 shows the time evolution of θ_1 and θ_2, which are the phase differences of J_1 and J_2, respectively, during excitation. θ_1 and θ_2 gradually change as $2MI_x$ increases, which indicates that the logic state of AQFP can be changed quasi-statically and adiabatically, or thermodynamically reversibly. Because of this adiabatic switching [16], [17], the switching energy of a single AQFP gate can fall below k_BT and becomes zero in the quasi-static limit [18]. At a finite speed, an AQFP gate dissipates energy proportional to the ratio of the time constants of Josephson junctions to the rise and fall time of I_x [19], where the time constant is given by $2\pi L_j/R = \Phi_0/I_cR$ using Josephson inductance $L_j = \Phi_0/2\pi I_c$ and damping resistance R. Therefore, in AQFP logic, high critical-current-density fabrication processes and/or underdamed Josephsson junctions are adopted, so as to reduce time constants and energy dissipation. In this study, all Josephson junctions are unshunted, so the damping resistance corresponds to sub-gap resistance.

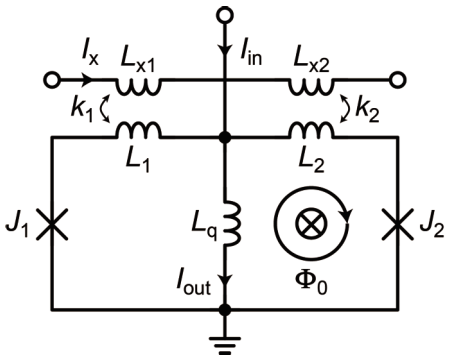

Fig. 1 AQFP gate. One of J_1 and J_2 switches, depending on the direction of I_{in}. The polarity of I_{out} shows its logic state. The typical parameters are: $\beta_L = 2\pi LI_c/\Phi_0 = 0.2, \beta_q = 2\pi L_q I_c/\Phi_0 = 0.8$.

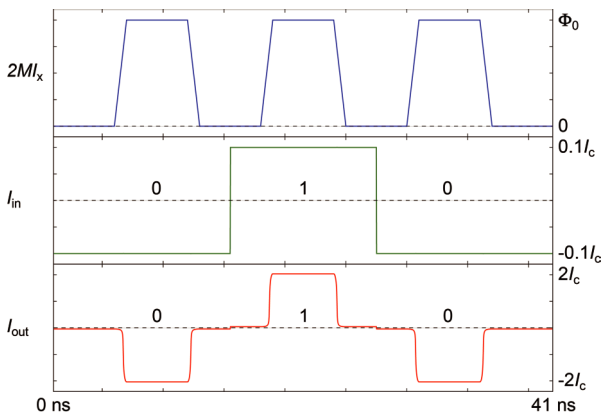

Fig. 2 Transient analysis of an AQFP gate. I_{out} is generated, when $2MI_x$ of approximately Φ_0 is applied. The polarity of I_{out} is determined by that of I_{in}.

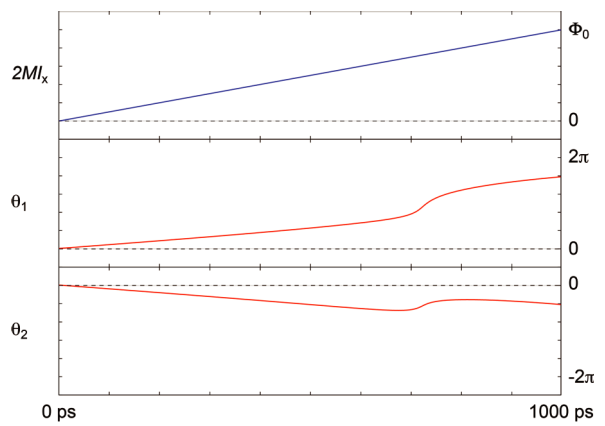

Fig. 3 Time evolution of the phase differences in AQFP. Both θ_1 and θ_2 change gradually as I_x increases, which indicates that this switching process can be performed thermodynamically reversibly.

Recently, much effort has been spent on the development of energy-efficient AQFP microprocessors [20]–[22] and AQFP interfaces for superconductor detectors [23] through building the circuit design environment for AQFP logic [22], [24]–[26].

3. Irreversible AQFP Logic Gate

Although a single AQFP gate can operate thermodynamically reversibly, it is not easy to achieve a reversible logic gate using AQFP. This is because some AQFPs can operate non-adiabatically, depending on how we interconnect AQFPs in logic gate design. We take an example of an irreversible logic gate using a 1-bit-erasure (1BE) gate [14], the schematic of which is shown in Fig. 4. A 1BE gate includes six AQFPs (A through C and X through Z), which are interconnected via magnetic couplings. Gates A and C operate as two-output splitter (SPL) gates, and Gates Y operates as a three-input majority (MAJ) gate. A SPL gate is a multi-fanout buffer gate, and a MAJ gate is a logic gate, the output of which is determined by the majority vote of the inputs. I_{xs} and I_{xm} are the excitation currents for Gates A through C and Gates X through Z, respectively. I_{xm} is increased after I_{xs} is ramped up, so as to proceed logic operations from left to right. a, b, and c are the inputs, and $x = a$, $y = ab+bc+ca$, and $z = c$ are the outputs. While a and c are copied to x and z, respectively, b is not. Thereby, it is not possible to determine b after a logic operation, which indicates that a 1BE gate is not bijective and is logically irreversible [27].

Figure 5 shows the time evolution of the phase differ-

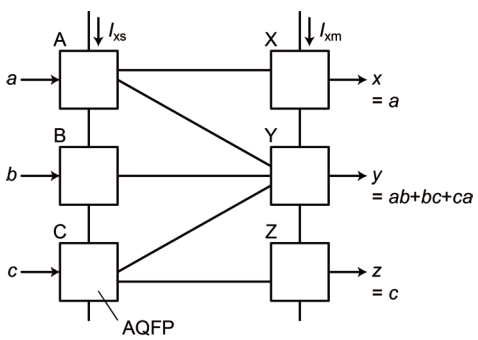

Fig. 4 1BE gate. Since it is not possible to predict b after calculation, this gate is logically irreversible.

ences (θ_1 and θ_2) of the Josephson junctions (J_1 and J_2) of the AQFPs in a 1BE gate during a logic operation. For $a = b = c = 1$, all the phase differences change gradually, which indicates that all the AQFPs (A through C and X through Z) in the 1BE gate can operate quasi-statically and adiabatically, or thermodynamically reversibly. On the other hand, for $a = 1$, $b = 0$, and $c = 1$, θ_1 of Gate B changes non-adiabatically, while the gate is being reset. Therefore, a 1BE gate is thermodynamically, as well as logically, irreversible. The non-adiabatic phase change in Gate B for $a = 1$, $b = 0$, and $c = 1$ is due to the interaction between Gates B and Y. While the logic state of Gate B is 0, that of Gate Y is 1, thereby tilting the potential energy of Gate B toward logic 1. As a result, Gate B switches suddenly from logic 0 to 1 while being reset, as shown in Fig. 5.

Figure 6 shows the energy dissipation of the 1 BE gate for a logic operation as a function of the rise and fall time, τ_{rf}, of the excitation currents (I_{xs} and I_{xm}), which were calculated by using the Josephson circuit simulator, JSIM_n [28], [29]. The lines represent the calculation results for $T = 0$ K, and the markers represent those for $T = 4.2$ K, which are the averages over 500 iterations. The figure shows that there are no significant differences in the calculated energy dissipation between 0 K and 4.2 K. For $a = b = c = 1$, since all the AQFPs can operate adiabatically as shown in Fig. 5, energy dissipation decreases in inverse proportion to τ_{rf}. Conversely, minimum values appear in the energy dissipation for $a = 1$, $b = 0$, and $c = 1$. This is because, as shown in Fig. 5, Gate B experiences non-adiabatic processes and induces non-zero minimum energy dissipation, which is much larger than $k_B T \ln 2$. The detailed discussion on the mechanism of the energy dissipation in irreversible logic gates is given in the literature [14].

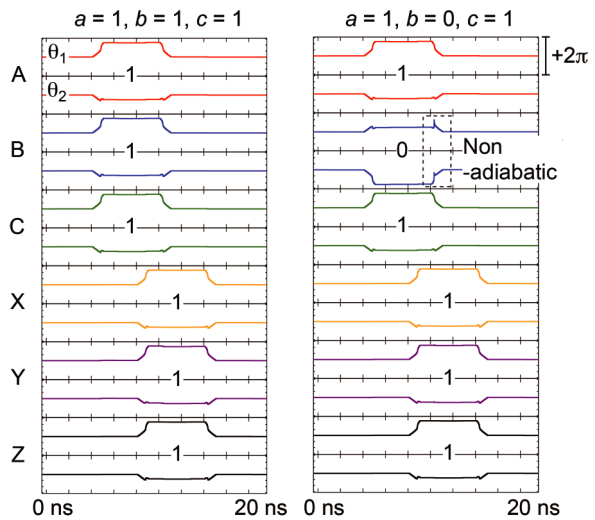

Fig. 5 Time evolution of the phase differences of the AQFPs in a 1BE gate. For $a = 1$, $b = 0$, and $c = 1$, θ_1 and θ_2 change non-adiabatically, which indicates that a 1BE gate is thermodynamically, as well as logically, irreversible.

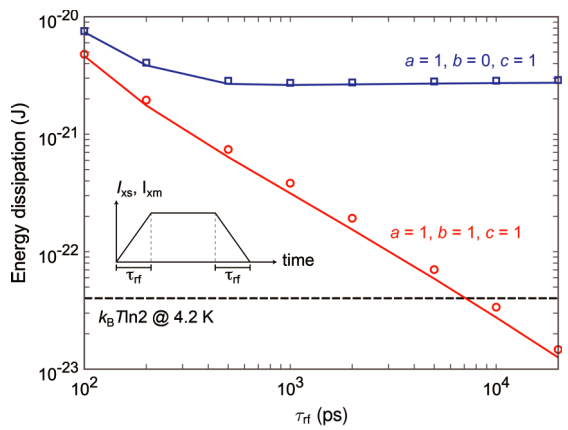

Fig. 6 Energy dissipation of a 1BE gate for a logic operation. For $a = 1$, $b = 0$, and $c = 1$, energy dissipation has a minimum because of the non-adiabatic switching shown in Fig. 5.

4. Reversible Quantum-Flux-Parametron (RQFP)

One reason why a 1BE gate is thermodynamically irreversible is that the gate is not bijective. Another reason is that the schematic of a 1BE gate is asymmetrical and thus data cannot propagate bi-directionally. These two points represent the time irreversibility of 1BE gates and should be solved to achieve a reversible logic gate, because a system is thermodynamically reversible if and only if the system is time reversible [30], [31].

Figure 7 shows our proposed reversible logic gate, RQFP. Gates A through C operate as three-output SPL gates, and Gates X through Z operate as three-input MAJ gates. The outputs of RQFP are given by $x = \neg ab + bc + c\neg a$, $y = a\neg b + \neg bc + ca$, and $z = ab + b\neg c + \neg ca$, where a, b, and c are the inputs. From the truth table [10], it is obvious that RQFP is bijective or logically reversible. Since the schematic of the SPL gates (Gates A through C) is the same as that of the MAJ gates (Gates X through Z), RQFP is symmetrical and can perform logic operations bi-directionally. Therefore, RQFP solves the two challenges toward realizing reversible logic gates.

Figure 8 shows the time evolution of the phase differences of the Josephson junctions of the AQFPs in RQFP during a logic operation. For both data combinations, $a =$

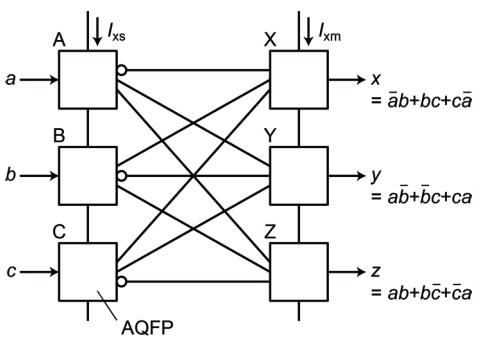

Fig. 7 RQFP gate. Because of its symmetrical structure and bijective function, logic operations can be performed bi-directionally.

$b = c = 1$, and $a = 1$, $b = 0$, and $c = 1$, all the phase differences change gradually, which indicates that all the AQFPs (A through C and X through Z) in RQFP can operate quasi-statically and adiabatically, or thermodynamically reversibly. This is the case with all the data combinations [14]. Therefore, RQFP is thermodynamically, as well as logically, reversible in the quasi-static limit.

Figure 9 shows the calculated energy dissipation of RQFP for a logic operation as a function of τ_{rf}. The lines represent the calculation results for $T = 0$ K, and the markers represent those for $T = 4.2$ K, which are the averages over 500 iterations. The figure shows that, for all the input data combinations, the energy dissipation decreases in inverse proportion to τ_{rf} and falls below $k_B T \ln 2$ for τ_{rf} of approximately 7,000 ps. This is because, due to thermodynamic reversibility, the time evolution of the phase differences of the Josephson junctions in all the AQFPs in RQFP approach quasi-static processes as τ_{rf} increases.

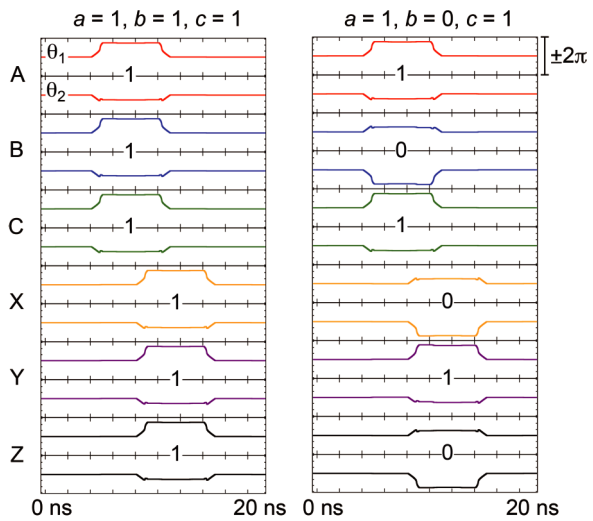

Fig. 8 Time evolution of the phase differences of the AQFPs in RQFP. All the phase differences can be changed quasi-statically and adiabatically for all the input data combinations, which shows that RQFP is thermodynamically, as well as logically, reversible.

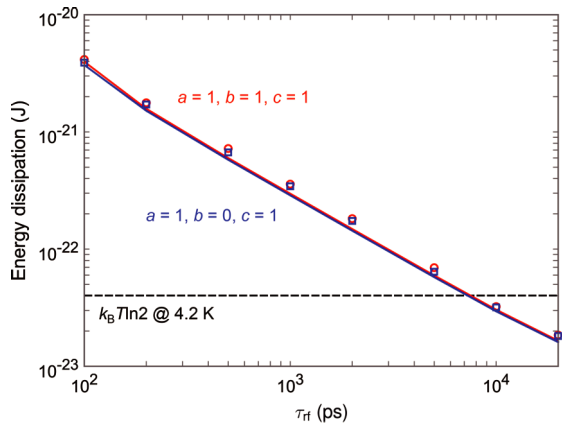

Fig. 9 Energy dissipation of RQFP for a logic operation. For all the input data combinations, energy dissipation decreases in inverse proportional to τ_{rf}.

5. Experiment

In the preceding chapters, we reviewed our previous numerical studies. Our next step is to design and demonstrate reversible logic circuits using RQFP cells. In order to design RQFP-based circuits, we need a cell library including both RQFP cells and AQFP logic cells, as it is possible that we will combine RQFP cells with basic AQFP logic cells, such as buffers (BUFs) and inverters. In a previous study [10], we fabricated RQFP cells using the AIST 2.5 kA/cm^2 standard process (STP2) [32] and demonstrated their correct logic operations, where the RQFP cells were driven by three-phase excitation currents. However, the previously designed RQFP cell is not compatible with the current AQFP logic cells due to the difference in fabrication processes and excitation schemes; the latest AQFP cells are designed and fabricated using the AIST 10 kA/cm^2 high-speed standard process (HSTP) [24], and they are driven by the four-phase excitation mode using a pair of ac excitation currents and a dc-offset current [24]. Therefore, in this chapter, we design and demonstrate a new RQFP cell for the latest cell library. It is noteworthy that, while basic AQFP logic cells are easily designed by arraying four types of building blocks, which is called minimal design [22], RQFP cells are custom-designed to ensure reversibility; the schematics of the SPL and MAJ gates in RQFP cells are different from those of the counterparts in minimal design. For instance, while the MAJ gate in minimal design includes three AQFPs, the MAJ gate in RQFP includes one AQFP as shown in Fig. 7. Thus, it is worth demonstrating new RQFP cells for the latest cell library.

Figure 10 shows a micrograph of the circuit to test the RQFP cell, which was fabricated using HSTP. The RQFP cell is placed between AQFP BUF chains to confirm its compatibility with current AQFP cells. The layout of the RQFP cell was designed using an inductance extraction tool, InductEx [33], [34]. The dimension of the RQFP cell is 180 μm $\times$ 145 μm, which is only 36% of that of the original design (270 μm $\times$ 270 μm) [10]. Further miniaturization might be possible by using a three-dimensional fabrication process [35]. I_{x1} and I_{x2} are the excitation currents, I_{ina} through I_{inc} are the input currents, which are applied to the RQFP cell through BUF chains, and V_{outx} through V_{outz} are the output voltages, which are generated by using the dc superconducting quantum interference devices (dc-SQUIDs) coupled to AQFPs. The circuit is driven by the four-phase excitation mode using I_{x1} and I_{x2} [24]. We operated this circuit in the liquid He. Figure 11 shows the waveforms of the experiment, which shows the correct logic operations of RQFP for all the input data combinations. The measured operation margins were 4.7 dB and 5.0 dB for I_{x1} and I_{x2}, respectively. The above results confirm the compatibility between the RQFP cell and current AQFP cells, thus ensuring the use of the RQFP cell to logic circuit design.

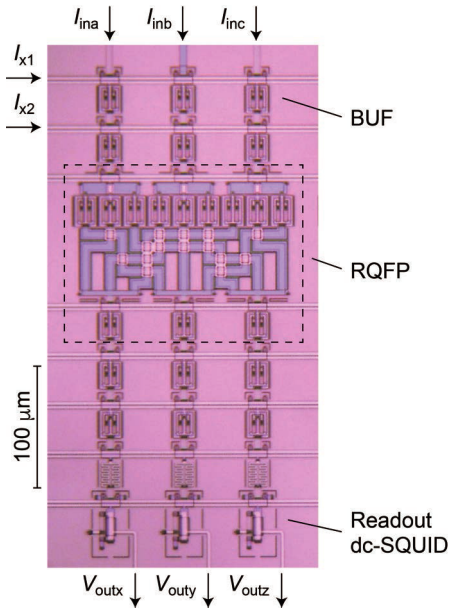

Fig. 10 Micrograph of the circuit to test the RQFP cell. The dimension of the RQFP cell is 180 μm × 145 μm. The outputs are read out through the readout dc-SQUIDs.

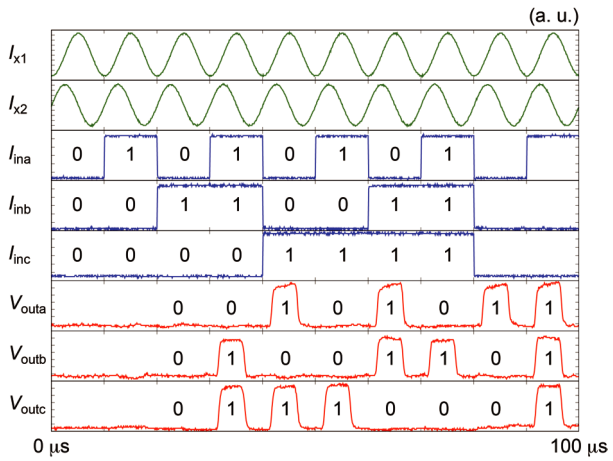

Fig. 11 Waveforms of the experiment. The correct logic operations of RQFP are observed for all the input data combinations.

6. Conclusions

We reviewed the recent progress of our proposed reversible logic gate, RQFP. We compared an irreversible logic gate (1BE) with RQFP from the viewpoint of time evolution and energy dissipation using numerical calculation. All the AQFPs included in RQFP can operate quasi-statically and adiabatically, and thus the energy dissipation required for RQFP to perform a logic operation becomes zero in the quasi-static limit. On the other hand, some AQFPs in the 1BE gate can operate non-adiabatically, and therefore the energy dissipation has a minimum, depending on the input data combination.

We redesigned the RQFP cell for the current cell library. We fabricated a test circuit using HSTP, which includes the RQFP cell, and confirmed the correct logic operations of it. Moreover, the measurement results revealed the wide operation margins of the RQFP cell. The above results indicate that the RQFP cell can be used for logic circuit design. For our next step, we will design somewhat complex logic circuits, such as an eight-bit adder, using the RQFP cell. We will discuss the usefulness of reversible computing in light of energy dissipation and hardware complexity through designing and demonstrating RQFP-based circuits.

Acknowledgments

The present study was supported by a Grant-in-Aid for Scientific Research (S) (No. 26220904) from the Japan Society for the Promotion of Science (JSPS), PRESTO (No. JPMJPR1528) from the Japan Science and Technology Agency (JST), and the MEXT Program for Promoting the Reform of National Universities. The circuits were fabricated in the Clean Room for Analog-digital superconductiVITY (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the high-speed standard process (HSTP). We would like to thank C.J. Fourie for providing the 3D inductance extractor, InductEx.

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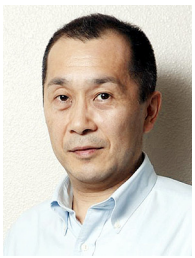
Naoki Takeuchi received the B.S., M.E., and Ph.D. degrees from Yokohama National University, Yokohama, Japan, in 2008, 2010, and 2014, respectively, all in electrical and computer engineering. He was an electronic circuit designer at SONY from 2010 to 2011; and a Postdoctoral Researcher at National Institute of Information and Communications Technology and at Japan Society for the Promotion of Science from 2014 to 2015. Since 2015, he has been with the Institute of Advanced Sciences, Yokohama National University, where he is now an Associate Professor; and with Japan Science and Technology Agency, where he is now a PRESTO Researcher. He has been engaged in the research and development of superconductor digital circuits: rapid single-flux-quantum logic, adiabatic quantum-flux-parametron logic, and reversible computing. Dr. Takeuchi is a member of the Japan Society of Applied Physics and the Institute of Electronics, Information and Communication Engineers of Japan.

Yuki Yamanashi received the B.E., M.E., and Ph.D. degrees in electrical and computer engineering from Yokohama National University, in 2003, 2005, and 2007, respectively. From 2007 to 2012, he was with Interdisciplinary Research Center, Yokohama National University. Since 2012, he has been with Department of Electrical and Computer Engineering, Yokohama National University. His research interests include superconductive circuit design and its applications. He is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Japan Society of Applied Physics, the Institute of Electrical Engineering of Japan, Cryogenics and Superconductivity Society of Japan, and the Institute of Electrical and Electronics Engineers.



Nobuyuki Yoshikawa received the B.E., M.E., and Ph.D. degrees in electrical and computer engineering from Yokohama National University, Yokohama, Japan, in 1984, 1986, and 1989, respectively. Since 1989, he has been with the Department of Electrical and Computer Engineering, Yokohama National University, where he is currently a Professor. His research interests include superconductive devices and their application in digital and analog circuits. He is also interested in single-electron-tunneling devices, quantum computing devices, and cryo-CMOS devices. Dr. Yoshikawa is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Japan Society of Applied Physics, the Institute of Electrical Engineering of Japan, and Cryogenics and Superconductivity Society of Japan.