IEICE TRANS. ELECTRON., VOL.E101–C, NO.5 MAY 2018

INVITED PAPER *Special Section on Innovative Superconducting Devices Based on New Physical Phenomena*

Thermally Assisted Superconductor Transistors for Josephson-CMOS Hybrid Memories

Kyosuke SANO[†a)], **Masato SUZUKI**[†], **Kohei MARUYAMA**[†], **Soya TANIGUCHI**[†], ***Nonmembers***, **Masamitsu TANAKA**[†], **Akira FUJIMAKI**[†], **Masumi INOUE**[††], ***and*** **Nobuyuki YOSHIKAWA**[†††], ***Members***

SUMMARY We have studied on thermally assisted nano-structured transistors made of superconductor ultra-thin films. These transistors potentially work as interface devices for Josephson-CMOS (complementary metal oxide semiconductor) hybrid memory systems, because they can generate a high output voltage of sub-V enough to drive a CMOS transistor. In addition, our superconductor transistors are formed with very fine lines down to several tens of nm in widths, leading to very small foot print enabling us to make large capacity hybrid memories. Our superconductor transistors are made with niobium titanium nitride (NbTiN) thin films deposited on thermally-oxidized silicon substrates, on which other superconductor circuits or semiconductor circuits can be formed. The NbTiN thickness dependence of the critical temperature and of resistivity suggest thermally activated vortex or anti-vortex behavior in pseudo-two-dimensional superconducting films plays an important role for the operating principle of the transistors. To show the potential that the transistors can drive MOS transistors, we analyzed the driving ability of the superconductor transistors with HSPICE simulation. We also showed the turn-on behavior of a MOS transistor used for readout of a CMOS memory cell experimentally. These results showed the high potential of superconductor transistors for Josephson-CMOS hybrid memories.

key words: *nanodevices, thermally assisted device, single-flux-quantum logic, superconducting integrated circuits*

1. Introduction

Single-flux-quantum (SFQ) circuits [1] are expected to be next-generation devices enabling high-performance computing because of their natures of high-speed operation and low power consumption. Microprocessors or accelerators made up of more than 10,000 Josephson junctions (JJs) have been demonstrated [2]–[4]. In particular, programs stored in an embedded memory have been executed in a bit-serial microprocessor at 50 GHz for bit-operations [5], and a bit-parallel arithmetic logic unit has successfully been demonstrated at 50 GHz [6]. These demonstrations show that SFQ large-scale logic circuits have very high potential for high performance computing, that is, high-speed and energy-efficient computing. The microprocessors with an optimized architecture for SFQ circuits can achieve better performance in both the computing power measured in the number of million instructions per second (MIPS) and the power efficiency (MIPS/W) than the CMOS (complementary metal oxide semiconductor) microprocessors, even if the cooling penalty is considered.

On the other hand, it still remains how to build large-capacity memories operating at low temperatures, because superconducting loops needed for storing an SFQ require large footprints. To overcome this drawback, several memories have been proposed so far, such as a Josephson-CMOS hybrid memory [7], magnetic-Josephson-junction-based memories [8], [9]. Note that the drivers for bit-lines and for word-lines are one of the most important subjects for development of large-capacity matrix memories.

Among the above-mentioned memories, a Josephson-CMOS hybrid memory, which hybridizes high-speed SFQ circuits with well-established high-density CMOS memories, has the largest capacity with present technology [10]–[13]. However, there is a major problem with the combination of SFQ and CMOS circuits due to the lack of appropriate interfaces, that is, the drivers. CMOS amplifiers working as a driver consume huge power, while output voltages of SFQ circuits are too small to drive semiconductor transistors directly. Although superconducting quantum interference device (SQUID) amplifiers [14] and Suzuki stacks [15] have been used to generate high output voltages, they need very large footprints and much power, unacceptable for highly integrated Josephson–CMOS hybrid memory systems.

Recently, an electrothermal nano-structured transistor called a nanocryotron (nTron) [16] was proposed and demonstrated by a group at the Massachusetts Institute of Technology (MIT) as a three-terminal superconductive device. nTrons can act as a current-voltage transformer in a scheme of the source-grounded operation, and have high sensitivity for gate currents as well as SFQ circuits. Most important feature of nTrons is high output voltage in the sub-V range with high impedance in the kilo-Ohm range. This feature enables us to drive CMOS circuits directly. Furthermore, nTrons can achieve very low-power amplification with sufficiently small footprints at a cryogenic temperature compared with CMOS amplifiers. With these advantages, in previous study, we proposed a highly integrated Josephson–CMOS hybrid memories using the nTrons [17].

Although the nTrons reported by the MIT group were fabricated using niobium nitride (NbN) thin films [16], the crystallinity of NbN thin films is strongly influenced by the substrate. Therefore, we examined niobium titanium nitride

Manuscript received October 1, 2017.
Manuscript revised December 25, 2017.

[†]The authors are with Nagoya University, Nagoya-shi, 464–8603 Japan.
[††]The author is with Meijo University, Nagoya-shi, 468–8502 Japan.
[†††]The author is with Yokohama National University, Yokohama-shi, 240–8501 Japan.
a) E-mail: k_sano@super.nuee.nagoya-u.ac.jp

DOI: 10.1587/transele.E101.C.370

(NbTiN) thin films for the fabrication of nTrons. NbTiN thin films can be suitable for highly integrated Josephson–CMOS hybrid systems due to their good superconducting properties on various substrates, such as Si and SiO_2 wafers [18]. The aim of this study is to show that nTrons fabricated with NbTiN thin films potentially work as transistors between Josephson devices and CMOS memories. In this study, we investigated the thickness dependency of the critical temperature, T_c, and the resistivity, to figure out the characteristics of NbTiN nTrons, and fixed the design based on the obtained characteristics. We then proposed a thermal-electrical model of the nTron in order to perform circuit simulation with the designed nTron and MOS transistors using the HSPICE simulator. Finally, we fabricated nTrons using NbTiN thin films, and tested the readout from the CMOS memories using the fabricated nTrons, demonstrating the applicability of NbTiN nTrons for Josephson-CMOS hybrid memories. Although a high-electron-mobility transistor driven by the NbN nTron has already been demonstrated [19], NbTiN nTron is attractive for highly integrated hybrid systems. This is because that ultra-thin films of NbTiN can be easily deposited on Si or SiO_2 substrates without buffer layers. Therefore, we can highly integrated the SFQ circuits, the NbTiN nTrons, and the CMOS memories on the same Si substrates.

The paper is organized as follows: we briefly review the operation of an nTron and show the characteristics of NbTiN thin films obtained from experiments in Sect. 2. Then, we describe the proposed device model and show HSPICE simulation including an nTron and MOS transistors in Sect. 3. In Sect. 4, we report the measurement results in readout test using the fabricated NbTiN nTrons and CMOS memory cells. We give concluding remarks in Sect. 5.

2. Evaluation of NbTiN Thin Films for Nanocryotron (nTron)

2.1 Structure and Operation of an nTron

nTrons are fabricated by processing a superconducting thin film and have three terminals (the drain, source, and gate), similar to field-effect transistors (FETs), as depicted in Fig. 1 [16]. The gate and channel (drain-source) paths cross at right angles, and their intersection is referred to as a choke and is narrow on a several tens of nanometers. The channel current, $I_{channel}$, can be controlled by the gate current, I_{gate}, supplied.

In the operation of nTrons, a superconducting current less than the critical current of the channel, $I_c^{channel}$, is supplied from the drain to the source in the initial state. By supplying I_{gate} over the critical current of the gate, I_c^{gate}, the superconductive state in the choke is broken down and a resistive area, called hotspot [20] is formed. The area of the hotspot expands via Joule heat and a wide resistive area is formed, as shown in Fig. 1. The darkness in Fig. 1 illustrates the degree of the temperature rise. Thus, an nTron achieves high resistance and the supply current flows to the load resistance, R_L. The Joule heat diffuses and escapes to the substrate after I_{gate} is turned off, and the nTron cools and returns to the superconductive state.

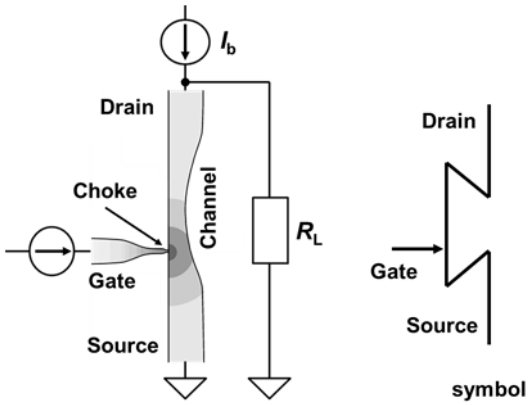


Fig. 1 A nanocryotron (nTron) [16].

The nTrons driven by the SFQ circuits was reported in [19]. It is estimated that the Joule heat generated in the choke is lower than 10^{-19} J. The heat is conducted through the substrate because superconductors are impenetrable to heat. The temperature of the sapphire hemisphere can be raised using the energy over a radius of just a few nm even if the heat spreads isotropically. Therefore, it is insufficient for forming large resistive area in the channel part. From the aspect of superconductivity, pseudo-two-dimensional behavior enlarges the fluctuation of the phase in the superconducting macroscopic wave function, which promotes the creation and the unbinding of vortex-antivortex pair (VAP) as described by Yamashita [21] inside the films, at T_c, this effect contributes to increase sensitivity to the gate currents during their operation. Therefore, we investigated the characteristics of ultra-thin films of the NbTiN in this study.

2.2 Characteristics of NbTiN Thin Films

To build a highly integrated Josephson–CMOS hybrid system, nTrons should be fabricated on the insulating layer (SiO_2) in the SFQ circuits. Therefore, in this study, we fabricated nTrons using NbTiN thin films, the superconducting properties of which do not strongly depend on the substrate.

Typical SFQ circuits are fabricated using the Nb process [22] and operate in liquid helium. Therefore, the T_c of the NbTiN nTrons should be higher than and close to the temperature of liquid helium (4.2K) for nTrons switching to the normal state with the energy of an SFQ ($I_c\Phi_0 = 4.0 \times 10^{-19}$ J). The resistivity should be sufficiently high to obtain high impedance and a high output voltage.

To meet these requirements, we evaluated the thickness dependencies of T_c and the resistivity for designing NbTiN nTrons. Figure 2 shows the measurement results. T_c decreased with thinner films, and we obtained the minimum T_c of 4.9K in the helium gas atmosphere when the thickness was 3.6 nm. In terms of resistivity obtained at 20K, it increased with the thinner films including the dispersion

of the measured data. We observed a maximum resistivity of 3.61 $\mu\Omega$m with 5.4-nm-thick thin film, where the T_c was 5.3K. The obtained resistivity was higher compared to that reported in other researches [18], [23], [24]. Although this could be caused by influence of the grain boundary and the crystallinity, it is still under investigation. With the 1.8 nm-thick NbTiN thin film, we obtained a very high resistivity of 16.2 $\mu\Omega$m and a small residual resistance ratio *RRR* (R_{300K}/R_{20K}) of 0.54. These values are markedly different from those of the thicker films. Therefore, there could be the dead layer of around 2 nm.

In this study, we selected a 5.4-nm-thick NbTiN thin film for the operation simulation of the nTron in Sect. 3 due to the high resistivity. For a J_c of 5×10^6 A/cm^2, film thickness of 5.4 nm, and choke width of 50 nm, the critical current of the choke, I_c^{choke}, is about 14 μA. Then, the superconductive state of the choke can be broken down by the input current of several tens μA obtained from the SFQ circuits.

The normal resistance of the nTron R_n and the supplied bias current I_b are calculated to 13 kΩ and 97 μA ($I_b = 0.9\ I_c$), respectively, under the condition that the channel width, the length of the resistive area, and J_c in the channel were 100 nm, 2 μm, and 2×10^7 A/cm^2, respectively.

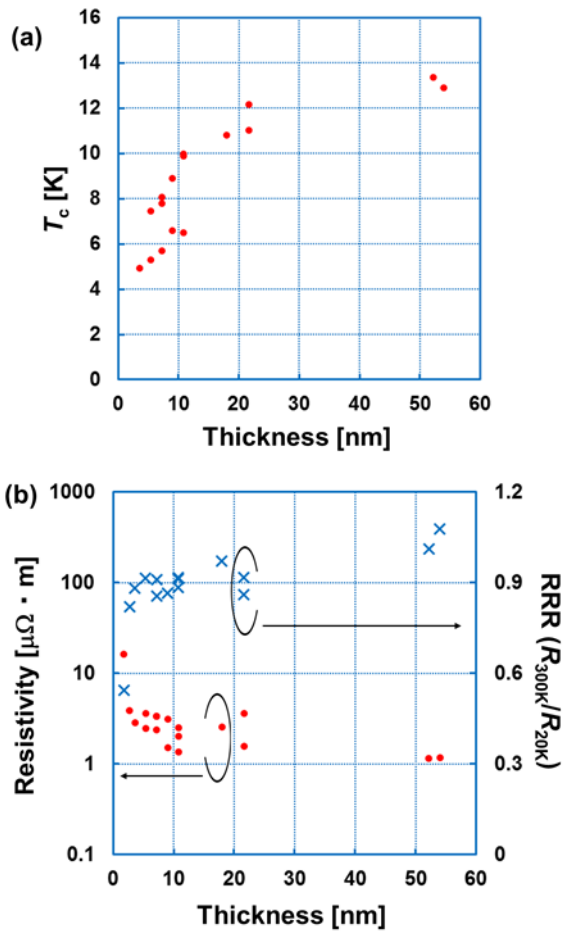


Fig. 2 The thickness dependencies of the niobium titanium nitride (NbTiN) thin films: (a) T_c and (b) the resistivity obtained at 20K and RRR.

3. HSPICE Simulation of the nTron and a CMOS Memory Cell

3.1 Electric Circuit Model of an nTron

To build a hybrid memory system, the HSPICE simulation must include Josephson, thermally assisted, and CMOS devices. Therefore, we proposed an electrical model of the nTrons considering the effect of thermal diffusion. Figure 3 (a) shows a schematic of the proposed model.

The transition between superconduction and normal conduction can be represented by using a lead wire with a switch (S_1) and R_n, where they are connected in parallel. The generation of the hotspot at the choke takes a few picoseconds so that the nTron can transit to the normal state rapidly, while the thermal diffusion to the substrate after the transition to the normal state will take several nanoseconds. As the resistive area of the nTron changes with time, the model must incorporate the thermal diffusion effect. Therefore, we proposed an electrical circuit model by adding another inductance $L_{k'}$ connected in parallel to R_n with switch

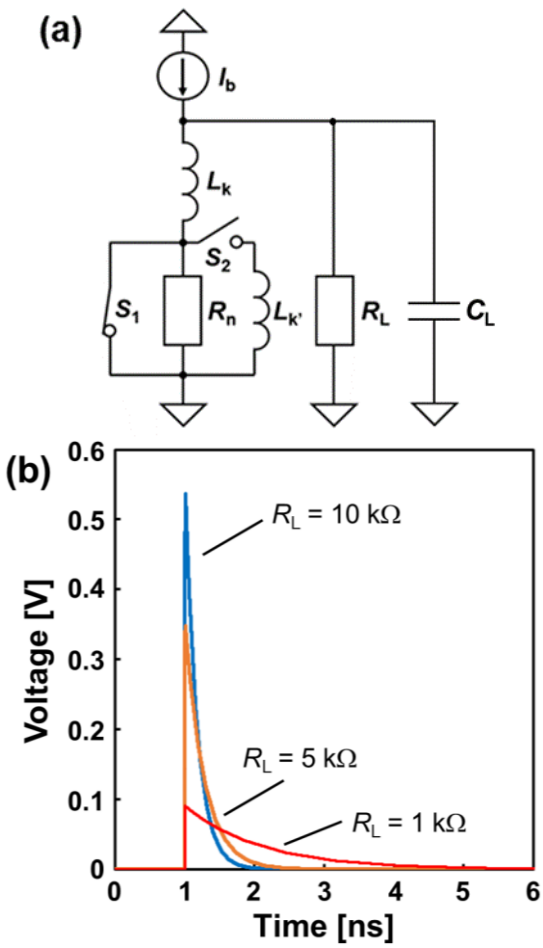


Fig. 3 Electrical model of an nTron. $I_b = 97\ \mu$A, $L_k = 5$ nH, $L_{k'} = 1\ \mu$H, $R_n = 13$ kΩ, $R_L = 1, 5, 10$ kΩ, $C_L = 0.43$ fF. (a) Schematic of the electrical model. (b) An example of the simulation results.

S_2, as shown in Fig. 3 (a), since it is difficult to represent the change of resistance with time in HSPICE simulators.

In the initial (superconducting) state, switch S_1 is closed, S_2 is open, and the supplied bias current I_b flows through the inductance of channel L_k and the lead wire. When switch S_1 opens, S_2 closes a few picoseconds later, where the delay corresponds to the pulse width of the SFQ. Then, the output voltage simulating the output signal from the nTron is obtained at load resistance R_L. In this case, the output voltage rises quickly based on the time constant $L_k/(R_n + R_L)$, when the nTron returns to the normal state. To cause the nTron to turn to the superconducting state, a large voltage is immediately generated in $L_{k'}$ by closing S_2. The voltage generated in $L_{k'}$ corresponds to the difference in temperature between the nTron and the substrate according based on the analogy of the electrical and thermal circuits. The gradual current flowing to $L_{k'}$ corresponds to the thermal diffusion to the substrate and the output voltage observed at R_L falls slowly with the value of $L_{k'}$. This model is not designed to perform in latching mode [19] yet, where the resistive domain is sustained, because the input of SFQ pulses rapidly return to zero and nTron can be cooled down.

In the measurement described in Sect. 4, we supply the bias current to nTron using voltage supply through a load resistance R_L. In this work, we simulated the output voltage from the nTron with changing the value of R_L in order to obtain sufficient output voltage for driving nMOS transistors. We connected the load capacitance C_L of the gate in the CMOS memory cell in parallel to the nTron as shown in Fig. 3 (a). The parameters of the nTrons are based on the experimentally extracted characteristics of the NbTiN thin film. Figure 3 (b) shows an example of the simulation results using HSPICE under the conditions. We changed the value of R_L up to 10 kΩ, where the value of 10 kΩ is comparable to the value of R_n, because the nTrons can enter the latching mode when the R_L is higher. As shown in Fig. 3 (b), we obtained an output voltage exceeding 0.5 V with R_L of 10 kΩ. As we could not experimentally confirmed the dynamic characteristic of nTrons yet, the value of $L_{k'}$ was set to 1 μH in order to achieve the reported operation speed around several gigahertz. From this simulation result, we decided to adopt R_L of 10 kΩ for our measurement described in Sect. 4. We should examine the validity of the value of $L_{k'}$ by evaluation of dynamic characteristic of the nTron. Additionally, we need to study on the appropriate I_c and output voltage of the nTrons because the effect depending on the relationship of I_c^{gate} and $I_c^{channel}$ is not taken into consideration in this model yet.

3.2 Simulation of the Readout from a Memory Cell

We connected the proposed model with a CMOS eight-transistor, static random access memory (SRAM) cell and tested the readout operation of the memory cell in the HSPICE simulation of our Josephson-CMOS hybrid memory system [17]. We used the same circuit parameters as used in Sect. 3.1 for the nTron model. Therefore, the normal

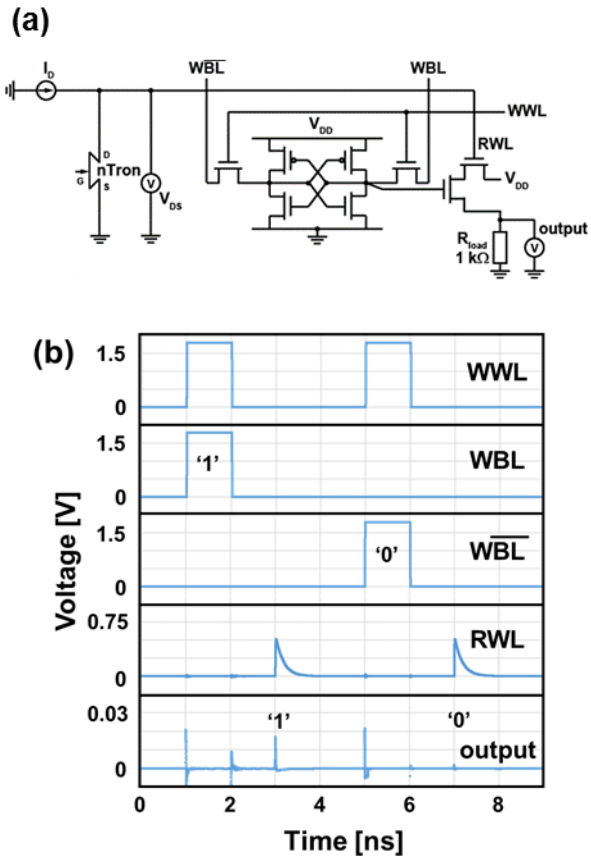


Fig. 4 Readout of the data written in complementary metal oxide semiconductor (CMOS) memory (HSPICE). (a) Schematic of the nTron and 8T-SRAM cell. (b) An example of the simulation results.

resistance of the nTron was set to 13 kΩ. The parameters of the CMOS memory cell were the same as those operated successfully in Yokohama National University, which are based on the Rohm 0.18 μm CMOS process.

Figure 4 (a) shows a schematic in which both circuits are connected. In the operation of the SRAM cell, the values "1" or "0" are written in the memory cell by feeding HIGHs into write bit line (WBL) or write bit line bar ($\overline{\text{WBL}}$) when HIGHs are fed into write word line (WWL), and the written data are read out by feeding HIGHs into read word line (RWL). Here, the written data can be read out when the nTron turns to the normal state and an output voltage exceeding 0.4 V is obtained. This is because the path to the RWL is connected directly to the output of the nTron. The voltage heights for HIGHs and supply voltage V_{DD}, are set to 1.8 V. From the simulation results, the output voltage of 0.5 V from the nTron model was input to RWL, and an output voltage of 20 mV at the load resistance was obtained by applying the voltage to RWL with the inputs to WWL and WBL, as shown in Fig. 4 (b). This result showed that the nTron could drive the nMOS transistor and the written data are read out correctly. We also observed an unexpected noise signal when the signals were input to WWL. The through-current with the input to WWL is also observed

in the simulation of the CMOS memory cell itself. Therefore, this is not caused by the nTron model and the connection of the nTron and the CMOS memory cell.

4. Readout Test from the CMOS Memory Cell

We fabricated an NbTiN nTron and tested the readout from the CMOS memory cell using the nTron, as we confirmed that the nTron could drive the MOS transistor in the HSPICE simulation.

4.1 Fabrication of NbTiN nTrons

In this paper, we argues that thinner film is better for obtaining large output voltage. However, the thicker films can be suitable for obtaining large current for rapidly charging capacitance in the CMOS transistors, and be one choice depending on application field. On the other hand, we are still optimizing the exposure of the electron beam to form narrow patterns for ultra-thin film. So far, we have successfully fabricated only 50-nm thick NbTiN nTrons. Although we evaluated only preliminary characteristics of the nTrons in previous study [17], we evaluated the I–V characteristics and output voltages of the nTrons in detail, and tested the readout from a CMOS memory cell for driving MOS transistors.

We deposited a 50-nm-thick NbTiN film on a thermally oxidized silicon substrate by DC magnetron sputtering, and patterned it using electron-beam lithography (EBL) and reactive ion etching (RIE). The electron beam was accelerated with a voltage of 50 kV, and the dose time and beam currents were set to 0.25 μs/cm^2 and 5.0×10^{-11} A, respectively. Figure 5 shows optical and scanning electron microscope (SEM) images of the fabricated nTrons. The widths of the choke and channel of the nTron were 0.22 μm and 0.28 μm, respectively. These were wider than the designed values (0.1 μm and 0.2 μm), and this was due to scattering of the electron beam when the nTron pattern was formed.

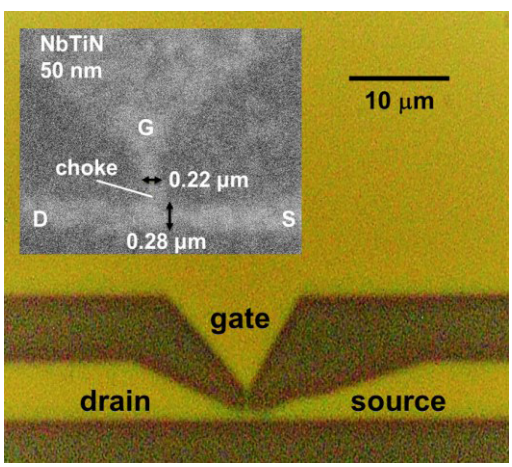


Fig. 5 Optical and scanning electron microscope (inset) images of the fabricated NbTiN nTrons.

4.2 Static Characteristics of the Fabricated NbTiN nTrons

First, we measured the resistance–temperature characteristics of the NbTiN nTron in a helium atmosphere. From the results, we evaluated the critical temperature, $T_c^{D\text{-}S}$, of the nTron between the drain and source and found that $T_c^{D\text{-}S}$ was 12.7K. We did not observe a normal transition due to the thermal effect because of the large I_c at the temperature of liquid helium (4.2K). Next, we measured the I–V characteristics of the nTron between the drain and source at 11K, where the drain current was supplied through a load resistance of 10 kΩ. Figure 6 shows the obtained I–V characteristics with changing values of I_{gate}. We successfully observed output voltages of up to several hundred millivolts when the nTron was in the normal state. Load lines were drawn, as shown in Fig. 6. We confirmed that the I_c between the drain and source ($I_c^{D\text{-}S}$) without I_{gate} was 160 μA and $I_c^{D\text{-}S}$ decreased with the input I_{gate} over the critical current of I_{gate} (90 μA). The shift in the I–V curves were not simply caused by input of I_{gate}. It is thought that this was caused by the thermal effect of the nTron. An output of approximately 200 mV is expected when we supply I_{drain} = 150 μA and I_{gate} = 100 μA. Although we obtained a high output voltage of sub-V, it was insufficient for driving an nMOS transistor for the readout in the SRAM cell when we used only the expected thermal effect of the nTron. However, the nMOS transistor could be driven by inputting a greater input current to the drain. In this case, the nTron did not operate in the expected mode. The nTron operated using not only primary thermal effect by supplying I_{gate} but also the heat caused by channel because the I_{drain} was supplied over $I_c^{channel}$ in this mode. Therefore, smaller nTrons are required to obtain higher sensitivity for I_{gate} and larger resistivity for driving nMOS transistors in expected thermal effect mode.

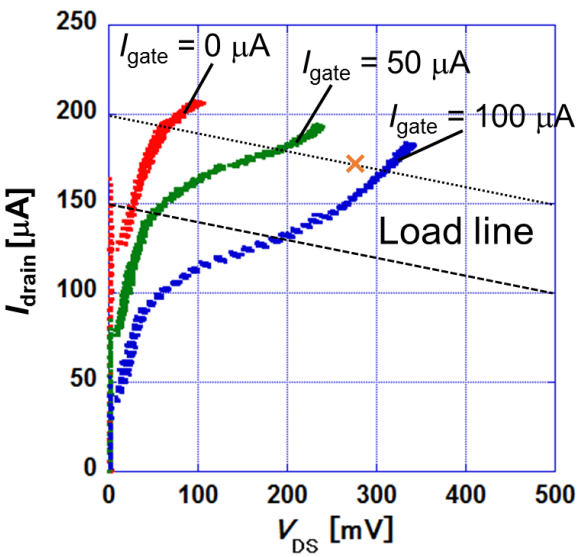


Fig. 6 Current–voltage (I–V) characteristics of the drain and source in the fabricated nTron measured with a load resistance of 10 kΩ.

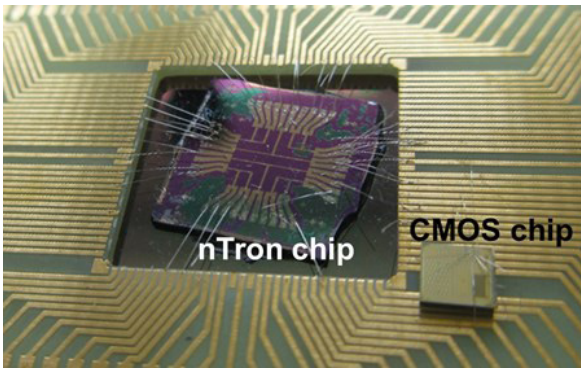


Fig. 7 An nTron chip and CMOS chip.

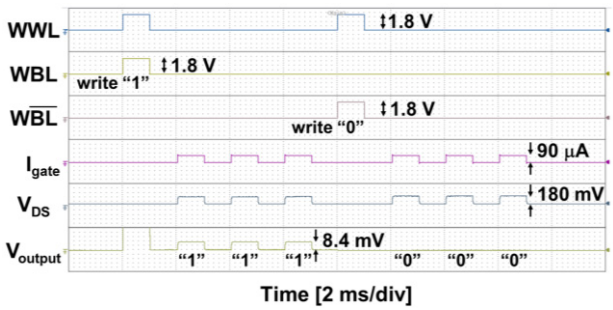


Fig. 8 An example of the test results for readout from CMOS memory using the fabricated nTron.

4.3 Readout Test Using the Fabricated NbTiN nTrons

We tested the data readout from the SRAM cell using the fabricated nTron in the same way as described in Sect. 3.2. The nTron and the SRAM cell on the separate chip were connected electrically by using Al bonding wires, as shown in Fig. 7. The signals to WWL, WBL, and $\overline{\text{WBL}}$ were input by a pulse pattern generator operating at room temperature, where the voltage heights were 1.8 V, and the supply voltage V_{DD} was set to 1.8 V.

In this measurement, we supplied $I_{drain} = 200\,\mu$A to obtain a sufficient output voltage from the nTrons and evaluated the output voltage from the CMOS memory cell on changing I_{gate}. Figure 8 shows an example of the readout test results. We observed a voltage exceeding 200 mV, which includes the offset voltage of 50 mV, between the drain and source of the nTron (V_{DS}) triggered by an input of $I_{gate} = 90\,\mu$A. This result agrees with the obtained I_{DS}–V_{DS} characteristic of the nTron as shown by a cross mark on the load line in Fig. 6. This means that the nTron adopted the normal state on input I_{gate}. We also observed that the values "1" and "0" were correctly read out when a current of I_{gate} was supplied to the nTron. This showed the potential of NbTiN-based thermally assisted superconductor transistors for Josephson-CMOS hybrid memories.

5. Conclusion

To build a Josephson–CMOS hybrid memory system, we investigated the characteristics of the NbTiN thin film deposited on thermally oxidized silicon, and obtained good characteristics for the nTron, with a low critical temperature of 5.3K and a high resistivity of 3.61 $\mu\Omega$m with 5.4-nm-thick NbTiN thin films. The 5.4-nm-thick NbTiN nTrons can achieve the high output resistance of 13 kΩ.

We also proposed an electrical circuit model of the thermally assisted transistors and confirmed that the nTron could drive MOS transistors in an HSPICE simulation. We fabricated NbTiN nTrons and successfully read out the data written in a CMOS memory cell driven by the NbTiN nTrons.

From these results, we confirmed the basic operation of NbTiN nTron for driving CMOS memory cells in both the simulation and experimental studied. It will be expected to build highly integrated Josephson–CMOS hybrid memory systems by using NbTiN nTrons because the Nb-based SFQ circuits, the NbTiN nTrons, and MOS transistors can be integrated on the same substrate. In this work, the fabricated nTrons were larger than expected and did not operate in expected mode. Therefore, we need to optimize the exposure of the electron beam to form narrow patterns.

Acknowledgments

The authors would like to thank Hiroyuki Akaike of Daido Univ. for his effort on the preparation of NbTiN films.

This work was supported by JSPS KAKENHI Grant Numbers JP26220904, JP16H02340, and JST-ALCA. This work was supported in part by VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Cadence Design Systems, Inc. and Synopsis, Inc. The CMOS chip in this study was fabricated in chip fabrication program of VDEC in collaboration with Rohm Corporation and Toppan Printing Corporation.

References

[1] K.K. Likharev and V.K. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," IEEE Trans. Appl. Supercond., vol.1, no.1, pp.3–28, March 1991.

[2] Y. Yamanashi, M. Tanaka, A. Akimoto, H. Park, Y. Kamiya, N. Irie, N. Yoshikawa, A. Fujimaki, H. Terai, and Y. Hashimoto, "Design and Implementation of a Pipelined Bit-Serial SFQ Microprocessor, CORE1β," IEEE Trans. Appl. Supercond., vol.17, no.2, pp.474–477, June 2007.

[3] A. Fujimaki, M. Tanaka, R. Kasagi, K. Takagi, M. Okada, Y. Hayakawa, K. Takata, H. Akaike, N. Yoshikawa, S. Nagasawa, K. Takagi, and N. Takagi, "Large-scale integrated circuit design based on a Nb nine-layer structure for reconfigurable data-path processors," IEICE Trans. Electron., vol.E97-C, no.3, pp.157–165, March 2014.

[4] X. Peng, Q. Xu, T. Kato, Y. Yamanashi, N. Yoshikawa, A. Fujimaki, N. Takagi, K. Takagi, and M. Hidaka, "High-Speed Demonstration of Bit-Serial Floating-Point Adders and Multipliers Using Single-Flux-Quantum Circuits," IEEE Trans. Appl. Supercond., vol.25, no.3, p.1301106, June 2015.

[5] A. Fujimaki, R. Sato, Y. Hatanaka, Y. Matsui, K. Takagi, N. Takagi, and M. Tanaka, "Execution of stored programs in a single-flux quantum microprocessor with embeded memories at 50 GHz," 13th Eu-

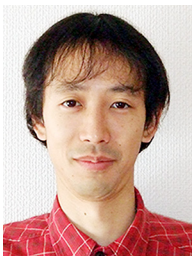
ropean Conference on Applied Superconductivity (EUCAS 2017), Geneva, Switzerland, Sept. 2017.
[6] K. Ishida, M. Tanaka, T. Ono, and K. Inoue, "Towards Ultra High-Speed Cryogenic Single-Flux-Quantum Computing," submitted to IEICE Trans. Electron.
[7] U. Ghoshal, H. Kroger, and T. Van Duzar, "Superconductor-semiconductor memories," IEEE Trans. Appl. Supercond., vol.3, no.1, pp.2315–2318, March 1993.
[8] I.V. Vernik, V.V. Bol'ginov, S.V. Bakurskiy, A.A. Golubov, M.Y. Kupriyanov, V.V. Ryazanov, and O.A. Mukhanov, "Magnetic Josephson Junctions with Superconducting Interlayer for Cryogenic Memory," IEEE Trans. Appl. Supercond., vol.23, no.3, p.1701208, June 2013.
[9] J.W.A. Robinson, J.D.S. Witt, and M.G. Blamire, "Controlled Injection of Spin-Triplet Supercurrents into a Strong Ferromagnet," Science, vol.329, no.5987, pp.59–61, July 2010.
[10] Q. Liu, T. VanDuzer, X. Meng, S.R. Whiteley, K. Fujiwara, T. Tomida, K. Tokuda, and N. Yoshikawa, "Simulation and measurements on a 64-kbit hybrid Josephson-CMOS memory," IEEE Trans. Appl. Supercond., vol.15, no.2, pp.415–418, June 2005.
[11] N. Yoshikawa, M. Tokuda, T. Tomida, H. Kojima, K. Fujiwara, Q. Liu, and T.V. Duzer, "Access time measurement of Josephson-CMOS hybrid memory using single-flux-quantum circuits," Supercond. Sci. Technol., vol.19, no.5, pp.S350–S353, May 2006.
[12] T.V. Duzer, L. Zheng, S.R. Whiteley, H. Kim, J. Kim, X. Meng, and T. Ortlepp, "64-kb hybrid Josephson-CMOS 4 kelvin RAM with 400 ps access time and 12 mW read power," IEEE Trans. Appl. Supercond., vol.23, no.3, p.1700504, June 2013.
[13] G. Konno, Y. Yamanashi, and N. Yoshikawa, "Fully-Functional Operation of Low-Power 64-kb Josephson-CMOS Hybrid Memories," IEEE Trans. Appl. Supercond., vol.27, no.4, p.1300607, June 2017.
[14] O.A. Mukhanov, S.V. Rylov, D.V. Gaidarenko, N.B. Dubash, and V.V. Borzenets, "Josephson output interfaces for RSFQ circuits," IEEE Trans. Appl. Supercond., vol.7, no.2, pp.2826–2831, June 1997.
[15] H. Suzuki, A. Inoue, T. Imamura, and S. Hasuo, "A Josephson driver to interface Josephson junctions to semiconductor transistors," Technical Digest., Int. Electron Devices Meeting, pp.290–293, Dec. 1988.
[16] A.N. McCaughan and K.K. Berggren, "A superconducting-nanowire three-terminal electrothermal device," Nano Lett., vol.14, no.10, pp.5748–5753, Sept. 2014.
[17] M. Tanaka, M. Suzuki, G. Konno, Y. Ito, A. Fujimaki, and N. Yoshikawa, "Josephson-CMOS Hybrid Memory With Nanocryotrons," IEEE Trans. Appl. Supercond., vol.27, no.4, p.1800904, June 2017.
[18] K. Makise, H. Terai, M. Takeda, Y. Uzawa, and Z. Wang, "Characterization of NbTiN Thin Films Deposited on Various Substrates," IEEE Trans. Appl. Supercond., vol.21, no.3, pp.139–142, June 2011.
[19] Q.-Y. Zhao, A.N. McCaughan, A.E. Dane, K.K. Bergren, and T. Ortlepp, "A nanoCryotron comparator can connect single-flux-quantum circuits to conventional electronics," Supercond. Sci. Technol., vol.30, no.4, p.044002, March 2017.
[20] G.N. Gol'tsman, O. Okunev, G. Chulkova, A. Lipatov, A. Semenov, K. Smirnov, B. Voronov, A. Dzardanov, C. Williams, and R. Sobolewski, "Picosecond superconducting single-photon optical detector," Appl. Phys. Lett., vol.79, no.6, pp.705–707, Aug. 2001.
[21] T. Yamashita, S. Miki, K. Makise, W. Qiu, H. Terai, M. Fujiwara, M. Sasaki, and Z. Wang, "Origin of intrinsic dark count in superconducting nanowire single-photon detectors," Appl. Phys. Lett., vol.99, no.16, p.161105, Oct. 2011.
[22] S. Nagasawa, K. Hinode, T. Satoh, M. Hidaka, H. Akaike, A. Fujimaki, N. Yoshikawa, K. Takagi, and N. Takagi, "Nb 9-layer fabrication process for superconducting large-scale SFQ circuits and its process evaluation," IEICE Trans. Electron., vol.E97-C, no.3, pp.132–140, March 2014.
[23] T. Shiino, S. Shiba, N. Sakai, T. Yamakura, L. Jiang, Y. Uzawa, H. Maezawa, and S. Yamamoto, "Improvement of the critical temperature of superconducting NbTiN and NbN thin films using the AlN buffer layer," Supercond. Sci. Technol., vol.23, no.4, p.045004, March 2010.
[24] L. Zhang, W. Peng, L.X. You, and Z. Wang, "Superconducting properties and chemical composition of NbTiN thin films with different thickness," Appl. Phys. Lett., vol.107, no.12, p.122603, Sept. 2015.

Kyosuke Sano received the B.E., M.E., and Ph.D. degrees in Electrical and computer Engineering from Yokohama National University, in 2012, 2014, and 2017, respectively. He was a JSPS Research Fellow from 2015 to 2017. He joined Graduate School of Engineering, Nagoya University in 2017, where he is currently a designated assistant professor. His current research interests include superconducting devices such as thermally assisted nano-structured devices and RSFQ circuits He is a member of the Japan Society of Applied Physics.

Masato Suzuki received the B.E. degree in Electronics from Nagoya University, in 2016. He has been engaged in the research and development of superconducting devices. He is a member of the Japan Society of Applied Physics. He is currently with Nagoya University.

Kohei Maruyama received the B.E. degree in Electronics from Nagoya University, in 2017. He has been engaged in the research and development of superconducting devices. He is a member of the Japan Society of Applied Physics. He is currently with Nagoya University.

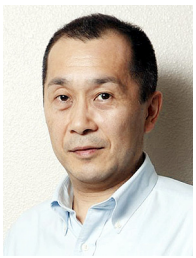
Soya Taniguchi received the B.E. and M.E. degrees in Electronics from Nagoya University, in 2013 and 2015, respectively. He is a JSPS Research Fellow from 2016. His current research interests include superconducting digital circuits with ferromagnetic materials. He is a member of the Japan Society of Applied Physics.



Masamitsu Tanaka received the M.E. and Ph.D. degrees in electronics and information electronics from Nagoya University, Nagoya, Japan, in 2003 and 2006, respectively. He was a JSPS Research Fellow from 2005 to 2007. He joined Graduate School of Information Science, Nagoya University in 2007, and moved to Graduate School of Engineering in 2010, where he is currently an assistant professor. In 2011 he was a research scholar at the University of California, Berkeley, CA, USA. He has been also a research associate at VLSI Design and Education Center, the University of Tokyo since 2013. His research interests include the ultra-fast/energy-efficient computing using RSFQ circuits and logic design methodologies. He is a member of the IEICE, IEEE, Japan Society of Applied Physics, Cryogenics and Superconductivity Society of Japan, and Institute of Electrical Engineers of Japan.

Akira Fujimaki received his B.E, M.E., and Dr.Eng. degrees from Tohoku University in 1982, 1984, and 1987, respectively. He was a Visiting Assistant Research Engineer at the University of California, Berkeley, in 1987. Since 1988, he has been working on superconductor devices and circuits at the School of Engineering, Nagoya University, Nagoya, Japan, where he is currently a professor. His current research interests include single-flux-quantum circuits and their applications based on low- and high-temperature superconductors. He is a member of the IEICE, IEEE, Japan Society of Applied Physics, Cryogenics and Superconductivity Society of Japan, and Institute of Electrical Engineers of Japan.

Masumi Inoue received the B.E., M.E., and Ph.D. degrees from Nagoya University, Japan, in 1983, 1985, and 1988, respectively. He joined Nagoya University as a research associate in 1988. Since 1988, he has been working on superconductor devices. In 2013, he moved to Meijo University, Japan, where he is currently a professor. His research interests include superconductive electronics, wireless power transmission, and energy harvesting devices. He is a member of the Institute of Electronics, Information and Communication Engineers, the Japan Society of Applied Physics, the Institute of Electrical Engineers of Japan, the Society of Polymer Science, Japan, and Materials Research Society.



Nobuyuki Yoshikawa received the B.E., M.E., and Ph.D. degrees in electrical and computer engineering from Yokohama National University, Japan, in 1984, 1986, and 1989, respectively. Since 1989, he has been with the Department of Electrical and Computer Engineering, Yokohama National University, where he is currently a Professor. His research interests include superconductive devices and their application in digital and analog circuits. He is also interested in single-electron-tunneling devices, quantum computing devices and cryo-CMOS devices. Prof. Yoshikawa is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Japan Society of Applied Physics, the Institute of Electrical Engineering of Japan, and Cryogenics and Superconductivity Society of Japan.