FOREWORD

Special Section on Analog Circuits and Their Application Technologies

The concept of IoT (Internet of Things) can be recognized as a technology to build a super smart society enabled with over 1 trillion sensors connected to the internet, and it becomes fundamental in the current and future information and communication systems along with AI. The total market of IoT is expected over 5 trillion dollars in 2035, and its economical ripple effect has strong impacts to IC industries especially in analog products for sensing, such as amplifiers, filters, and AD converters (ADC), and wireless/wireline communications. The productization of current systems including steps of PoC (proof of concept) and PoB (proof of Business) strongly demands the short TAT (turn-around-time) development for electronics systems, and consequently, design approach using off-the-shelf devices is becoming more important. By taking account of this technology trend, the editorial committee has changed the title of the special section from "Analog Circuits and Related SoC Integration" to "Analog Circuits and Their Application Technologies" to encourage submissions designed by various application-oriented approaches including the off-the-shelf designs.

Here, we are happy to publish this special section illustrating analog circuit innovations in the fields of IoT, medical/bioelectronics and high-speed wireless communications. This year's special section includes two invited papers and five submitted papers. The first invited paper, entitled "A Unified Analysis of the Signal Transfer Characteristics of a Single-Path FET-R-C Circuit," discusses a unified analysis method for circuits consisting of FET-R-C, which can be sample-and-hold, passive mixer, band-pass filter, band-pass impedance, etc. The second invited paper, entitled "Column-Parallel ADCs for CMOS Image Sensors and Their FoM-Based Evaluations," illustrates the technology evolution of column-parallel ADCs commonly used in CMOS image sensor. The author presents an insightful analysis based on FoM, which is helpful for understanding ADC performance trade-offs.

The five submitted papers present various aspects in analog circuit design. The four regular papers include subjects of a 1024-QAM OFDM signal capable WLAN receiver with IQ mismatch self-calibration technique, an LNA-less 300 GHz CMOS receiver, a low power Code-Modulated Synchronized-OOK transmitter for normally-off wireless sensor networks and a 3rd-order noise coupled $\Delta\Sigma$AD modulator with a passive adder embedded noise shaping SAR quantizer. One brief paper presents a top-down design methodology to optimize resonant capacitance in a wireless power transfer system for 3-D stacked multiple receivers.

On behalf of the editorial committee of this special section, I would like to express our sincere appreciation to all the authors of the submitted papers. I would also like to thank all the reviewers and all the committee members of this special section for their important contributions to the editorial work. Finally, I would like to thank Dr. Yasumoto Tomita and professor Kiichi Niitsu for their extensive work as guest editors.

Guest Editors:
Yasumoto Tomita (Fujitsu Lab.), Kiichi Niitsu (Nagoya Univ.)

Kenichi Okada (Tokyo Institute of Technology), Guest Editor-in-Chief

Kenichi Okada *(Senior Member)* received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively. From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science with Kyoto University. From 2003 to 2007, he was an Assistant Professor with the Precision and Intelligence Laboratory, Tokyo Institute of Technology, Tokyo, Japan, where he has been an Associate Professor with the Department of Physical Electronics since 2007. He has authored or co-authored over 300 journal and conference papers. His current research interests include millimeter-wave CMOS wireless transceiver, digital phase-locked loop, 5G mobile system, and ultralow power RF circuits. Dr. Okada is a member of the Institute of Electronics, Information and Communication Engineers, the Information Processing Society of Japan, and the Japan Society of Applied Physics. He received the Ericsson Young Scientist Award in 2004, the A-SSCC Outstanding Design Award in 2006 and 2011, the ASP-DAC Special Feature Award in 2011 and the Best Design Award in 2014, 2015 and 2017, JSPS Prize in 2014, Suematsu Yasuharu Award in 2015, the MEXT Prizes for Science and Technology in 2017, and 38 other international and domestic awards. He is/was a member of the technical program committees of ISSCC, VLSI Circuits, and ESSCIRC, and serves as an Associate Editor of IEEE Journal of Solid-State Circuits.