PAPER

A Transformer Noise-Canceling Ultra-Wideband CMOS Low-Noise Amplifier

Takao KIHARA[†a)], ***Nonmember***, **Toshimasa MATSUOKA**[†], ***and*** **Kenji TANIGUCHI**[†], ***Members***

SUMMARY Previously reported wideband CMOS low-noise amplifiers (LNAs) have difficulty in achieving both wideband input impedance matching and low noise performance at low power consumption and low supply voltage. We present a transformer noise-canceling wideband CMOS LNA based on a common-gate topology. The transformer, composed of the input and shunt-peaking inductors, partly cancels the noise originating from the common-gate transistor and load resistor. The combination of the transformer with an output series inductor provides wideband input impedance matching. The LNA designed for ultra-wideband (UWB) applications is implemented in a 90 nm digital CMOS process. It occupies 0.12 mm^2 and achieves $|S_{11}| < -10$ dB, $NF < 4.4$ dB, and $|S_{21}| > 9.3$ dB across 3.1–10.6 GHz with a power consumption of 2.5 mW from a 1.0 V supply. These results show that the proposed topology is the most suitable for low-power and low-voltage UWB CMOS LNAs.

key words: *CMOS, low-noise amplifier (LNA), noise cancellation, ultra-wideband (UWB), transformer*

1. Introduction

Ultra-wideband (UWB) technology has attracted much interest in recent years, because of its ability to realize high-speed wireless personal area networks (WPANs), in which electronic devices are required to transfer large amounts of data, such as audio or video files, at a high data transfer rate. UWB frequency bands assigned from 3.1 to 10.6 GHz are utilized by two different communication systems: multiband orthogonal frequency division multiplexing (MB-OFDM) UWB [1] or single-carrier direct sequence (DS) UWB [2]. The MB-OFDM UWB system using 14 sub-bands, each with a bandwidth of 528 MHz, transmits signals modulated by OFDM in the subband. The data rate is up to 480 Mbps. The DS-UWB system spreads the spectrum over the low band (3.1–4.85 GHz) or high band (6.2–9.7 GHz), and provides a maximum data rate of 1320 Mbps. In either case, wideband low-noise amplifiers (LNAs) are essential for the RF front-ends of UWB receivers.

The UWB LNA must meet several stringent requirements: input impedance matching, low noise performance, and sufficient gain across 3.1–10.6 GHz at low power consumption, a low supply voltage, and low cost (i.e., small area and requiring no additional layers). In addition, it is desirable to implement the LNA with digital CMOS technologies for the integration of RF front-ends and digital circuits. Although several wideband CMOS LNAs have been proposed in recent years, none of them have simultaneously met all these requirements. An LNA with wideband LC matching networks [3] consumes a large chip area. Although resistive-feedback LNAs [4]–[6] and common-drain feedback LNAs [7], [8] occupy small chip areas, they require high power consumption and high supply voltages to simultaneously achieve wideband input impedance matching and low noise performance. A reactive-feedback LNA [9], [10] demands two thick metal layers to form a transformer that provides a reactive feedback. Noise-canceling LNAs [11]–[14] require additional circuits and power consumption. Distributed LNAs [15], [16] consume much higher power and larger areas than other LNAs.

In this paper, we propose a transformer noise-canceling common-gate LNA employing an output series inductor [17]. The proposed LNA is suitable for low-power and low-voltage operation, and achieves $|S_{11}| < -10$ dB, $NF < 4.4$ dB, and $|S_{21}| > 9.3$ dB across 3.1–10.6 GHz. This paper is organized as follows. Section 2 describes the proposed circuit topology and noise cancellation mechanisms. The noise, input admittance, gain, stability, and group delay of the proposed LNA are analyzed in Sect. 3. Section 4 describes the design methodology for the LNA. Section 5 shows the measurements of the LNA implemented in a 90 nm digital CMOS process, and Sect. 6 concludes the paper.

2. Transformer Noise-Canceling LNA

This section presents the circuit topology of the transformer noise-canceling CMOS LNA and the noise cancellation mechanisms.

2.1 Circuit Topology

Figure 1 shows a schematic of the proposed LNA, based on a common-gate (CG) LNA with a shunt-peaking inductor. The CG topology is suitable for low-voltage operation, because it does not require a cascode transistor to alleviate the Miller effect from the CG transistor M_1 [18]. The main difference between the proposed LNA and the CG LNA is that the input and shunt-peaking inductors, L_p and L_s, are magnetically coupled to form a transformer. A similar topology has been reported for narrowband applications [19]. The transformer cancels the noise produced by M_1 and the load resistor R_L, thereby improving the noise performance with-

Manuscript received May 2, 2009.
Manuscript revised August 30, 2009.

[†]The authors are with the Division of Electrical, Electronics and Information Engineering, Graduate School of Engineering, Osaka University, Suita-shi, 565-0871 Japan.
a) E-mail: kihara@si.eei.eng.osaka-u.ac.jp

DOI: 10.1587/transele.E93.C.187

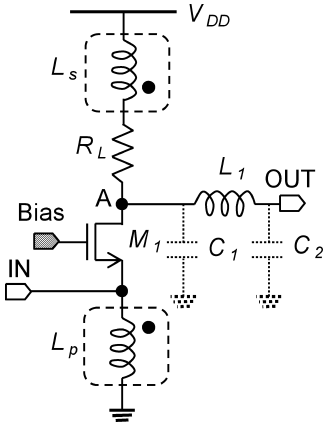


Fig. 1 Schematic of the proposed LNA.

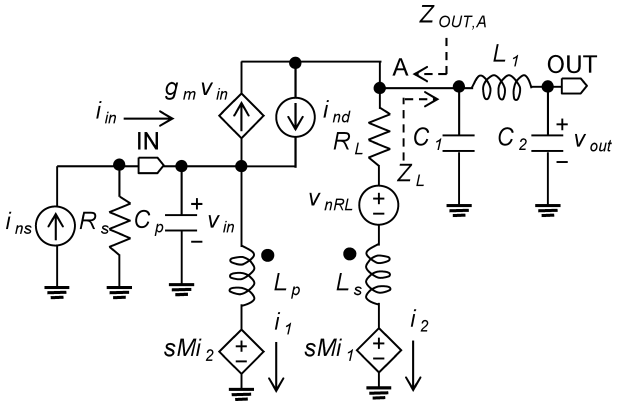


Fig. 2 Small-signal equivalent circuit with noise sources.

out additional circuits or increased power consumption. The transformer also provides a positive feedback, whose mechanism is as follows: An output current generated by a signal voltage flows through L_s, which induces a voltage that is in phase with the signal voltage to L_p. The output series inductor L_1 forms a π network with the parasitic capacitances, C_1 and C_2, extending not only the gain bandwidth, but also the input bandwidth, which is defined as the frequency range of $|S_{11}| < -10$ dB. The chip area of the proposed LNA is the same as that of a CG LNA with a shunt-peaking inductor, because L_p can be stacked on L_s, i.e., a stacked transformer, which occupies the area of one inductor.

2.2 Noise Cancellation

The transformer partly cancels the output noise originating from the CG transistor M_1 and load resistor R_L, thereby improving the LNA noise performance. The small-signal circuit of the proposed LNA is shown in Fig. 2, where the voltage supply terminal ($V_{\rm DD}$) is connected to the AC ground; the noise of the signal source resistance R_s, M_1, and R_L are represented by the noise current sources i_{ns}, i_{nd}, and noise voltage source v_{nR_L}, respectively; M, given by $k\sqrt{L_pL_s}$, is the mutual inductance of the transformer and k the magnetic coupling factor; C_p represents the sum of the gate-source capacitance of M_1 and the parasitic capacitances of the input pad and L_p; Z_L is the load impedance considering the right hand side of output node A. The mechanisms for the noise cancellation are conceptually illustrated in Figs. 3(a) and (b). The transformer detects noise currents flowing through the primary (or secondary) inductor L_p, inducing voltages correlated with the currents to the secondary (or primary) inductor L_s.

2.2.1 Transistor Noise Cancellation

The output noise voltage generated by i_{nd} is partly canceled by the induced noise voltage originating from i_{nd} flowing through L_p, as shown in Fig. 3(a). The noise current i_{nd} first flowing through L_s and R_L generates a noise voltage $v_{n1} = -i_{nd}(R_L + sL_s)$, and then a noise voltage $v'_{n1} = -i_{nd} \cdot sM$ is induced in L_p. Next, i_{nd} flows through L_p, producing a noise voltage $v_{n2} = i_{nd} \cdot sL_p$, which is canceled by v'_{n1}. Here, the transformer induces a noise voltage $v'_{n2} = i_{nd} \cdot sM$ in L_s. The induced noise voltage v'_{n2} is correlated and in antiphase with v_{n1} and hence the total output noise voltage is reduced: $-i_{nd}(R_L + sL_s - sM)$. The expression of the output noise voltage (at node A) including the effect of Z_L can be derived from Fig. 2:

$$v_{out,i_{nd}} = -i_{nd}Z_L \times \frac{n^2k^2 - nk + \left(\frac{1}{R_s} + sC_p + \frac{1}{sL_p}\right)\left(R_L + s(1-k^2)L_s\right)}{\left(\frac{1}{R_s} + Y_{IN}\right)\left(Z_L + R_L + s(1-k^2)L_s\right)}, \quad (1)$$

where $n = \sqrt{L_s/L_p}$ is the turn ratio of the transformer; $Y_{IN} = i_{in}/v_{in}$, described in the next section, is the input admittance of the LNA, and i_{in} and v_{in} are the input current and voltage, respectively, as shown in Fig. 2. The term of $s(1 - k^2)L_s$ in the numerator of Eq. (1) shows that the transistor noise is partly canceled by the transformer.

2.2.2 Load Resistor Noise Cancellation

The CG transistor M_1 drains a part of the output noise current originating from v_{nR_L}, reducing the output noise voltage, as shown in Fig. 3(b). The noise current due to v_{nR_L}, which is given by $v_{nR_L}/(sL_s + R_L + Z_L)$, first flows through L_s and then the transformer induces a noise voltage $v'_{nR_L} = -sMv_{nR_L}/(sL_s + R_L + Z_L)$ in L_p. The transistor M_1 detects a gate-source voltage $v_{gs} = v'_{nR_L}/sL_p(1/R_s + g_m + sC_p + 1/sL_p)$, and drains noise current of $g_m v_{gs}$ accordingly. This results in a reduction of the output noise current originating from v_{nR_L}. Considering the noise current due to M_1, we can obtain the output noise current flowing Z_L:

$$i_{out,v_{nR_L}} = \frac{\left(\frac{1}{R_s} + (1 - nk)g_m + sC_p + \frac{1}{sL_p}\right)v_{nR_L}}{\left(\frac{1}{R_s} + Y_{IN}\right)\left(Z_L + R_L + s(1 - k^2)L_s\right)}, \quad (2)$$

and the output noise voltage (at node A), $v_{out,v_{nR_L}}$, is given by $i_{out,v_{nR_L}}Z_L$. The term $-nkg_m$ in Eq. (2) originates from the

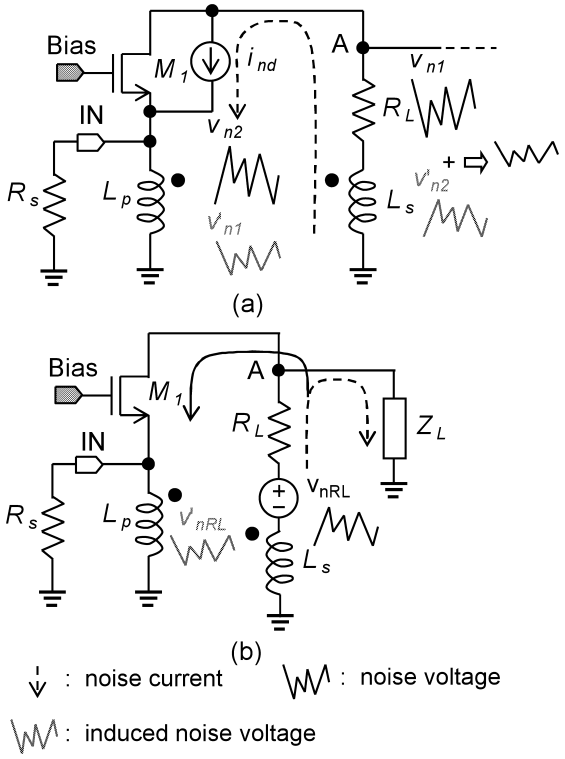


Fig. 3 Mechanisms for noise cancellation of (a) i_{nd} and (b) v_{nR_L}.

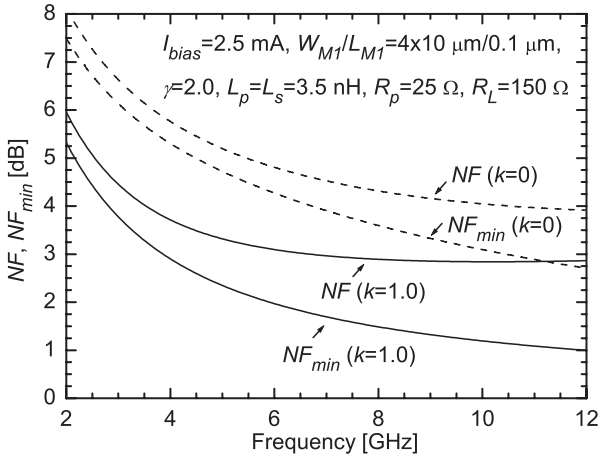


Fig. 4 Simulated NF and $NF_{\min}$ of the LNAs with and without noise cancellation ($k = 0, 1.0$).

noise cancellation.

2.2.3 Verification

The effectiveness of the transformer noise cancellation is verified through simulation. Figure 4 shows the simulated NF and $NF_{\min}$ of the proposed LNAs with and without the noise cancellation (i.e., $k = 0, 1.0$), where 90 nm CMOS process parameters are used and R_p represents the parasitic resistance of L_p. The LNA with $k = 0$ corresponds to a CG LNA with a load resistor and shunt-peaking inductor. The

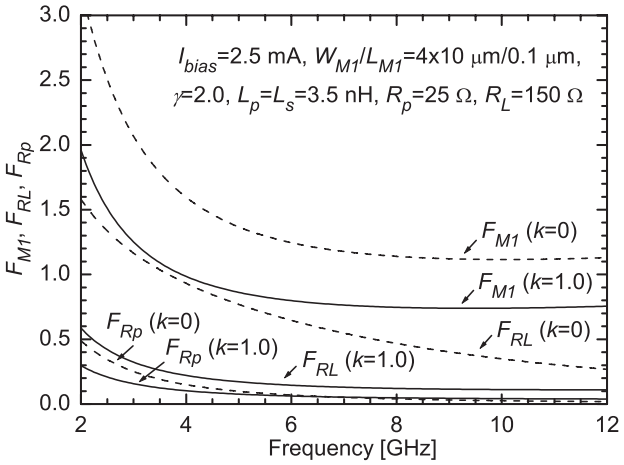


Fig. 5 Simulated noise contributions from M_1, R_L, and R_p to the LNAs with and without noise cancellation ($k = 0, 1.0$).

NF of the LNA with $k = 1.0$ is up to 2.2 dB lower than that of the LNA with $k = 0$. Figure 5 shows the simulated noise factors contributed from M_1, R_L, and R_p (F_{M_1}, F_{R_L}, and F_{R_p}, respectively) with and without the noise cancellation. The transformer reduces F_{M_1} by up to 35% and F_{R_L} by 65%. The contribution from R_p also slightly decreases and hence R_p contributes little to the overall NF (i.e., 0.1 dB in Fig. 4). The noise contributions from M_1 and R_L change with the turn ratio. A noise optimization procedure will be presented in the next section.

3. Circuit Analysis

The transformer improves the LNA noise performance at the cost of the input and gain bandwidths. The output series inductor L_1 extends both the bandwidths. In this section, the noise, input admittance, gain, stability, and group delay of the LNA are analyzed, and noise optimization and impedance matching procedures are presented.

3.1 Noise

The amount of noise cancellation is mainly determined by the turn ratio of the transformer. From the small-signal equivalent circuit shown in Fig. 2, the output noise voltage due to R_s is given by

$$v_{out,i_{ns}} = Z_L \frac{\left(g_m R_L + nk + s(1-k^2)L_s g_m\right) i_{ns}}{\left(\frac{1}{R_s} + Y_{IN}\right)\left(Z_L + R_L + s(1-k^2)L_s\right)}. \quad (3)$$

Using Eqs. (1)–(3), we obtain the noise factor of the proposed LNA:

$$F \approx 1 + F_{M_1} + F_{R_L}, \quad (4)$$

$$F_{M_1} = \left|\frac{v_{out,i_{nd}}}{v_{out,i_{ns}}}\right|^2$$

$$= \left| \frac{n^2 - n + \left(\frac{1}{R_s} + j\omega C_p + \frac{1}{j\omega L_p}\right) R_L}{g_m R_L + n} \right|^2 \gamma g_{d0} R_s, \quad (5)$$

$$F_{R_L} = \left| \frac{v_{out,v_{nR_L}}}{v_{out,i_{ns}}} \right|^2 = \left| \frac{(1-n)\, g_m R_L + \left(\frac{1}{R_s} + j\omega C_p + \frac{1}{j\omega L_p}\right) R_L}{g_m R_L + n} \right|^2 \frac{R_s}{R_L}, \quad (6)$$

where g_{d0} is the zero-bias drain conductance of M_1; the coefficient of channel thermal noise γ equals 2/3 in long-channel MOSFETs, but exceeds this value in short-channel MOSFETs [20]–[22]. The value of γ in a fabricated 90 nm MOSFET is approximately two, shown by the measured and simulated NF of the LNA, as will be shown in Sect. 5. For simplicity, the magnetic coupling factor k is assumed to be one. The parasitic resistance of L_p, the parasitic capacitance between L_p and L_s, and the induced-gate noise current of M_1 are ignored, because they do not have a significant effect on the overall NF. The transconductance g_m and load resistance R_L cannot be optimized for noise, because they are determined from input impedance matching conditions, as will be shown in the following subsection.

The optimum n for the noise performance can be obtained from Eqs. (4)–(6). Setting the derivatives of Eqs. (5) and (6) with respect to n to zero (i.e., $\partial F_{M_1}/\partial n = 0$ and $\partial F_{R_L}/\partial n = 0$ for $\omega = 1/\sqrt{L_p C_p}$), we can obtain

$$n_{opt,i_{nd}} = -g_m R_L + \sqrt{(g_m R_L)^2 + g_m R_L + \frac{R_L}{R_s}}, \quad (7)$$

$$n_{opt,v_{nR_L}} = 1 + \frac{1}{g_m R_s}, \quad (8)$$

for which a minimum F_{M_1} and F_{R_L} are achieved, respectively. Similarly, the optimum n for F, n_{opt}, can be obtained from $\partial F/\partial n = 0$:

$$\left(n_{opt}^2 - n_{opt} + \frac{R_L}{R_s}\right) \times \left(n_{opt}^2 + (2n_{opt} - 1) g_m R_L - \frac{R_L}{R_s}\right) \gamma g_{d0} - \left(\left(1 - n_{opt}\right) g_m + \frac{1}{R_s}\right)\left(g_m^2 R_L + g_m + \frac{1}{R_s}\right) R_L = 0. \quad (9)$$

Figures 6(a) and (b) show the calculated F, F_{M_1}, and F_{R_L} ($R_L = 50\,\Omega$) versus n and NF with R_L as a parameter at $\omega = 1/\sqrt{L_p C_p}$, respectively. For $R_L = 50\,\Omega$, minimum F_{M_1}, F_{R_L}, and F are achieved for n of 0.68, 1.66, and 1.0, given by Eqs. (7)–(9), respectively. Figure 6(b) shows that the calculated NF ($R_L = 150\,\Omega$) for $n = 1.0$ is consistent with the simulated NF ($k = 1.0$) at 7.2 GHz, shown in Fig. 4, although R_p is ignored in Eqs. (4)–(6). Moreover, the NF becomes a minimum around one even with varying R_L from 50 to 200 Ω. A large n makes the LNA unstable, as will be explained in Section 3.4, and leads to an increase in the parasitic capacitance of L_s, causing poor high-frequency performance. The optimum n is thus determined to be one.

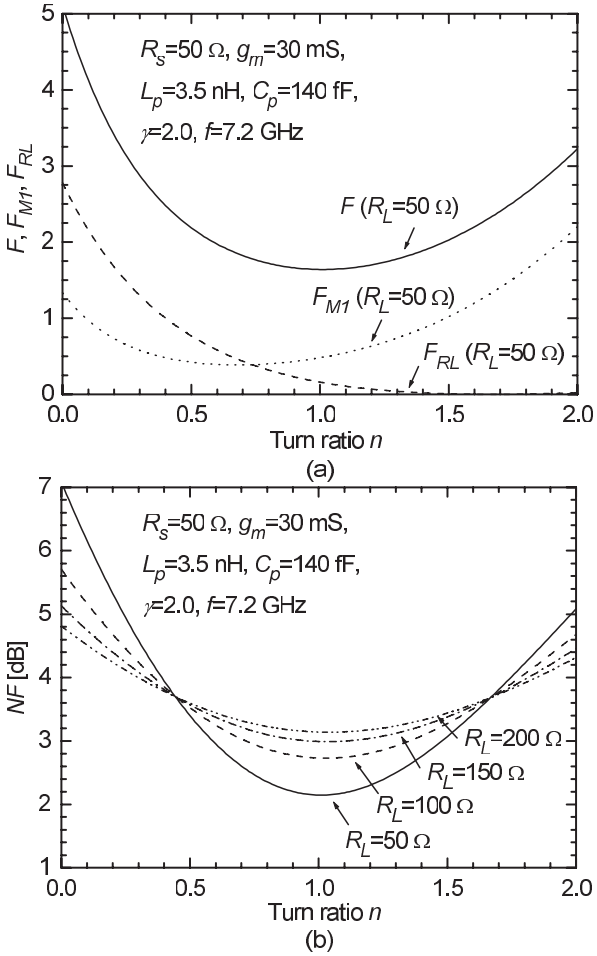


Fig. 6 Calculated (a) F, F_{M_1}, and F_{R_L} ($R_L = 50\,\Omega$) versus n and (b) NF with R_L as a parameter.

3.2 Input Impedance Matching

In the proposed topology with the input and shunt-peaking inductors coupled, the output load affects the LNA input impedance through the coupling. The output series inductor L_1 contributes to wideband input impedance matching. From Fig. 2, the input admittance of the proposed LNA, Y_{IN}, is given by

$$Y_{IN}(j\omega) = g_m + j\omega C_p + \frac{1}{j\omega L_p} + Y_T. \quad (10)$$

The first three terms in Eq. (10) represent the input admittance of the CG LNA. The last term Y_T is generated by coupling L_p and L_s, and is given by

$$Y_T(j\omega) = \frac{nk(nk - g_m Z_L)}{R_L + Z_L + j\omega n^2 L_p (1 - k^2)}. \quad (11)$$

When L_1 is connected in series with the output, Z_L is expressed as

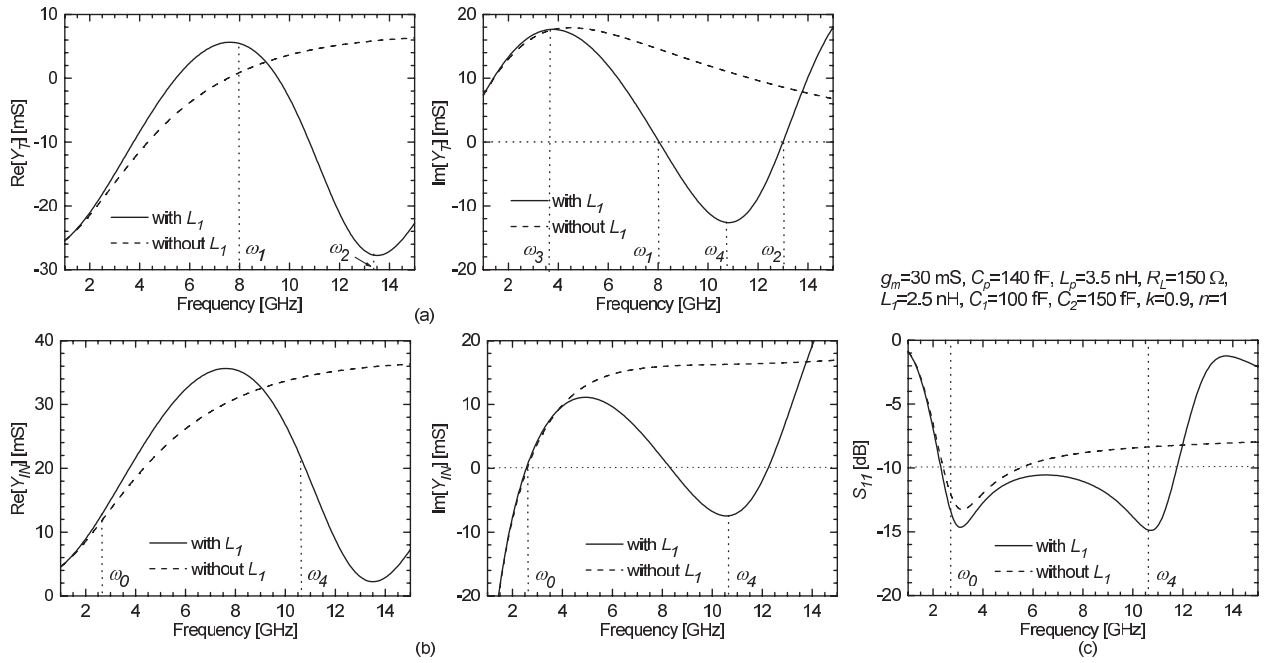


Fig. 7 Calculated real and imaginary parts of (a) Y_T and (b) Y_{IN}, and (c) S_{11} of the LNAs with and without L_1.

$$Z_L(j\omega) = \frac{1}{j\omega C_1} // \left(j\omega L_1 + \frac{1}{j\omega C_2} \right), \tag{12}$$

where C_1 represents the sum of the gate-drain capacitance of M_1 and the parasitic capacitance of L_1; C_2, which is typically larger than C_1, represents the sum of the input capacitance of the following stage and the parasitic capacitance of L_1. Equations (10)–(12) show that Y_{IN} is a function of Y_T, whose frequency behavior significantly depends on that of Z_L. From Eqs. (10)–(12), the calculated frequency behavior of Y_T is shown in Fig. 7(a) (solid line), and that of Y_T for $Z_L(j\omega) = 1/j\omega(C_1 + C_2)$ is also shown for comparison (dashed line). The π network consisting of C_1, L_1, and C_2 acts as a short or an open [23] (i.e., $Z_L = 0$ or ∞), providing a maximum and minimum $\mathrm{Re}[Y_T(j\omega)]$ and $\mathrm{Im}[Y_T(j\omega)]$:

$$\mathrm{Re}[Y_T(j\omega)]_{\max} \approx \frac{n^2k^2}{R_L}, \tag{13}$$

$$\mathrm{Re}[Y_T(j\omega)]_{\min} \approx -nkg_m, \tag{14}$$

$$\mathrm{Im}[Y_T(j\omega)]_{\max} \approx \frac{nk}{2}\left(g_m + \frac{nk}{R_L} \right), \tag{15}$$

$$\mathrm{Im}[Y_T(j\omega)]_{\min} \approx -\frac{nk}{2} \times \left(\frac{g_m \frac{L_1C_2}{C_1+C_2}}{\frac{L_1C_2}{C_1+C_2} + n^2(1-k^2)L_p} + \frac{nk}{R_L} \right), \tag{16}$$

at the following frequencies:

$$\omega_1 = \frac{1}{\sqrt{L_1C_2}}, \tag{17}$$

$$\omega_2 = \frac{1}{\sqrt{L_1 \frac{C_1C_2}{C_1+C_2}}}, \tag{18}$$

$$\omega_3 \approx \omega_c = \frac{1}{R_L(C_1+C_2)}, \tag{19}$$

$$\omega_4 \approx \frac{R_L}{\frac{L_1C_2}{C_1+C_2} + n^2(1-k^2)L_p}, \tag{20}$$

respectively. The above equations and approximations are derived from the following conditions: $Z_L = 0$ and $j\omega n^2(1-k^2)L_p$ is ignored against R_L in Eqs. (13) and (17); $Z_L = \infty$ in Eqs. (14) and (18); $Z_L = 1/j\omega(C_1 + C_2)$ and $\omega^2n^2(1-k^2)L_p(C_1+C_2) \ll 1$ in Eqs. (15) and (19); $Z_L = j\omega L_1C_2/(C_1+C_2)$ in Eqs. (16) and (20). A negative $\mathrm{Re}[Y_T(j\omega)]$ shown in Eq. (14) originates from the positive feedback provided by the transformer. The calculated Y_{IN} is also shown in Fig. 7(b). The real part of Y_{IN}, $\mathrm{Re}[Y_{IN}(j\omega)]$, is simply shifted by g_m from $\mathrm{Re}[Y_T(j\omega)]$, and the imaginary part of Y_{IN}, $\mathrm{Im}[Y_{IN}(j\omega)]$, becomes zero at resonance frequencies. The first resonance frequency ω_0 is derived from the following equation:

$$\mathrm{Im}[Y_{IN}(j\omega_0)] \approx j\omega_0C_p + \frac{1}{j\omega_0L_p} + j\omega_0 \frac{nk(C_1+C_2)(nk+g_mR_L)}{1+\omega_0^2R_L^2(C_1+C_2)^2} = 0, \tag{21}$$

where the last term in $\mathrm{Im}[Y_{IN}(j\omega_0)]$ is $\mathrm{Im}[Y_T(j\omega_0)]$ for $Z_L = 1/j\omega_0(C_1+C_2)$ and $\omega_0^2n^2(1-k^2)L_p(C_1+C_2) \ll 1$.

The requirements of g_m and R_L are derived from the input impedance matching condition in the frequency range from ω_0 to ω_1. For input impedance matching ($|S_{11}| < -10$ dB), Y_{IN} must satisfy the following condition:

$$|S_{11}| = \left| \frac{1 - R_sY_{IN}}{1 + R_sY_{IN}} \right| < 0.316. \tag{22}$$

When $\mathrm{Im}[Y_{IN}(j\omega)] = 0$, Eq. (22) can be simplified to

$$10\,\mathrm{mS} < \mathrm{Re}[Y_{IN}(j\omega)] < 38\,\mathrm{mS}. \tag{23}$$

At ω_0, $\mathrm{Im}[Y_{IN}(j\omega_0)] = 0$ and the real part of $Y_{IN}(j\omega)$ is approximated as

$$\mathrm{Re}[Y_{IN}(j\omega_0)] \approx g_m\left(1 - \frac{nk}{1+\omega_0^2 R_L^2(C_1+C_2)^2}\right), \tag{24}$$

where $\omega_0^2 nkR_L(C_1+C_2)^2/g_m \ll 1$. Substituting Eq. (24) into Eq. (23) gives the lower limit to g_m:

$$10\,\mathrm{mS} < g_m\left(1 - \frac{nk}{1+\omega_0^2 R_L^2(C_1+C_2)^2}\right). \tag{25}$$

In the frequency range from ω_0 to ω_1, the real and imaginary parts of Y_{IN} reach the maximum values at ω_1 and ω_3, respectively:

$$\mathrm{Re}[Y_{IN}(j\omega)]_{\max} = g_m + \frac{n^2k^2}{R_L}, \tag{26}$$

$$\mathrm{Im}[Y_{IN}(j\omega)]_{\max} = \omega_3 C_p - \frac{1}{\omega_3 L_p} + \frac{nk}{2}\left(g_m + \frac{nk}{R_L}\right), \tag{27}$$

where $\omega_0 < \omega_3 < \omega_1$ and $\omega_3 < 1/\sqrt{L_pC_p}$ are assumed. Substituting Eqs. (26) and (27) into Eq. (22), we can have the worst case upper limit to g_m and lower limit to R_L. For example, when $\mathrm{Im}[Y_{IN}(j\omega)]$ is negligible against $\mathrm{Re}[Y_{IN}(j\omega)]$ (around ω_1), the following condition is derived from Eqs. (22) and (26):

$$g_m + \frac{n^2k^2}{R_L} < 38\,\mathrm{mS}. \tag{28}$$

An impedance matching procedure for the proposed LNA is as follows:

1. Select g_m and R_L to satisfy Eqs. (25) and (28)
2. Select L_p such that ω_0 equals the lower edge of the desired input band
3. Select L_1 such that ω_4 equals the upper edge of the desired input band

Figure 7(c) shows the calculated S_{11} of the LNAs with and without L_1, where ω_0 and ω_4 are set to approximately 3.1 GHz and 10.6 GHz, respectively. A transconductance of 30 mS, a load resistance of 150 Ω, and other values shown in Fig. 7 result in $\mathrm{Re}[Y_{IN}(j\omega)]_{\max} \simeq 35\,\mathrm{mS}$ and $\mathrm{Im}[Y_{IN}(j\omega)]_{\max} \simeq 10\,\mathrm{mS}$, allowing $|S_{11}| < -10\,\mathrm{dB}$ from ω_0 to ω_1. Around ω_4, the π network including L_1 decreases $\mathrm{Re}[Y_{IN}(j\omega)]$ and $\mathrm{Im}[Y_{IN}(j\omega)]$:

$$\mathrm{Re}[Y_{IN}(j\omega_4)] = g_m - \frac{nk}{2R_L}\left(\frac{\omega_4 L_1 C_2 g_m}{C_1+C_2} - nk\right), \tag{29}$$

$$\mathrm{Im}[Y_{IN}(j\omega_4)] = \omega_4 C_p - \frac{1}{\omega_4 L_p} - \frac{nk}{2R_L}\left(\frac{\omega_4 L_1 C_2 g_m}{C_1+C_2} + nk\right), \tag{30}$$

providing $|S_{11}| < -10\,\mathrm{dB}$. Consequently, the input impedance matching is achieved from ω_0 to ω_4.

3.3 Gain

The transformer provides the positive feedback from node A to the input, as shown in Sect. 2.1. The transformer positive feedback reduces the gain (S_{21}) bandwidth of the LNA. The S_{21} of the LNA with output impedance matching is given by

$$S_{21} = \frac{v_{out}}{v_s/2} = \frac{2v_{in}}{v_s}\frac{v_{out}}{v_{in}} = \frac{2}{1+R_sY_{IN}}A_v, \tag{31}$$

where v_s is the signal voltage and A_v, defined by v_{out}/v_{in}, is the voltage gain from the input to the output of the LNA, as shown in Fig. 2. Equation (31) shows that the frequency response of A_v is shaped by that of Y_{IN} (i.e., S_{11}), which results in that of S_{21}.

The frequency response of A_v of the proposed LNA is similar to that of a CG LNA with a load resistor and output series inductor. The output network combining a shunt-peaking inductor with an output series inductor gives a larger bandwidth than the counterpart with either inductor, as explained in [23], [24]. However, the shunt-peaking inductor L_s in the proposed LNA does not increase the bandwidth. The A_v of the LNA is given by

$$A_v(s) = \frac{g_mR_L\left(1+\frac{nk}{g_mR_L}+\frac{1-k^2}{m_1}\frac{s}{\omega_c}\right)}{1+\frac{s}{\omega_c}+\left(\frac{1-k^2}{m_1}+\frac{1-k_c}{m_2}\right)\frac{s^2}{\omega_c^2}+\frac{k_c(1-k_c)}{m_2}\frac{s^3}{\omega_c^3}+\frac{1-k^2}{m_1}\frac{k_c(1-k_c)}{m_2}\frac{s^4}{\omega_c^4}}, \tag{32}$$

where $k_c = C_1/(C_1+C_2)$, $m_1 = R_L^2(C_1+C_2)/L_s$, and $m_2 = R_L^2(C_1+C_2)/L_1$ [24]. Substituting $k = 0$ into Eq. (32) gives the A_v of the CG LNA with both the shunt-peaking and output series inductors. Equation (32) shows that all m_1 are divided by a factor of $(1-k^2)$, i.e., L_s is multiplied by a factor of $(1-k^2)$. This means that the effective L_s in the proposed LNA becomes small, compared with the shunt-peaking inductor in the CG LNA, and then contributes less to bandwidth extension. The calculated A_v with k as a parameter is shown in Fig. 8, where $f_c = 4.2\,\mathrm{GHz}$, $k_c = 0.4$, $m_1 = 1.6$, and $m_2 = 2.25$ originate from $C_1 = 100\,\mathrm{fF}$, $C_2 = 150\,\mathrm{fF}$, $L_s = 3.5\,\mathrm{nH}$, $L_1 = 2.5\,\mathrm{nH}$, and $R_L = 150\,\Omega$. A very large peak (ripple) is found when $k = 0$, because L_s is larger than L_1, i.e., $m_1 < m_2$ [23], [24]. Figure 8 shows that both the peak and bandwidth decrease as k increases. Consequently, the bandwidth of the proposed LNA ($k \simeq 0.9$) closely equals that of the CG LNA with only the output series inductor. A flat voltage gain of the CG LNA across the entire UWB frequency band can be obtained by selecting an appropriate value of m_2 (approximately 2), as discussed in [24].

An S_{21} variation of the proposed LNA mainly originates from the characteristic of Y_{IN} (S_{11}). As shown in Fig. 7(c), the input impedance matching condition improves around ω_0 and ω_4, but deteriorates around ω_1. This means that an input signal of ω_1 is less transferred to the input of

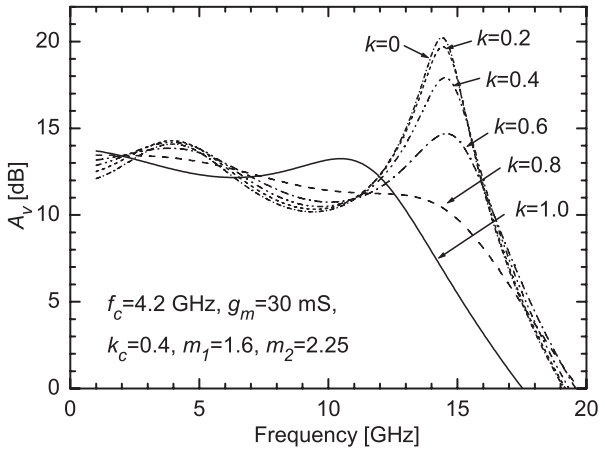


Fig. 8 Calculated A_v of the proposed LNA with k as a parameter.

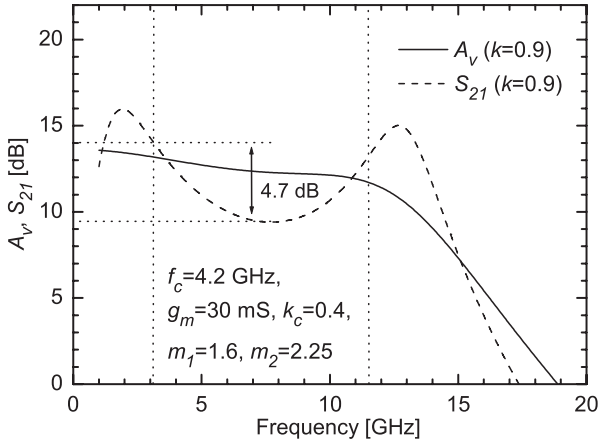


Fig. 9 Calculated A_v and S_{21} of the proposed LNA with $k = 0.9$.

the LNA, compared to that of ω_0 or ω_4, which results in a reduction in the magnitude of S_{21} around ω_1. The difference between $S_{21}(j\omega_0)$ and $S_{21}(j\omega_1)$ can be approximated from Eq. (31):

$$\begin{aligned}\Delta S_{21} &= \frac{S_{21}(j\omega_0)}{S_{21}(j\omega_1)} = \frac{1 + R_s Y_{IN}(j\omega_1)}{1 + R_s Y_{IN}(j\omega_0)} \\ &\approx \frac{1 + R_s \cdot \mathrm{Re}[Y_{IN}(j\omega_1)]}{1 + R_s \cdot \mathrm{Re}[Y_{IN}(j\omega_0)]},\end{aligned} \tag{33}$$

where $A_v(j\omega_0) = A_v(j\omega_1)$ is assumed, the real parts of $Y_{IN}(j\omega_0)$ and $Y_{IN}(j\omega_1)$ are given by Eqs. (24) and (26), respectively, and the imaginary parts of $Y_{IN}(j\omega_0)$ and $Y_{IN}(j\omega_1)$ can be neglected, as shown in the previous subsection. Figure 9 shows the calculated A_v and S_{21} of the proposed LNA with $k = 0.9$. Substituting the parameters shown in Fig. 9 into Eq. (33) gives $\Delta S_{21} = -3.6$ dB, while an S_{21} variation of -4.7 dB is seen in Fig. 9, and then -1.1 dB originates from the difference of A_v. The difference of S_{21} can be reduced by decreasing R_L, as shown by Eqs. (24), (26), and (33). Moreover, using a common-source (CS) amplifier with a gain peak around ω_1 as the second stage, we can obtain a flat gain.

3.4 Stability

The proposed LNA becomes potentially unstable, due to the transformer positive feedback. A linear two-port is unconditionally stable when it meets the following conditions [25]:

$$|\Gamma_S| < 1, \tag{34}$$
$$|\Gamma_L| < 1, \tag{35}$$
$$|\Gamma_{IN}| < 1, \tag{36}$$
$$|\Gamma_{OUT}| < 1, \tag{37}$$

where Γ_S, Γ_{IN}, Γ_L, and Γ_{OUT} represent the source, input, load, and output reflection coefficients, respectively. Equations (34)–(37) state that the real parts of the input and output impedances for passive source and load impedances must be positive [25]:

$$\mathrm{Re}[Z_{IN}] > 0, \tag{38}$$
$$\mathrm{Re}[Z_{OUT}] > 0. \tag{39}$$

In what follows, to simplify the expression of the output impedance of the LNA, we will verify whether the LNA without the output π network (C_1, L_1, and C_2) satisfies the above conditions or not.

First, the real part of the input admittance of the LNA can be derived from Eqs. (10)–(11) for $Z_L = \infty$:

$$\mathrm{Re}[Y_{IN}(j\omega)] = g_m(1 - nk). \tag{40}$$

In the case of the proposed LNA, n is selected to be one, shown in Sect. 3.1, and k of the on-chip transformer is less than one [26]: $nk < 1$. The requirement of Eq. (38) is thus satisfied. Next, the output impedance considering the left hand side of output node A (Fig. 2) is given by

$$Z_{OUT,A}(j\omega) = \frac{\left(\frac{1}{R_s} + g_m + j\omega C_p\right)\left(R_L + j\omega(1-k^2)L_s\right) + n^2 + \frac{R_L}{j\omega L_p}}{\frac{1}{R_s} + g_m(1-nk) + j\omega C_p + \frac{1}{j\omega L_p}}. \tag{41}$$

Equation (41) indicates that the real part of $Z_{OUT,A}$ becomes a maximum around $\omega = 1/\sqrt{L_p C_p}$ and can be approximated by

$$\mathrm{Re}[Z_{OUT,A}(j\omega)] \approx R_L, \tag{42}$$
$$\mathrm{Re}[Z_{OUT,A}(j\omega)] \approx R_L + \frac{(1-k^2)L_s}{C_p}\left(\frac{1}{R_s} + g_m\right), \tag{43}$$

at low and high frequencies (i.e., $\omega \ll 1/\sqrt{L_p C_p}$ and $\omega \gg 1/\sqrt{L_p C_p}$), respectively. The requirement of Eq. (39) is therefore satisfied.

The stability is also ensured through simulation. Figure 10 shows the simulated K and B_1 of the proposed LNA, which are given by [25]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}, \tag{44}$$

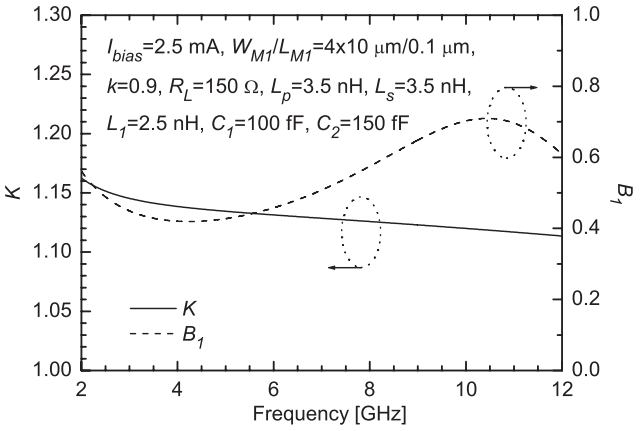


Fig. 10 Simulated K and B_1 of the proposed LNA.

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2, \tag{45}$$

respectively, where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. The necessary and sufficient conditions for unconditional stability are $K > 1$ and $B_1 > 0$ [25]. The simulations show that the LNA satisfies these conditions across the entire UWB frequency band.

3.5 Group Delay

A group delay variation is important for DS-UWB or pulse-based UWB systems. The group delay is the derivative of the phase of the signal transfer function (S_{21}), and hence any resonance in the signal path contributes to the variation [27]. The critical resonances in the proposed LNA originate from the combinations of L_p (transformer) and C_p at the input, and L_1, C_1, and C_2 at the output, and these resonance frequencies, ω_0 and ω_2, are given by Eqs. (21) and (18), respectively. Pushing the resonance frequencies out of the desired frequency band (i.e., increasing L_p or decreasing L_1) allows a small group delay variation. Figure 11 shows that the simulated group delays of the proposed LNA with L_p and L_1 as a parameter. The group delay (for $L_p = 3.0$ nH in Fig. 11(a)) dramatically changes around 3 GHz (ω_0) and 11 GHz (ω_2). The simulations also show that the variation can be reduced by increasing L_p or decreasing L_1.

4. Design

By using a 90 nm CMOS process and device parameters, the proposed LNA is designed to satisfy the following typical specifications of the UWB LNA: $|S_{11}| < -10$ dB, $NF < 4$ dB, and $|S_{21}| > 10$ dB across the entire UWB frequency band (3.1–10.6 GHz). Current consumption is set to 2.5 mA at a 1.0 V supply.

4.1 Input Transistor and Load Resistor

The transconductance g_m and load resistance R_L are determined by the input impedance matching conditions, given by Eqs. (25) and (28), and the desired gain. A transconductance of 30 mS and load resistance of 145 Ω provide both $|S_{11}| < -10$ dB and $A_v \simeq 14$ dB[†] in the lower UWB band (3.1–5 GHz). The load resistance includes the parasitic resistance of L_s. A bias current of 2.5 mA and g_m of 30 mS result in a gate width of $4 \times 10\,\mu$m (10 gate fingers, each with a unit of of $4\,\mu$m width) and gate length of 100 nm.

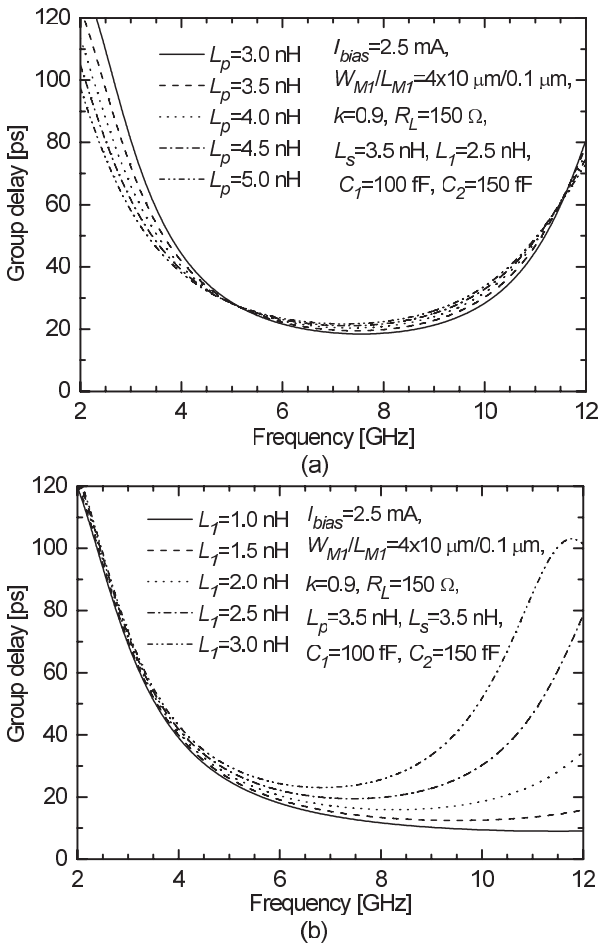


Fig. 11 Simulated group delays with (a) L_p and (b) L_1 as a parameter.

4.2 Transformer

The transformer adopts a stacked configuration in which L_p is stacked on L_s. This configuration provides the largest coupling factor and a small area [26]. The large parasitic resistance of L_s, due to the lower thin metal layer, is not problematic, because it can be absorbed into R_L.

The parasitic capacitance between L_p and L_s, C_c, has a relatively small effect on the LNA performance. This capacitance significantly affects the frequency response of a noninverting transformer [26]. Although the proposed LNA employs the noninverting stacked transformer, the signal current injected into L_s by M_1 reduces the effect of C_c. Figure 12 shows the simulated S_{11} and NF of the LNA includ-

[†]At low frequencies, $A_v \approx g_m R_L + nk = 5.25$.

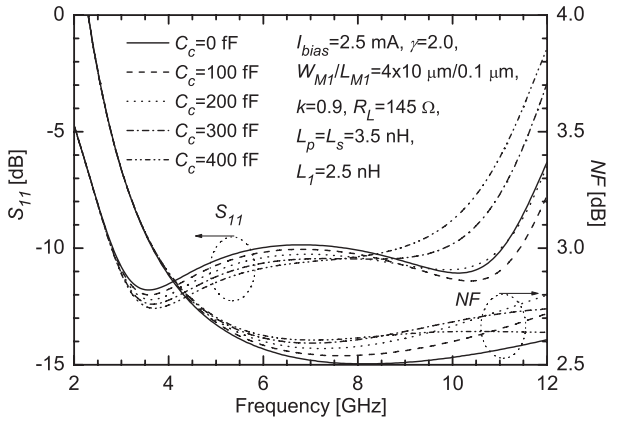


Fig. 12 Simulated S_{11} and NF of the LNA with C_c as a parameter.

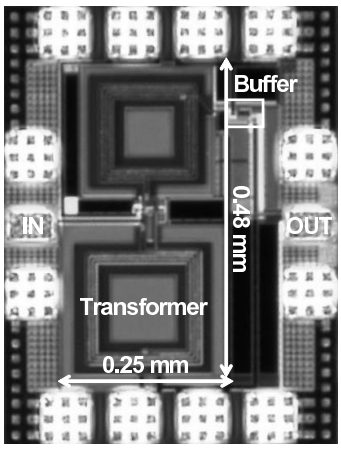


Fig. 13 Micrograph of the fabricated LNA.

ing C_c. In the lower UWB band, C_c slightly decreases the magnitude of the S_{11} and has little impact on the NF; in the higher, a large C_c decreases the input bandwidth and increases the NF by up to 0.20 dB. In the simulations, for wideband input impedance matching, C_c must be less than 300 fF, which can be realized even with the stacked transformer.

The transformer is designed to achieve $|S_{11}| < -10$ dB (of the LNA) in the lower UWB band and $NF < 4.0$ dB across the entire UWB band. Selecting L_p such that ω_0 equals approximately 3.1 GHz allows the LNA to achieve $|S_{11}| < -10$ dB in the lower band. A wide metal for realizing L_p reduces the parasitic resistance; however, it leads to a large chip area and large parasitic capacitance. For L_p, we adopt a 3.5-turn square inductor with an outer diameter of 165 μm, metal width of 3 μm, and metal spacing of 2 μm. To achieve a turn ratio of one, L_s is designed as follows: an outer diameter is 165 μm, a metal width 2 μm, and a metal spacing 3 μm. The metal thicknesses of L_p (top pad metal) and L_s (metal 6) are 1.9 μm and 0.9 μm, respectively†. The parasitic capacitance C_c is reduced by offsetting the upper metal layer from the lower by short horizontal distance (3 μm), which results in $C_c \simeq 240$ fF. Three-dimensional (3-D) electromagnetic (EM) simulations by Ansoft HFSS showed $L_p = L_s = 4.0$ nH and $k = 0.9$ at low frequencies.

4.3 Output Series Inductor

The output series inductor L_1 is designed to set ω_4 to the upper edge of the desired input band (10.6 GHz). We use a relatively low Q inductor to reduce the chip area and parasitic capacitance, which reduces the gain bandwidth of the LNA. The outer diameter of L_1 is 140 μm, the metal width 3 μm, the metal spacing 2 μm, and the metal thickness 1.9 μm (top pad metal)†. EM simulations showed that the inductance and maximum Q were 3.2 nH and 6.0 (at 5.0 GHz), respectively.

5. Experimental Results and Discussion

The designed LNA was fabricated in a 90 nm digital CMOS process without metal-insulator-metal (MIM) capacitors. A micrograph of the fabricated LNA is shown in Fig. 13. The active chip area excluding pads was 0.48×0.25 mm^2. The input and output pads were not electrostatic-discharge (ESD) protected. Metal fills consisting of metal 1–6 layers were placed both inside and outside the fabricated transformer and inductor to meet metal density rules in the CMOS process. They were 1.5 μm by 1.5 μm squares with a spacing of 0.2 μm. The average horizontal distance between the metal fills and traces of the inductors was 15 μm. For measurements, a unity-gain CS amplifier with a 50 Ω output resistor was used as a buffer. The S-parameters, noise, and linearity of the LNA were measured using on-wafer RF probes. The power consumption of the LNA and buffer were 2.5 mW and 4.0 mW, respectively, at a supply voltage of 1.0 V.

Figure 14 shows the measured and simulated S_{11} and S_{21} of the LNA. The LNA achieved $|S_{11}| < -10$ dB and $|S_{21}| > 9.3$ dB across 3.1–10.6 GHz. The discrepancy between the measurements and simulations at frequencies above 4 GHz is mainly attributed to insufficient accuracy in the simulations of the transformer and inductor used. The HFSS simulation models of the transformer and inductor included no metal fills to solve convergence problems and reduce the memory requirement. The metal fills increase the parasitic capacitances and resistances of the transformer and inductor [28]–[30], which results in the discrepancy.

Figure 15 shows the measured and simulated S_{12} of the LNA with the buffer. The LNA achieved $|S_{12}| < -34$ dB across 3.1–10.6 GHz. The measured S_{12} of the stand-alone buffer (not shown) was less than −24 dB over the same frequency range. Thus, the S_{12} of the LNA without the buffer was less than −10 dB. The poor reverse isolation performance is due to the transformer, and an additional stage may be required to improve the isolation performance.

Figure 16 shows the measured and simulated group de-

†The inductors L_p and L_1 in the previous work [17] were implemented by using metal 6 layers (0.9 μm thick) and L_s by using a metal 5 layer (0.3 μm thick). This leads to the differences between the simulations/measurements shown in [17] and in Sect. 5.

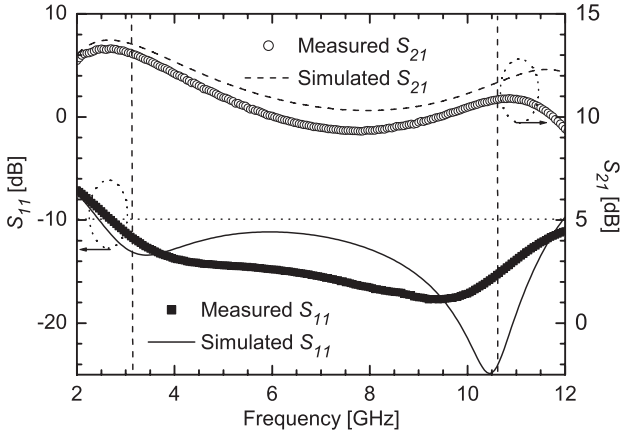


Fig. 14 Measured and simulated S_{11} and S_{21} of the LNA.

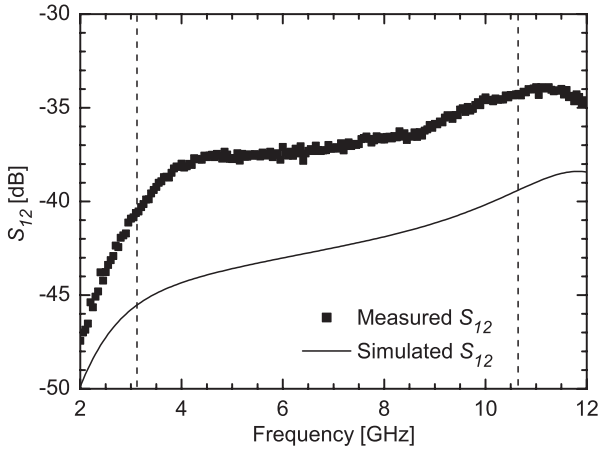


Fig. 15 Measured and simulated S_{12} of the LNA.

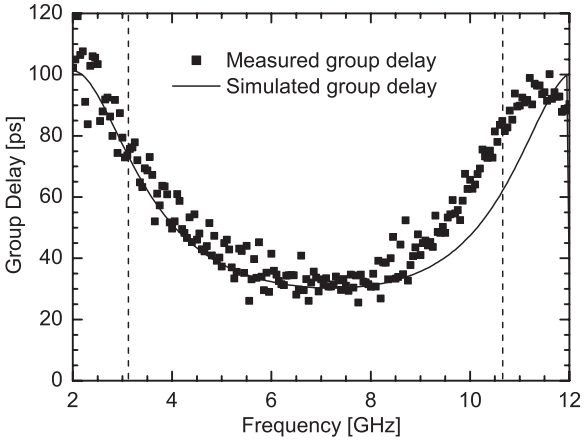


Fig. 16 Measured and simulated group delays of the LNA.

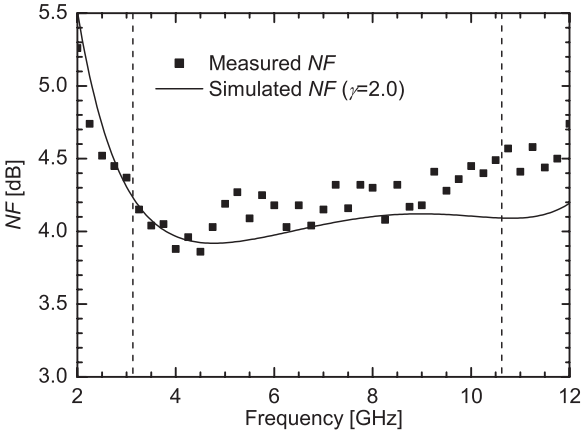


Fig. 17 Measured and simulated NF of the LNA.

lays. The group delay variation increased around the edge of the UWB frequency band, as analyzed in Sect. 3.5. A group delay variation of approximately 60 ps was achieved for the entire band.

Figure 17 shows the measured and simulated NF of the LNA. Note that these results included the noise of the output buffer, which increased the overall NF by 0.8 dB for an LNA gain of 10 dB in simulation. The LNA with the buffer achieved an NF of 3.8–4.4 dB[†] across the entire UWB band. This means that the proposed LNA with an additional CS amplifier like the buffer can achieve $NF < 4.4$ dB. The difference between the measurements and simulations can be explained by the extra input-referred noise of the buffer, caused by the lower measured gain than the simulated one.

Figure 18 shows the measured output power of the fundamental tone and third-order intermodulation (IM_3) products for two tones (3.000 GHz and 3.001 GHz). The measured input third-order intercept point (IIP_3) and 1-dB compression point (including the effect of the output buffer) were approximately −9.3 dBm and −20 dBm, respectively. Figure 19 shows IIP_3 and IIP_2 measured by applying two tones (f_{I1} and f_{I2}) with 1-MHz spacing. The measured frequency range of 3–6 GHz was limited by a signal generator, and IM_3 and IM_2 products were measured at $2f_{I1} - f_{I2}$ and $f_{I1} + f_{I2}$[††], respectively. The LNA obtained $IIP_3 > -9.3$ dBm and $IIP_2 > -6.3$ dBm in the frequency range.

Table 1 shows a summary of the LNA performance and a comparison with previously reported wideband CMOS LNAs. The proposed LNA achieved input impedance matching and comparable noise performance across the entire UWB band with the lowest reported power consumption and supply voltage. The LNA also consumed the smallest chip area among the 3.1–10.6 GHz LNAs employing inductors [10], [11], [16], [24].

An additional amplifier stage can allow the proposed LNA to achieve more and flatter gain across 3.1–10.6 GHz. A relatively low gain of the implemented LNA (> 9.3 dB) leads to an increase in the overall NF of the receiver. For instance, the NF specification for RF receivers of the MB-

[†]We found noise measurement errors in the previous work [17]. We overmeasured the loss of an input cable by approximately 1.0 dB. This resulted in smaller measured NF in [17] by 1.0 dB.

[††]Due to the wideband characteristic of a UWB LNA, IM_2 products at $f_{I1} + f_{I2}$ generated by the LNA do not decrease and then affect the performance of a receiver.

OFDM UWB system is less than 6.6 dB [31], [32]. A receiver employing the proposed LNA may have difficulty in satisfying such an NF specification. A CS amplifier with a load inductor, shown in Fig. 20, improves the LNA gain, alleviating this problem. The CS amplifier is designed to have a gain peak around 8.0 GHz and power consumption of 2.0 mW. The 2.6-nH inductor consists of stacked square spiral inductors implemented by the top pad metal and metal 6 layers, and occupies only $55\times55\,\mu m^2$. Figure 21 shows the simulated S_{21} and NF of the LNAs with and without the CS amplifier. The inductor was designed by using the EM simulator. The LNA with the CS amplifier achieved more and flatter gain ($|S_{21}| > 20$ dB) and the same noise performance as the LNA without the CS amplifier ($NF < 4.3$ dB) across 3.1–10.6 GHz. The group delay variation (not shown) was reduced to approximately 20 ps. Considering the measurements of the fabricated LNA, we conclude that the proposed LNA with the CS amplifier can achieve $|S_{21}| > 20$ dB and $NF < 4.4$ dB across 3.1–10.6 GHz with an additional power consumption of 2.0 mW and chip area of $55 \times 55\,\mu m^2$.

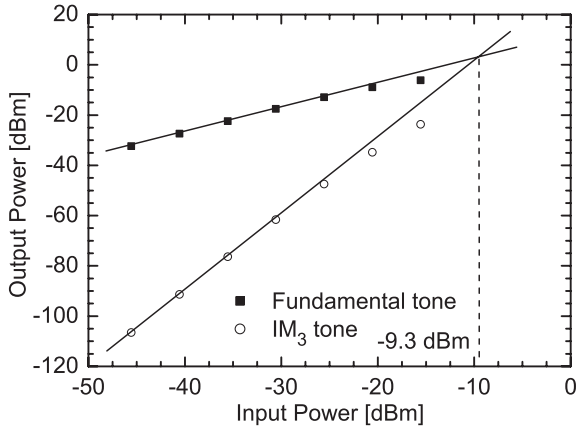


Fig. 18 Measured IIP_3 of the LNA at 3 GHz.

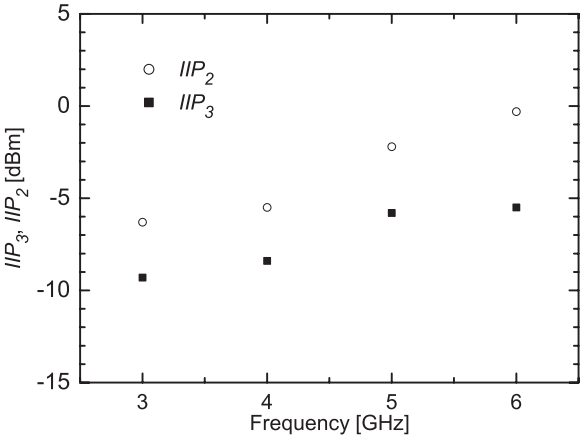


Fig. 19 Measured IIP_3 and IIP_2 of the LNA.

6. Conclusion

We have demonstrated a transformer noise-canceling UWB CMOS LNA with an output series inductor. The transformer partly cancels the noise of the common-gate transistor and load resistor, thereby improving the LNA noise performance. The output series inductor improves both the gain and input bandwidths. Circuit analysis showed

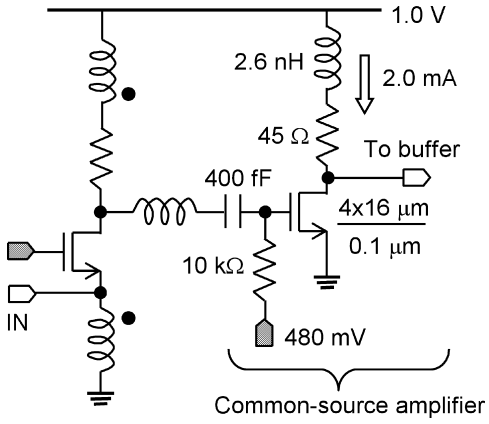


Fig. 20 Common-source amplifier with a load inductor.

Table 1 Measured performance and comparison of wideband CMOS LNAs.

Reference	CMOS Technology	BW* [GHz]	NF [dB]	S_{21} [dB]	IIP_3 [dBm]	Supply [V]	Power† [mW]	Area [mm^2]	Topology
This work	90 nm	2.8–12	3.8–4.4‡	9.3–13.1‡	−9.3	1.0	2.5	0.12	Transformer noise-canceling CG
[4]	90 nm	0.5–6.2	1.9–2.6	25°	−16	2.7	35.2	0.025	Resistive feedback CS
[6]	90 nm	0.5–5.0	2.3–2.6	21–22°	−8.8	1.8	12	0.012	Resistive feedback CS
[7]	90 nm	0–6	3.4–4.3	12.5–15.3	N/A	1.0	3.4	0.0017	Common-drain feedback CS
[8]	130 nm	1–7.4	>2.4	15–17°	−4.1	1.4	25	0.019	Common-drain feedback CS★
[10]	130 nm	3.1–10.6	2.1–2.9	13.7–16.5	−8.5	1.2	9.0	0.40	Reactive feedback CS
[11]	180 nm	0–14.1	4.5–5.1‡	12.0–13.7‡	−6.2	1.8	20	0.50	Noise-canceling CG using CS
[13]	65 nm	0.2–6.2	2.8–4.2	9.9–15.6°	0	1.2	14	0.009	Noise-canceling CG using CS
[14]	130 nm	3.7–8.8	3.6–4.5	8.1–11	−7.2	1.5	19	0.05	Noise-canceling CS
[16]	180 nm	1–11	2.9–3.0	8–9	−3.55	1.8	21.6	0.20	Distributed
[24]	180 nm	2.6–10.7	4.4–5.3‡	6.0–8.5‡	7.4	1.8	4.5	0.40	Capacitor cross-coupled CG★

*Input bandwidth †Without buffers ‡3.1–10.6 GHz frequency range °Voltage gain ★Input-output differential topology

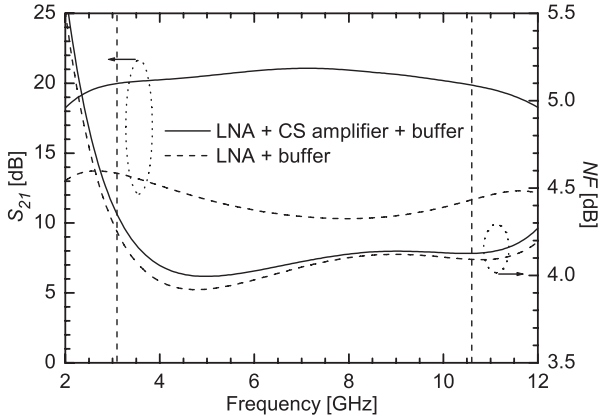


Fig. 21 Simulated S_{21} and NF of the LNAs with and without the common-source amplifier.

that the best turn ratio for the noise performance is one and input impedance matching depends not only on the common-gate transistor but also on the load resistor. The LNA designed for UWB applications was fabricated in a 90 nm digital CMOS process. The fabricated LNA occupied 0.12 mm^2, and achieved $|S_{11}| < -10$ dB, $NF < 4.4$ dB, and $|S_{21}| > 9.3$ dB across 3.1–10.6 GHz, while consuming 2.5 mW from a 1.0 V supply. The proposed topology is the most suitable for low-power and low-voltage UWB CMOS LNAs.

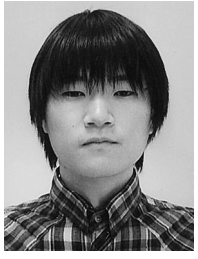
Acknowledgment

The chip in this study was fabricated through the chip fabrication program of the VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Semiconductor Technology Academic Research Center (STARC), Fujitsu Limited, Matsushita Electric Industrial Company Limited., NEC Electronics Corporation, Renesas Technology Corporation, and Toshiba Corporation. In addition, this study was financially supported by a grant to the Osaka University Global COE Program, "Center for Electronic Devices Innovation" from the Ministry of Education, Culture, Sports, Science and Technology of Japan, and Initiatives for Attractive Education in Graduate Schools from Japan Society for the Promotion of Science (JSPS).

References

[1] MultiBand OFDM Alliance SIG, "Multiband OFDM physical layer proposal for IEEE 802.15 task group 3a," Sept. 2004.
[2] R. Fisher, R. Kohno, H. Ogawa, H. Zhang, K. Takizawa, M. McLaughlin, and M. Welborn, "DS-UWB physical layer submission to 802.15 task group 3a," Sept. 2005.
[3] A. Bevilacqua and A.M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1–10.6 GHz wireless receivers," IEEE J. Solid-State Circuits, vol.39, no.12, pp.2259–2268, Dec. 2004.
[4] J.H.C. Zhan and S.S. Taylor, "A 5 GHz resistive-feedback CMOS LNA for low-cost multi-standard applications," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp.200–201, San Francisco, CA, Feb. 2006.
[5] B.G. Perumana, J.H.C. Zhan, S.S. Taylor, and J. Laskar, "A 12 mW, 7.5 GHz bandwidth, inductor-less CMOS LNA for low-power, low-cost, multi-standard receivers," IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers, pp.57–60, Honolulu, HI, June 2007.
[6] B.G. Perumana, J.H.C. Zhan, S.S. Taylor, B.R. Carlton, and J. Laskar, "Resistive-feedback CMOS low-noise amplifiers for multiband applications," IEEE Trans. Microw. Theory Tech., vol.56, no.5, pp.1218–1225, May 2008.
[7] J. Borremans, P. Wambacq, and D. Linten, "An ESD-protected DC-to-6 GHz 9.7 mW LNA in 90 nm digital CMOS," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp.422–423, San Francisco, CA, Feb. 2007.
[8] R. Ramzan, S. Andersson, J. Dabrowski, and C. Svensson, "A 1.4 V 25 mW inductorless wideband LNA in 0.13 μm CMOS," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp.424–425, San Francisco, CA, Feb. 2007.
[9] M.T. Reiha, J.R. Long, and J.J. Pekarik, "A 1.2 V reactive-feedback 3.1–10.6 GHz ultrawideband low-noise amplifier in 0.13 μm CMOS," IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers, pp.41–44, San Francisco, CA, June 2006.
[10] M.T. Reiha and J.R. Long, "A 1.2 V reactive-feedback 3.1–10.6 GHz low-noise amplifier in 0.13 μm CMOS," IEEE J. Solid-State Circuits, vol.42, no.5, pp.1023–1033, May 2007.
[11] C.F. Liao and S.I. Liu, "A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers," IEEE J. Solid-State Circuits, vol.42, no.2, pp.329–339, Feb. 2007.
[12] S. Chehrazi, A. Mirzaei, R. Bagheri, and A.A. Abidi, "A 6.5 GHz wideband CMOS low noise amplifier for muti-band use," Proc. IEEE Custom Integrated Circuits Conf., pp.801–804, San Francisco, CA, Sept. 2005.
[13] S.C. Blaakmeer, E.A. Klumperink, B. Nauta, and D.M. Leenaertsr, "An inductorless wideband balun-LNA in 65 nm CMOS with balanced output," Proc. IEEE European Solid-State Circuits Conf., pp.364–367, Munich, Germany, Sept. 2007.
[14] Q. Li and Y.P. Zhang, "A 1.5-V 2–9.6-GHz inductorless low-noise amplifier in 0.13-μm CMOS," IEEE Trans. Microw. Theory Tech., vol.55, no.10, pp.2015–2023, Oct. 2007.
[15] F. Zhang and P.R. Kinget, "Low-power programmable gain CMOS distributed LNA," IEEE J. Solid-State Circuits, vol.41, no.6, pp.1333–1343, June 2006.
[16] P. Heydari, "Design and analysis of a performance-optimized CMOS UWB distributed LNA," IEEE J. Solid-State Circuits, vol.42, no.9, pp.1892–1905, Sept. 2007.
[17] T. Kihara, T. Matsuoka, and K. Taniguchi, "A 1.0 V, 2.5 mW, transformer noise-canceling UWB CMOS LNA," IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers, pp.493–496, Atlanta, GA, June 2008.
[18] D.J. Allstot, X. Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers, pp.97–100, Fort Worth, TX, June 2004.
[19] A. Liscidini, C. Ghezzi, E. Depaoli, G. Albasini, I. Bietti, and R. Castello, "Common gate transformer feedback LNA in a high IIP3 current mode RF CMOS front-end," Proc. IEEE Custom Integrated Circuits Conf., pp.25–28, San Francisco, CA, July 2006.
[20] P.P. Jindal, "Compact noise models for MOSFETs," IEEE Trans. Electron Devices, vol.53, no.9, pp.2051–2061, Sept. 2006.
[21] Y. Kiyota, C.H. Chen, T. Kubodera, A. Nakamura, K. Takeshita, and M.J. Deen, "A new approach of high frequency noise modeling for 70-nm NMOS transistors by accurate noise source extraction," IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers, pp.635–638, Honolulu, HI, June 2007.
[22] J. Jussila and P. Sivonen, "A 1.2-V highly linear balanced noise-cancelling LNA in 0.13-μm CMOS," IEEE J. Solid-State Circuits, vol.43, no.3, pp.579–587, March 2008.
[23] S. Galal and B. Razavi, "40-Gb/s amplifier and ESD protection circuit in 0.18-μm CMOS technology," IEEE J. Solid-State Circuits, vol.39, no.12, pp.2389–2396, Dec. 2004.
[24] S. Shekhar, J.S. Walling, and D.J. Allstot, "Bandwidth extension

techniques for CMOS amplifiers," IEEE J. Solid-State Circuits, vol.41, no.11, pp.2424–2439, Nov. 2006.
[25] G. Gonzalez, Microwave Transistor Amplifiers, 2 ed., Prentice Hall, Upper Saddle River, NJ, 1997.
[26] J.R. Long, "Monolithic transformers for silicon RF IC design," IEEE J. Solid-State Circuits, vol.35, no.9, pp.1368–1381, Sept. 2000.
[27] Y. Park, C.H. Lee, J.D. Cressler, and J. Laskar, "The analysis of UWB SiGe HBT LNA for its noise, linearity, and minimum group delay variation," IEEE Trans. Microw. Theory Tech., vol.54, no.4, pp.1687–1697, April 2006.
[28] J.H. Chang, Y.S. Youn, H.K. Yu, and C.K. Kim, "Effects of dummy patterns and substrate on spiral inductors forsub-micron RF ICs," IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers, pp.419–422, Seattle, WA, June 2002.
[29] F. Zhang and P.R. Kinget, "Design of components and circuits underneath integrated inductors," IEEE J. Solid-State Circuits, vol.41, no.10, pp.2265–2271, Oct. 2006.
[30] L. Nan, K. Mouthaan, Y.Z. Xiong, J. Shi, S.C. Rustagi, and B.L. Ooi, "Experimental characterization of the effect of metal dummy fills on spiral inductors," IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers, pp.307–310, Honolulu, HI, June 2007.
[31] A. Batra, J. Balakrishnan, G.R. Aiello, J.R. Foerster, and A. Dabak, "Design of a multiband OFDM system for realistic UWB channel environments," IEEE Trans. Microw. Theory Tech., vol.52, no.9, pp.2123–2138, Sept. 2004.
[32] R. Roovers, D.M.W. Leenaerts, J. Bergervoet, K.S. Harish, R.C.H. van de Beek, G. van der Weide, H. Waite, Y. Zhang, S. Aggarwal, and C. Razzell, "An interference-robust receiver for ultra-wideband radio in SiGe BiCMOS technology," IEEE J. Solid-State Circuits, vol.40, no.12, pp.2563–2572, Dec. 2005.



Takao Kihara received the B.S., M.S., and Ph.D. degrees in electronic engineering from Osaka University, Osaka, Japan, in 2005, 2006, and 2009, respectively. His current research interests include CMOS RF transceivers.

Toshimasa Matsuoka received the B.S., M.S., and Ph.D. degrees in electronic engineering from Osaka University, Osaka, Japan, in 1989, 1991, and 1996, respectively. During 1991–1998, he worked for the Central Research Laboratories, Sharp Corporation, Nara, Japan, where he was engaged in the research and development of deep submicron CMOS devices and ultra thin gate oxides. Since 1999, he has been working for Osaka University, where he is Associate Professor now. His current research includes MOS device modeling and CMOS RF circuits. Dr. Matsuoka is a member of the Japan Society of Applied Physics (JSAP), the Institute of Electrical Engineers of Japan (IEEJ), and the Institute of Electrical and Electronic Engineers (IEEE).

Kenji Taniguchi received the B.S., M.S., and Ph.D. degrees from Osaka University, Osaka, Japan, in 1971, 1973, and 1986, respectively. From 1973 to 1986, he worked for Toshiba Research and Development Center, Kawasaki, Japan where he was engaged in process modeling and the design of MOS LSI fabrication technology. He was a Visiting Scientist at Massachusetts Institute of Technology, Cambridge, from July 1982 to November 1983. Presently, he is a Professor of Electrical, Electronic and Information Engineering at Osaka University. His current research interests are analog circuits, radio frequency circuits, device physics and process technology. Prof. Taniguchi is a member of the Japan Society of Applied Physics (JSAP), the Institute of Electrical Engineers of Japan (IEEJ), and the Institute of Electrical and Electronic Engineers (IEEE).