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Yoshimoto, Shusuke
Amashita, Takuro
Okumura, Shunsuke
Kawaguchi, Hiroshi
Yoshimoto, Masahiko

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PAPER

Multiple-Bit-Upset and Single-Bit-Upset Resilient 8T SRAM Bitcell Layout with Divided Wordline Structure*

Shusuke YOSHIMOTO[†a)], ***Student Member***, **Takuro AMASHITA**[†], ***Nonmember***, **Shunsuke OKUMURA**[†], ***Student Member***, **Hiroshi KAWAGUCHI**[†], ***and*** **Masahiko YOSHIMOTO**[††], ***Members***

SUMMARY This paper presents a new 8T (8-transistor) SRAM cell layout mitigating multiple-bit upset (MBU) in a divided wordline structure. Because bitlines along unselected columns are not activated, the divided wordline structure eliminates a half-select problem and achieves low-power operation, which is often preferred for low-power/low-voltage applications. However, the conventional 8T SRAM with the divided wordline structure engenders MBUs because all bits in the same word are physically adjoining. Consequently, it is difficult to apply an error correction coding (ECC) technique to it. In this paper, we propose a new 8T cell layout pattern that separates internal latches in SRAM cells using both an n-well and a p-substrate. We saw that a SEU cross section of nMOS is 3.5–4.5 times higher than that of pMOS (SEU: single event upset; a cross section signifies a sensitive area to soft error effects). By using a soft-error simulator, iRoC TFIT, we confirmed that the proposed 8T cell has better neutron-induced MBU tolerance. The simulator includes soft-error measurement data in a commercial 65-nm process. The MBU in the proposed 8T SRAM is improved by 90.70% and the MBU soft error rate (SER) is decreased to 3.46 FIT at 0.9 V when ECC is implemented (FIT: failure in time). Additionally, we conducted Synopsys 3-D TCAD simulation, which indicates that the linear energy transfer (LET) threshold in SEU is also improved by 66% in the proposed 8T SRAM by a common-mode effect.

key words: *SRAM, soft error, multiple-bit upset (MBU), single-event upset (SEU), error correction coding (ECC), alpha particle, neutron particle*

1. Introduction

The minimum feature size in transistors continues to decrease with the advance of process technology. Process scaling realizes higher density and lower cost. In a deep submicron era, the threshold voltage (Vt) deviation in transistors is, however, increasing to more than 100 mV as $3\sigma_{Vt}$ [1], [2]. Consequently, designing a 6T SRAM cell, presented in Fig. 1, has been more difficult: both read and write margins must be considered [3]. The 8T SRAM cell presented in Fig. 2(a) was proposed to eliminate read failures caused by the dedicated read port (comprising NRA and NRD) [4]. Therefore, in the 8T cell, only the write margin must be considered, which can make a layout smaller and less expensive than the 6T cell in future processes [4].

Figures 3(a) and 3(b) portray a general bit-interleaving SRAM structure and a divided wordline structure [5]. In the write operation in the general structure, all access gates (NA0 and NA1 in Fig. 2) in one end's cell to the other are activated. Then selected BLs are discharged or charged by write drivers. Consequently, the other BLs, which are unse-

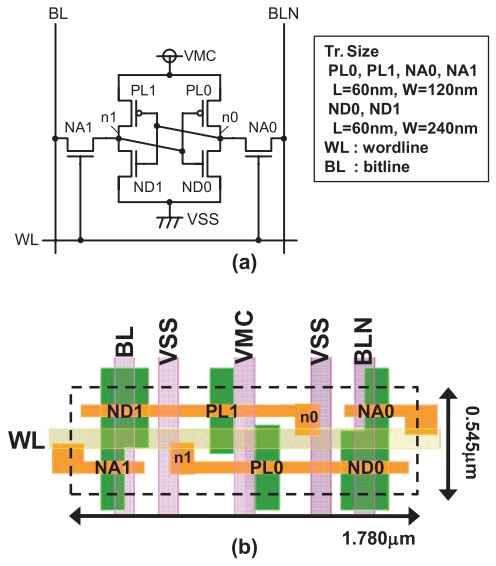

Fig. 1 (a) Schematic and (b) layout of 6T cell in 65-nm CMOS process (logic rule basis).

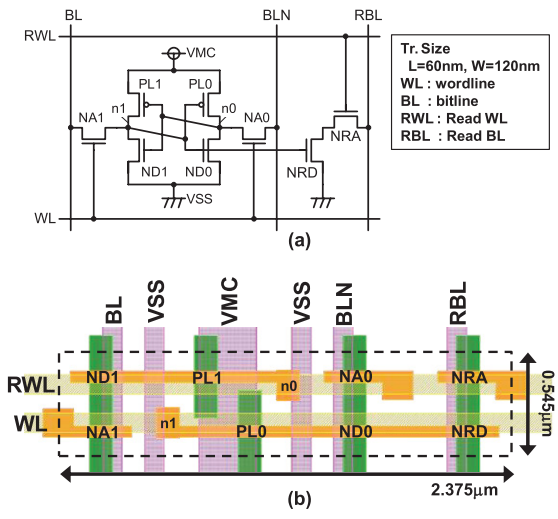

Fig. 2 (a) Schematic and (b) layout of conventional 8T cell in 65-nm CMOS process (logic rule basis) [4].

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[†]The authors are with Kobe University, Kobe-shi, 657-8501 Japan.
[††]The author is with JST CREST, Kobe-shi, 657-8501 Japan.
*This paper is the modified version of the original paper presented at the IOLTS 2011 [14].
a) E-mail: yoshipy@cs28.cs.kobe-u.ac.jp
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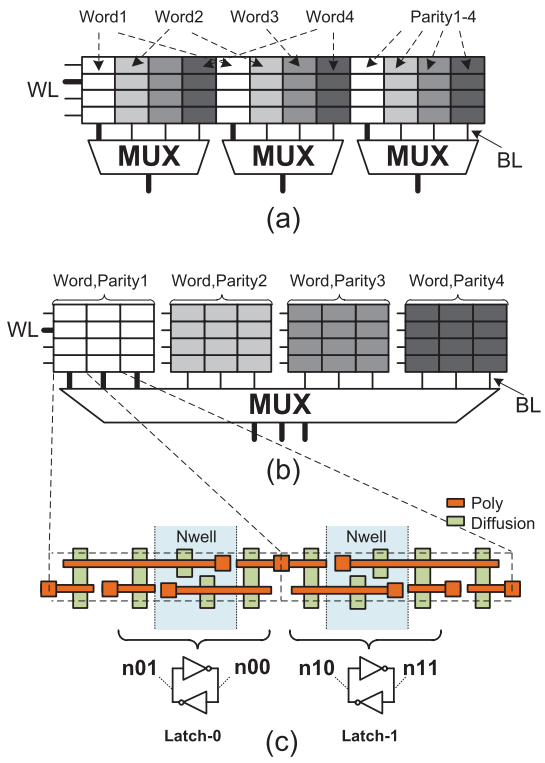

Fig. 3 (a) General structure, (b) divided wordline structure, and (c) conventional 8T SRAM cell layout pattern. ECC requires extra parity bits.

lected, incur the half-select problem [6] and consume large amounts of active power. The general structure has drawbacks related to low-power and low-voltage operation.

The divided wordline structure separates one word from others, and a large multiplexer (MUX) outputs a selected word. The BLs in the selected columns are only discharged, which can avoid the half-select problem and achieve low power. However, a conventional 8T SRAM with a divided wordline structure still holds the MBU problem in a word. Figure 3(c) presents the conventional 8T cell layout and alignment pattern. Because the conventional bilaterally symmetric allocation produces two adjacent latches (Latch-0 and Latch-1), two-bit upset in the horizontal direction can easily occur by a heavy-ion strike. In addition, the two adjoining nodes (n00 and n10) are n-diffusions, whose critical linear energy transfer (LET) is a quarter or less than that of p-diffusion [7]; it is difficult to avoid the MBU in a word in the conventional 8T cell.

As described in this paper, we propose a novel MBU-tolerant 8T cell layout and its alignment pattern. As presented in Fig. 4, a pMOS (PL0), nMOSes (ND0, NA0, ND1, NA1), pMOS (PL1) and nMOSes (NRA and NRD) form p-n-p-n diffusions. The internal latches are separated and not adjoining. The sensitive nMOSes (ND0 and ND1) are adjacent in a single cell, by which enhancing a SER tolerance can be expected using a common-mode effect [8]. Therefore, the proposed 8T cell layout achieves MBU tolerance, even in the divided wordline structure.

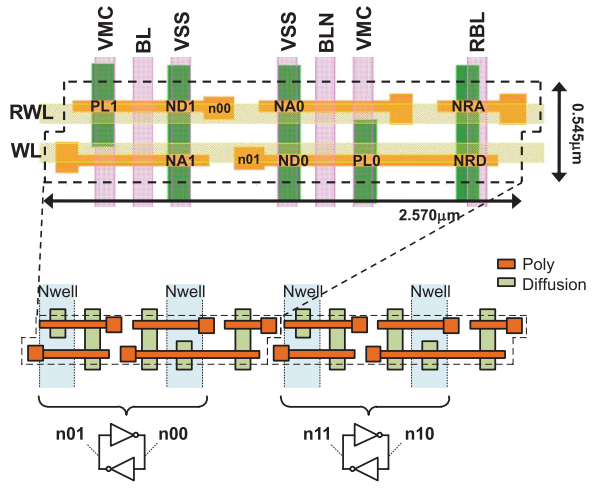

Fig. 4 Proposed 8T cell layout and alignment pattern.

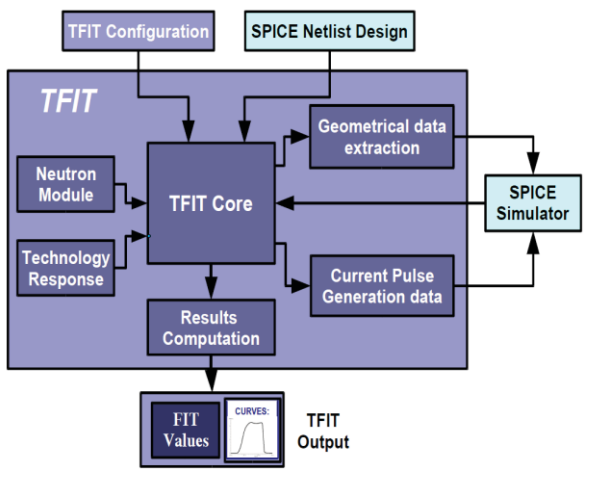

Fig. 5 TFIT simulation flow diagram [9].

2. Soft-Error Simulation Results

2.1 TFIT Simulation

iRoC TFIT is a tool for simulating soft errors caused by heavy ions and neutrons on semiconductor devices [9]. Figure 5 presents the TFIT simulation flow diagram. In reality, TFIT has a database of disturb currents and soft-error behaviors extracted from the Synopsys TCAD simulator, which is fitted to measurement data. In the TFIT simulation flow, we used a 65-nm generic CMOS database and a 65-nm predictive technology model (PTM) model for SPICE simulations [13].

Figures 6 and 7 present SEU cross sections of nMOSes (ND1 = ND2 = ND and NA1 = NA2 = NA) and pMOSes (PL1 = PL2 = PL) in a latch, respectively. The cross section is defined by an area in which a heavy ion strikes and a cell is flipped. The LET of a heavy ion was varied from 10 to 90 fC/μm. The cross section area was set from the center of the drain diffusion. We observed that the cross sections at

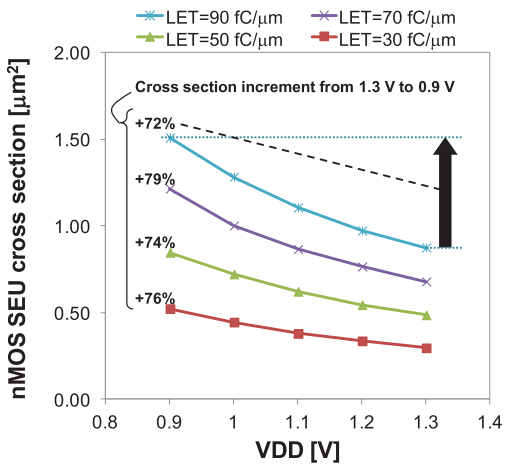

Fig. 6 SEU cross section in nMOSes (shared drain diffusion of ND and NA).

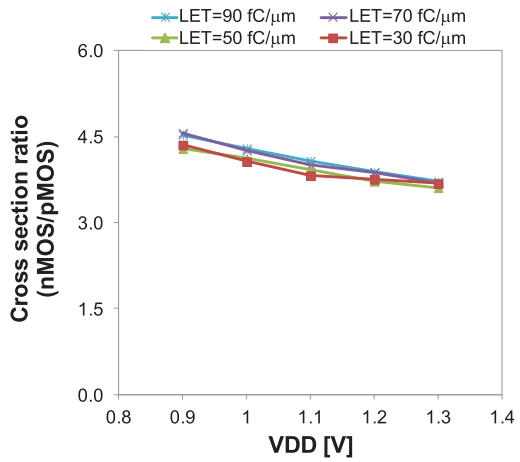

Fig. 8 Cross section ratio of nMOS to pMOS.

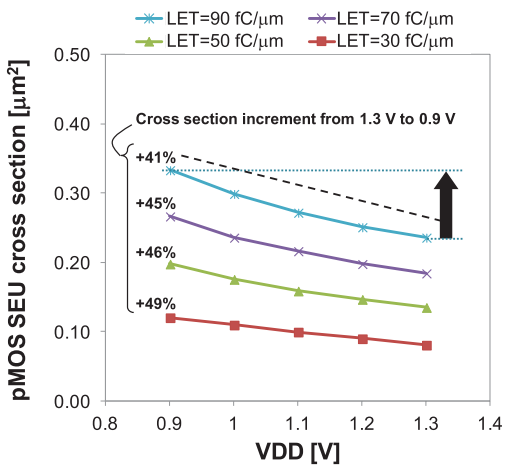

Fig. 7 SEU cross section in pMOSes (drain diffusion of PL).

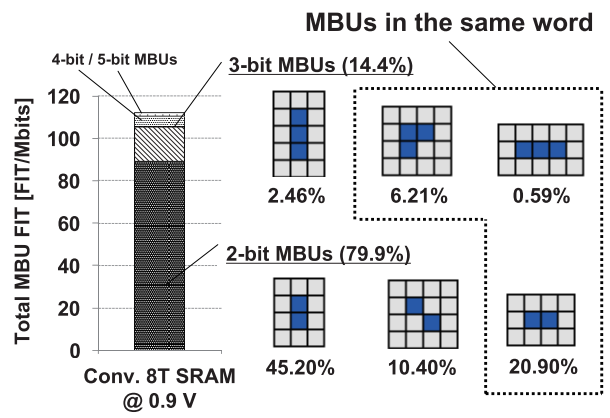

Fig. 9 MBU pattern examples in conventional 8T SRAM at 0.9 V. Note that they are examples; there are other patterns to be considered.

0.9 V are 72–79% larger than at 1.3 V in the nMOSes. In the pMOSes, their cross sections at 0.9 V are 41–49% larger than at 1.3 V. For examples, at an LET of 90 fC/μm, the factors are 72% and 41% in the nMOSes and pMOSes, respectively. As a result, the SEU cross section ratio of nMOS to pMOS is increased in the lower-voltage region; Fig. 8 presents that it is 3.5 at 1.3 V but goes up to 4.5 at 0.9 V. Because the proposed cell layout has nMOSes in the middle and the sensitive n-diffusions are separated in two adjoining cells, it can decrease the horizontal MBUs.

We also investigated neutron-induced MBU SER considering both horizontal and vertical directions, and compared the conventional and proposed 8T layout patterns. The TFIT has neutron-induced SER database fitted to sea level in New York. The SRAM data pattern was set to random and the memory capacity was assumed as 1 Mbits. Figure 9 portrays the MBU FIT and the error pattern examples in the conventional 8T SRAM at 0.9 V. The MBUs in the vertical direction can be corrected by ECC, but the two-bit or more upsets in the horizontal direction are not, which might cause important problems such as system failure. In the conventional 8T SRAM, the rates of the MBUs in the same words are 22.84% (2-bit MBU), 7.57% (3-bit MBU), 2.27% (4-bit MBU), and 0.56% (5-bit MBU) at 0.9 V; the total rate comes to 33.24% (= 22.84% + 7.57% + 2.27% + 0.56%).

Figure 10 shows that, in the divided wordline structure with the conventional 8T cell, the MBU SER reduction rate by ECC is 66.76% (= 100.00% – 33.24%) at 0.9 V as mentioned above. On the other hand, the MBU SER is decreased by 96.27% in the proposed 8T cell because the internal latches are separated by the n-well and p-substrate; the MBU in the same word is improved by 90.70% using the proposed layout.

In the proposed 8T SRAM, the total rate of the MBU in the same word is 3.73%, which is broken down into 0.00% (2-bit MBU), 2.72% (3-bit MBU), 0.81% (4-bit MBU), and 0.20% (5-bit MBU). The MBU SER is calculated as 3.46 FIT in ECC (FIT: failure in time). Table 1 presents neutron simulation results at 0.9–1.3 V; The MBU SERs are reduced by 66.76–69.02% with ECC in the conventional 8T cell while those in the proposed 8T cell correspond to

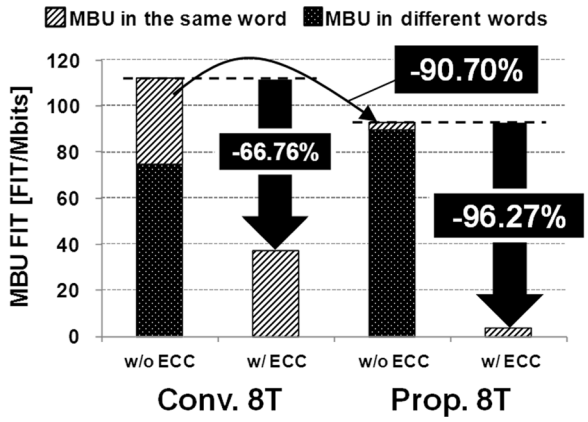

Fig. 10 Neutron-induced MBU improvement at 0.9 V in divided wordline structure: conventional and proposed 8T SRAMs.

Table 1 MBU reduction rate.

Type	VDD [V]	MBU SER w/o ECC [FIT]	MBU SER w/ ECC [FIT]	MBU SER reduction rate
	0.9	111.92	37.20	-66.76%
	1.0	85.87	27.85	-67.56%
Conv. 8T	1.1	64.68	20.77	-67.89%
	1.2	43.79	13.60	-68.95%
	1.3	37.12	11.50	-69.02%
	0.9	92.78	3.46	-96.27%
	1.0	68.49	2.57	-96.24%
Prop. 8T	1.1	50.04	1.82	-96.36%
	1.2	32.68	1.06	-96.74%
	1.3	26.79	0.85	-96.81%

96.24–96.81%. This demonstrates that the proposed 8T cell suppresses the MBU SER in the same word effectively.

2.2 Synopsys 3-D TCAD Simulation

We investigated an SEU tolerance in the proposed 8T SRAM layout using Synopsys 3-D TCAD simulation [10]. The proposed 8T cell has two internal nodes (N1 and N0) of nMOSes (ND and NA) in the middle. The distance between the nodes is 0.46 μm. When a heavy ion strikes an area around them, these nodes are pulled down; in this case, the SEU tolerance is expected to be improved because of the common-mode effect. However, the conventional 8T cell is separated nMOSes by n-well and has no common-mode effect. In this simulation, two nMOSes (ND0 and ND1) in the proposed 8T cell and one nMOS (ND1) in the conventional 8T cell were made with 65-nm 3-D device models [11]. The other transistors were based on the PTM 65-nm SPICE model. The gate length and width of the nMOS were set respectively to 60 nm and 120 nm.

Figure 11 portrays a cross section and an ion strike point of an nMOS: Fig. 11(a) shows the case of the conventional 8T cell, and Fig. 11(b) shows the proposed 8T cell case. The heavy ion strikes at 0.23 μm, which is far away from the edge of the drain node.

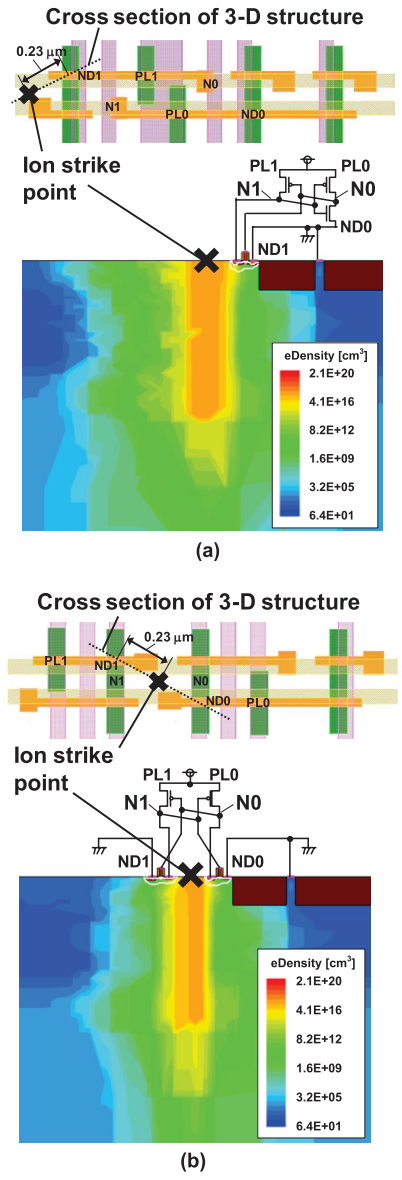

Fig. 11 Cross sections and ion strike points of nMOSes in (a) conventional 8T cell layout pattern (same as Fig. 2) and (b) proposed 8T cell layout pattern (same as Fig. 4). LET of heavy ion is 5.49 MeV.

Figures 12(a) and 12(b) show internal waveforms in the conventional and proposed 8T cells. The conventional 8T cell was flipped by the impact. In contrast, the proposed 8T cell is not flipped, which best explains the phenomenon of the common-mode effect. Figure 13 shows an LET threshold (LETth) improvement at 0.9 V in the proposed 8T cell. In this 3D TCAD simulation, the common-mode effect enhances the LETth from 1.360 MeV to 2.264 MeV (+66%). In reality, note that the improvement depends on the position and LET of the ion strike; however, the total effect in the proposed 8T cell is confirmed in the previous subsection.

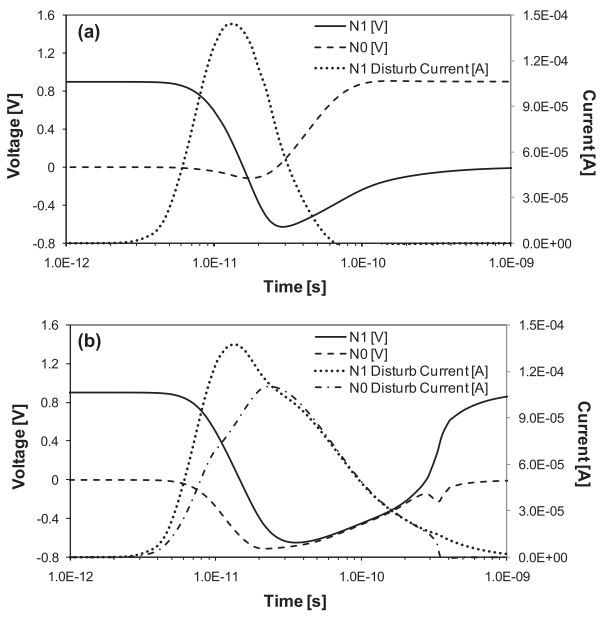

Fig. 12 Waveforms of internal nodes' (N1 and N0) voltages and their disturb currents in (a) conventional and (b) proposed 8T cells.

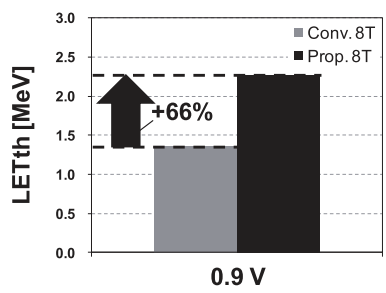

Fig. 13 LETth improvement at supply voltage of 0.9 V.

3. Area and Power Comparisons

3.1 Area Comparison

The proposed 8T SRAM layout has an area overhead due to its p-n-p-n diffusion. In addition, the divided wordline structure requires an extra AND gate for each word. In this subsection, we mention the overheads in the proposed layout.

Table 2 shows a cell area comparison (the conventional 6T cell, the conventional 8T cell, and the proposed 8T cell). The three kinds of cells are all designed in a 65-nm CMOS logic rule, as illustrated in Figs. 1, 2, and 4. The cell area overhead in the conventional and the proposed 8T cell is 33% and 44% over the conventional 6T cell, respectively.

Figure 14 shows area overheads on an SRAM macro level when a bits/word (B in Table 2) is varied. The conventional 6T SRAM macro has the bit-interleaving structure and the conventional and proposed 8T SRAM macros have the divided wordline structure. The cell arrays consist of eight words/row and 256 cells/bitline. The SRAM macros

Table 2 SRAM array features.

	Conv. 6T SRAM	Conv. 8T SRAM	Prop. 8T SRAM
Cell area [um2]	0.9701 / cell	1.294 / cell	1.401 / cell
(ratio to 6T)	(× 1.00)	(× 1.33)	(× 1.44)
Array style	Bit interleaving	Divided WL	Divided WL
Configuration	B bits/word × 8 words/row × 256 cells/bitlines		
ECC	1-bit correction		

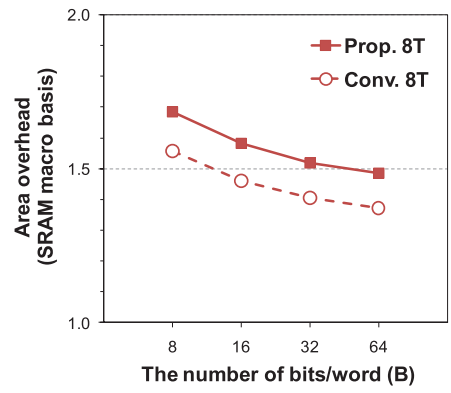

Fig. 14 Area overheads on an SRAM array level when the number of bits/word (B in Table 2) is varied.

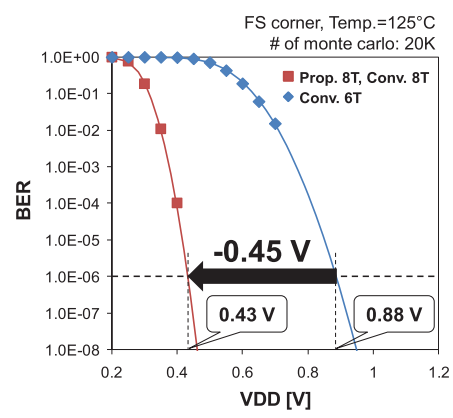

Fig. 15 Bit error rates (BERs) in the proposed and conventional 8T SRAMs and the conventional 6T SRAM. The minimum operation voltage is defined at a BER of 10^{-6}.

are equipped with 1-bit correcting ECC. As the word width (B) is increased, the array area overheads are decreased. The proposed 8T SRAM is 48% larger than the conventional 6T SRAM when using 64 bits/word.

3.2 Power Comparison

The proposed 8T SRAM layout has the drawbacks in the area overhead; however, it improves a minimum operating voltage as well as the conventional 8T SRAM.

Figure 15 portrays bit error rates (BERs) in the proposed and conventional 8T SRAMs and the 6T SRAM on the worst-case condition (FS corner and 125°C). A static

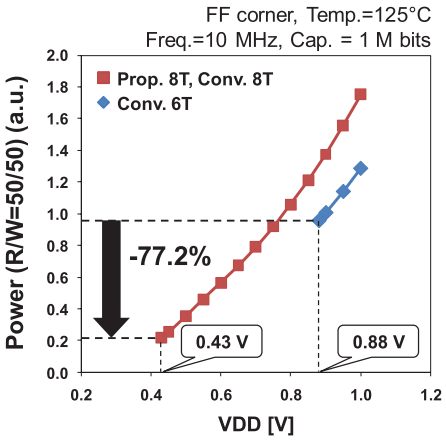

Fig. 16 Operating powers in the proposed and conventional 8T SRAMs and the conventional 6T SRAM.

noise margin (SNM) is used as a metric to evaluate the BERs [12]. Note that the proposed 8T SRAM has the same BER curve as the conventional one because their transistor sizes are identical. Since the 8T SRAMs can eliminate the half-select problem, the minimum operating voltage is reduced from 0.88 V to 0.43 V (0.45-V improvement). The minimum operation voltage is defined at a BER of 10^{-6}.

Figure 16 shows operating power including peripheral circuits in the proposed and conventional 8T SRAMs and the 6T SRAM (when read/write = 50/50 and the power worst corner: FF corner and 125°C). The memory capacity is 1 Mbits, and the clock cycle is set to 10 MHz. The proposed 8T cell has slightly longer wordlines and thus larger wordline metal capacitance than the conventional 8T cell; however, the power in the proposed SRAM consumes the same power as the conventional one because the power overhead in the proposed SRAM is negligible in the total power when the peripheral circuits are considered. Although the 8T SRAMs consume an extra power due to its single-ended read port, the operating voltage can be decreased and thus the power is improved by 77.2%. Consequently, the proposed 8T SRAM achieves a low-voltage and low-power operation as well as the conventional 8T SRAM.

4. Conclusion

We proposed an MBU-tolerant 8T SRAM cell layout with the divided wordline structure. The proposed layout improves MBU in the divided wordline by 90.70%, and the MBU SER is decreased to 3.46 FIT at a supply voltage of 0.9 V. TCAD simulation of results indicated that the proposed 8T cell layout improves the LETth by 66% due to the common-mode effect. The proposed 8T SRAM array has a 48% area overhead over the conventional 6T SRAM; however, the minimum operation voltage can be improved by 0.45 V and thus the operation power is decreased by 77.2%. Consequently, it can be said that the proposed 8T cell layout enhances soft-error reliability in the divided wordline structure and can achieve low-power and low-voltage operation.

Acknowledgments

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Shusuke Yoshimoto received B.E. and M.E. degrees in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2009 and 2011, respectively. He is currently working in the doctoral course at that university. His current research is low-power and soft-error tolerant SRAM designs. He was a recipient of IEEE SSCS 2011 Japan Chapter Academic Research Award. He is a student member of IPSJ and IEEE.

Takuro Amashita received his B.E. degree in Computer and Systems Engineering in 2010 from Kobe University, Hyogo, Japan, where he is currently working in the M.E. course. His current research is soft-error tolerant SRAM designs.

Shunsuke Okumura received his B.E. and M.E. degrees in Computer and Systems Engineering in 2008 and 2010, respectively from Kobe University, Hyogo, Japan, where he is currently working in the doctoral course. His current research is high-performance, low-power SRAM designs, dependable SRAM designs, and error correcting codes implementation. He is a student member of IPSJ and IEEE.

Hiroshi Kawaguchi received his B.E. and M.E. degrees in Electronic Engineering from Chiba University, Chiba, Japan, in 1991 and 1993, respectively, and earned a Ph.D. degree in Engineering from The University of Tokyo, Tokyo, Japan, in 2006. He joined Konami Corporation, Kobe, Japan, in 1993, where he developed arcade entertainment systems. He moved to the Institute of Industrial Science, The University of Tokyo, as a Technical Associate in 1996, and was appointed as a Research Associate in 2003. In 2005, he moved to Kobe University, Kobe, Japan. Since 2007, he has been an Associate Professor with the Department of Information Science at that university. He is also a Collaborative Researcher with the Institute of Industrial Science, The University of Tokyo. His current research interests include low-voltage SRAM, RF circuits, and ubiquitous sensor networks. Dr. Kawaguchi was a recipient of the IEEE ISSCC 2004 Takuo Sugano Outstanding Paper Award and the IEEE Kansai Section 2006 Gold Award. He has served as a Design and Implementation of Signal Processing Systems (DISPS) Technical Committee Member for IEEE Signal Processing Society, as a Program Committee Member for IEEE Custom Integrated Circuits Conference (CICC) and IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), and as a Guest Associate Editor of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences and IPSJ Transactions on System LSI Design Methodology (TSLDM). He is a member of IEEE, ACM, and IPSJ.

Masahiko Yoshimoto earned his B.S. degree in Electronic Engineering from Nagoya Institute of Technology, Nagoya, Japan, in 1975, and an M.S. degree in Electronic Engineering from Nagoya University, Nagoya, Japan, in 1977. He earned a Ph.D. degree in Electrical Engineering from Nagoya University, Nagoya, Japan in 1998. He joined the LSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan, in April 1977. During 1978–1983 he was engaged in the design of NMOS and CMOS static RAM including a 64K full CMOS RAM with the world's first divided-wordline structure. From 1984, he was involved in research and development of multimedia ULSI systems for digital broadcasting and digital communication systems based on MPEG2 and MPEG4 Codec LSI core technology. Since 2000, he has been a Professor of the Department of Electrical and Electronic Systems Engineering at Kanazawa University, Japan. Since 2004, he has been a Professor of the Department of Computer and Systems Engineering at Kobe University, Japan. His current activities are research and development of multimedia and ubiquitous media VLSI systems including an ultra-low-power image compression processor and a low-power wireless interface circuit. He holds 70 registered patents. He served on the Program Committee of the IEEE International Solid State Circuit Conference during 1991–1993. Additionally, he served as a Guest Editor for special issues on Low-Power System LSI, IP, and Related Technologies of IEICE Transactions in 2004. He received R&D100 awards in 1990 and 1996 from R&D Magazine for development of the DISP and development of a real-time MPEG2 video encoder chipset, respectively.