
FOREWORD

Special Section on Low-Power and High-Speed Chips

Low-power and high-speed chips (Cool Chips) encompass a broad range of architectures, applications, methodologies, and usage models. These technologies are present not only in multimedia, digital consumer electronics, mobile, graphics, encryption, robotics, networking, and biometrics, but also in the peta-scale computers. They are based on multiprocessing, reconfigurable computing, dependable computing, and memory architectures. Cool software, which includes binary translators and compilers, is also emerging.

These technologies all aim to reduce power consumption and enhance chip performance. Regardless of their goals, all of industry has been challenged with developing optimal solutions—both hardware and software—for power optimization according to the required performance. In general, in an attempt to migrate decades' worth of legacy approaches to low-power technology, industry approaches these optimal solutions from the perspective of starting from scratch.

With this in mind, we've been organizing annual Cool Chips conferences since 1998. We celebrated Cool Chips XIX in April 2016. Cool Chips, a sister conference to Hot Chips, focuses on all aspects of cool technologies. Approximately 150 individuals attend the conference. In addition to regular paper presentations, the conference includes keynote and invited talks, special topic sessions, and poster and panel discussions. To attract submissions from engineers working in industry, the program committee bases acceptance on a short abstract. The conference proceedings include only the short abstract with the final presentation rather than a set of long papers.

It is our great honor to announce the publication of this special section on Low-Power and High-Speed Chips. The section is devoted to variety of techniques for COOL Chips. It contains 5 papers, among 11 submissions, which covers, low power techniques for network on chips, memory access architectures including caches, and dedicated hardware architectures, and power control techniques spanning over system and software levels.

On behalf of the editorial committee, we would like to express our sincere appreciation to all the authors for their contributions and to all the reviewers for their critical reviewing papers. Lastly, I would like to thank the editorial committee for their work on this special section, especially, secretaries: Prof. Wada and Prof. Egawa.

Special Section Editorial Committee Members

Secretary: Yasutaka Wada (Meijo University), Ryusuke Egawa (Tohoku University)

Guest Associate Editors: Sugako Otani (Renesas), Yukinori Sato (JAIST), Yuichiro Shibata (Nagasaki University), Kotaro Shimamura (Hitachi), Hiroyuki Takizawa (Tohoku University), Mitaro Namiki (Tokyo University of Agriculture and Tech.), Masanori Muroyama (Tohoku University), Keiji Kimura (Waseda University), Yuetsu Kodama (University of Tsukuba), Jun Yao (Huawei)

Fumio Arakawa (Nagoya University) and Makoto Ikeda (The University of Tokyo), Guest Editor-in-Chief

Fumio Arakawa (*Member*) is a designated professor of Graduate School of Information Science at Nagoya University. His research interests include architecture and micro-architecture of low-power and high-performance microprocessors. Arakawa has a PhD in electrical engineering from the University of Tokyo. He is a program committee co-chair of the Cool Chips conference series, a program committee member of the VLSI Circuits Symposium, and a steering committee member of International Symposium on Embedded Multi/Many-core SoCs.



Makoto Ikeda (*Member*) is a professor in the Electrical Engineering and Information Systems department at the University of Tokyo. His research interests include high-performance, low-power, and reliable digital circuit and smart image sensor design. He is a program committee co-chair of the Cool Chips conference series, and a program committee member of the International Solid-State Circuits Conference, VLSI Circuits Symposium, Asian Solid-State Circuits Conference, and several others. Ikeda has a PhD in electrical engineering from the University of Tokyo.

