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LETTER *Special Section on Circuits and Systems*

Consideration of Integrated Low-Frequency Low-Pass Notch Filter Employing CCII Based Capacitance Multipliers

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SUMMARY In a field of biomedical engineering, not only low-pass filters for high frequency elimination but also notch filters for suppressing powerline interference are necessary to process low-frequency biosignals. For integration of low-frequency filters, chip implementation of large capacitances is major difficulty. As methods to enhance capacitances with small chip area, use of capacitance multipliers is effective. This letter describes design consideration of integrated low-frequency low-pass notch filter employing capacitance multipliers. Two main points are presented. Firstly, a new floating capacitance multiplier is proposed. Secondly, a technique to reduce the number of capacitance multipliers is proposed. By this technique, power consumption is reduced. The proposed techniques are applied a 3rd order low-pass notch filter. Simulation results show the effectiveness of the proposed techniques.

key words: *analog filters, low-frequency filters, low-pass notch filters, elliptic filters, capacitance multipliers*

1. Introduction

A Low-frequency filter plays an important role in a field of biomedical engineering. In a range of several to several tens Hz for EEG (electroencephalograph) measurement, not only low-pass filters for high frequency elimination but also notch filters for suppressing powerline interference are necessary. For such a demand, a filter with both low-pass and notch characteristics is useful [1]–[3]. Coexistence of low-pass and notch characteristics is realized by an elliptic filter, which is easily synthesized employing LC ladder structure as a prototype. Further, the elliptic filter can realize sharper notch than a well-known RC twin-T notch filter.

For integration of low-frequency filters, implementation of large resistances and capacitances is major difficulty against chip area. Capacitance values for frequency range of biosignals are several hundreds pF to several nF. Integration of a filter with such large capacitances on a chip is impossible. As methods to enhance capacitances with small chip area, capacitance multipliers have been proposed [4]–[6]. Enhancement of a capacitance is based on current feedback and is realized by a current amplifier, which amplifies the signal current flowing through a capacitor so as to unchange the signal voltage. As the current amplifiers, current mirrors, CCIIs (2nd generation Current Conveyors) with multiplied current output at Z terminal, and VCIIs (2nd generation voltage conveyor) with multiplied current output at X terminal, are used.

An LC ladder elliptic filter as a prototype of a low-pass notch filter has floating capacitors. Floating-type capacitance multipliers are needed to enhance the floating capacitances. Recently, several floating capacitance multipliers have been proposed [7]–[15]. Any of those circuits contain the block which have many terminals or several additional blocks, such as a CCCII [7], [8], a DV-CCTA [9], a CCD-DCC [10], a DVCC [8], [11], [12], [15], a translinear circuit [13], and an OTA[14]. The author group has proposed symmetry-type floating capacitance multipliers, which are effective for fully-balanced filters [16], [17]. However, because a common-mode feedback circuit is necessary, those circuits can not be applied to normal (unbalanced) elliptic filters which is focused on this study.

This letter describes design consideration of integrated low-frequency low-pass notch filter employing capacitance multipliers. Two main points are presented in this letter, Firstly, a floating capacitance multiplier, whose basic structure and operation principle are simple, is proposed. The circuit is constructed of only a capacitor and an MO (Multi-Output) CCII, which is simply combined with two CCIIs and has two Z terminals. The proposed circuit can be applied to not only a low-pass notch filter but also various low-frequency circuit having floating capacitors.

Secondly, a method to reduce the number of capacitance multipliers which is applicable to a low-pass notch filter is proposed. In this technique, the number of CCII is less than that of capacitors. Thus, this technique is very effective to reduce power consumption and the scale of circuit structure.

2. Filter Design

2.1 Prototype of Low-Pass Notch Filter

A low-pass notch characteristic is obtained by an LC ladder filter which is characterized by elliptic functions. In order to explain essence of new techniques in this letter, we consider the simplest prototype which is a 3rd order elliptic LC filter shown in Fig. 1 though sufficient stop-band attenuation is not obtained. Aiming for application to EEG measurement, the cut-off frequency f_0 and the notch frequency f_n are set to 40 Hz and 50 Hz, respectively. Under the condition of this frequency ratio, $f_n/f_0 = 1.25$, obtained element values from design table [18] are as follows:

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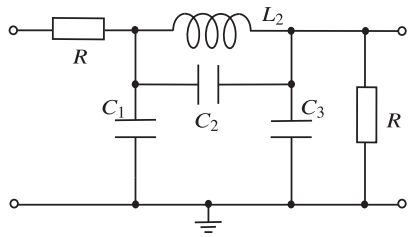


Fig. 1 3rd order LC ladder filter with elliptic function.

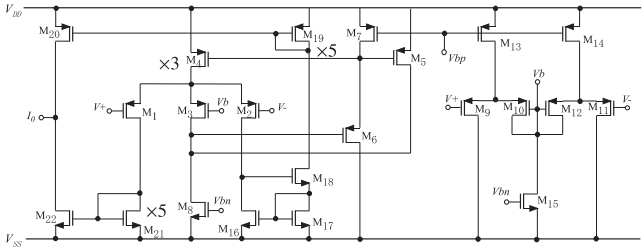


Fig. 2 Circuit configuration of OTA.

$$\begin{cases} R = 1 \\ L_2 = 0.4547 \\ C_1 = C_3 = 1.4922 \\ C_2 = 1.4198 \end{cases} \tag{1}$$

From these values, minimum stop-band attenuation A_{min} and pass-band ripple A_{max} become 15.3 dB and 1.25 dB, respectively.

2.2 Filter Integration

In many integrated filters, the cutoff frequency deviates from the ideal one due to variations in the PVT process. Therefore, an active filter with g_m-variable OTA circuits as active component blocks and an automatic tuning system to correct the cutoff frequency is commonly used.

The circuit configuration of the single-ended OTA employed in this study is illustrated in Fig. 2. This OTA has tunability and linear input range more than 100 mV with even simple structure and low-voltage operation. This circuit is based on the OTA proposed in the Ref. [19]. A signal current attenuator composed of M16-M22 is added to set the g_m to a small value so that the capacitances are as small as possible. From pre-simulation, a transconductance of 48 nS has been obtained. Setting impedance level to $1/g_m$ and $f_0 = 40$ Hz, the following capacitance values are obtained.

$$\begin{cases} C_L = 86.8\,\text{pF} \\ C_1 = C_3 = 285\,\text{pF} \\ C_2 = 271\,\text{pF} \end{cases} \tag{2}$$

Each capacitance requires huge area much larger than unit chip. Using the capacitance multiplier allows these capacitances to be implemented on a normal chip.

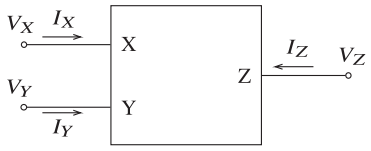
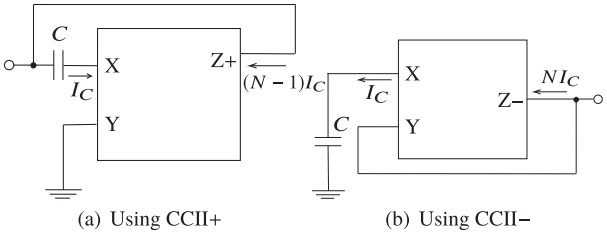


Fig. 3 Block diagram of CCII.



(a) Using CCII+ (b) Using CCII−

Fig. 4 Grounded capacitance multipliers constructed of a CCII.

3. Grounded Capacitance Multiplier Employing CCII

A block diagram of a CCII is illustrated in Fig. 3. A CCII has three terminals, X, Y, and Z. The voltages and the currents relationship is given by

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ \alpha & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix}. \tag{3}$$

In a CCII+, the directions of I_X and I_Z are the same, and $\alpha = +1$. In a CCII−, the directions of I_X and I_Z are opposite each other, and $\alpha = -1$.

Grounded N-times capacitance multipliers constructed of a CCII are illustrated in Fig. 4. The circuit shown in Fig. 4(a) [20] employs a CCII+, which has $N-1$ times current gain at Z terminal, namely $\alpha = N - 1$ in Eq. (3). The circuit shown Fig. 4(b) [21] employs CCII−. In this circuit, the current gain at Z terminal is N, namely $\alpha = -N$ in Eq. (3).

4. Proposed Technique

4.1 Floating Capacitance Multiplier

Figure 5 illustrates the proposed floating capacitance multiplier. This circuit is constructed of an MOCCII, which is realized by combining CCII+ and CCII−. The proposed circuit structure is simpler than any conventional floating capacitance multiplier based on a CCII or a similar block derived from a CCII such as a DVCC and so on.

In this circuit, the currents I_A and I_B are expressed as

$$I_A = I_C + (N-1)I_C = NI_C \tag{4}$$

$$I_B = NI_C \tag{5}$$

where I_C is the current flow through the capacitor C. The impedance of this circuit Z is expressed as

$$Z = \frac{V_A - V_B}{NI_C} = \frac{1}{sNC}. \tag{6}$$

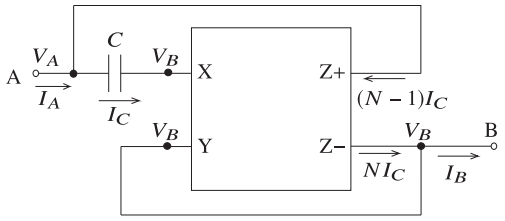


Fig. 5 Floating capacitance multiplier constructed of an MOCCII.

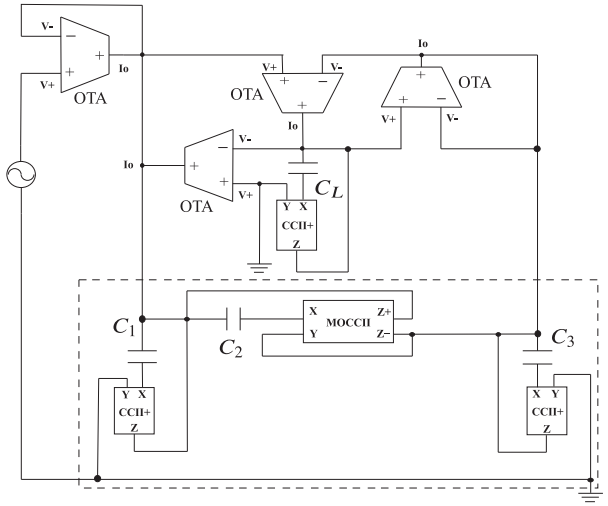


Fig. 6 Active 3rd order low-pass notch filter employing CCII based capacitance multipliers.

This shows that the floating capacitance C is multiplied by N times.

Figure 6 illustrates the configuration of the active low-frequency low-pass notch filter employing the CCII based capacitance multipliers. For the capacitor C_2, the proposed floating capacitance multiplier is used. The capacitance multipliers for the grounded capacitors C_1, C_3, and C_L are constructed by a CCII+ because the power dissipation is lower than that of a CCII− though the CCII− also can be employed.

4.2 Reduction of Capacitance Multipliers

The traditional usage of capacitance multipliers is that each capacitance is enhanced by a capacitance multiplier respectively, like Fig. 6. The second proposed technique is to scale the signal currents flowing a capacitor network employing fewer number of capacitance multipliers. The proposed circuit is obtained by replacing the broken-line part in Fig. 6 with the circuit shown in Fig. 7. In the proposed technique, CCII−s with N-times current gain factor at Z terminal are employed. It can be considered that the CCII−s scale the impedance of the entire network of capacitors.

Figure 8(a) illustrates a portion of the capacitor network that is cut out from Fig. 1. Current I_1 is expressed as

$$I_1 = s(C_1 + C_2)V_1 - sC_2V_2. \tag{7}$$

Figure 8(b) is a portion from Fig. 7. Current I_1 in this circuit

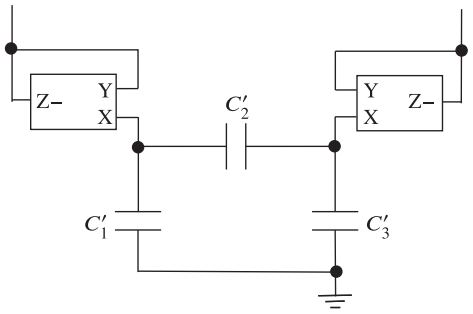
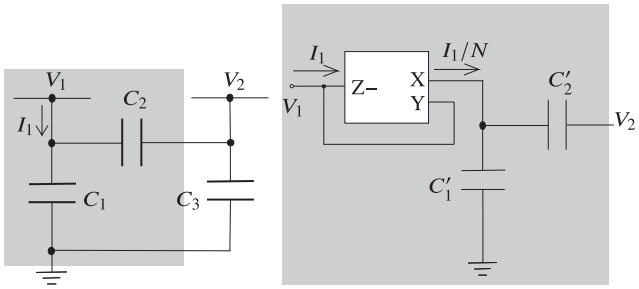


Fig. 7 Proposed technique to reduce capacitance multipliers.



(a) Part in Fig. 1 (b) Part in Fig. 7

Fig. 8 Corresponding part in capacitor network

is expressed as

$$I_1 = s(NC_1' + NC_2')V_1 - sNC_2'V_2. \tag{8}$$

Assuming

$$C_1 = NC_1' \tag{9}$$

$$C_2 = NC_2', \tag{10}$$

Eqs. (7) and (8) become equal. This means that small capacitances C_1' and C_2' can be enhanced by using a large scaling factor N. The relation of C_3 and C_3' is obtained similarly.

5. Simulation

5.1 Simulation Condition

The validity of the proposed techniques is confirmed by simulation of the 3rd order active low-pass filter using the simulation software LTspice. The simulated filter configurations are shown in Figs. 6 and 7. The filter specifications are shown in Sect. 2. The used transistor model is the 0.18 µm process BSIM3v1 full-parameter model. The supply voltage is 5 V. The circuit configurations of the CCII+ and the CCII− are illustrated in Figs. 9 and 10, respectively. The MOCCII is obtained by adding the Z− part surrounded by the broken line in Fig. 10 to the CCII+ shown in Fig. 9. The OTA shown in Fig. 2 is used for every filter simulation.

The gate width of all transistors was set to 1.8 µm. The gate length is also 1.8 µm, but only M6 in Fig. 2, which is used as a level shifter in the OTA, has a gate length of 18 µm. As shown by the gray boxes in Figs. 9 and 10, the number of

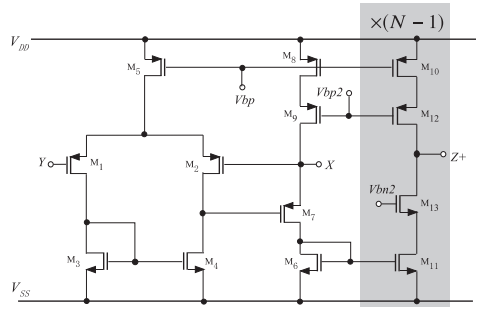


Fig. 9 Circuit configuration of CCII+.

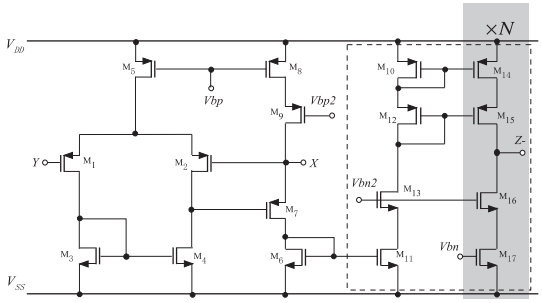


Fig. 10 Circuit configuration of CCII−.

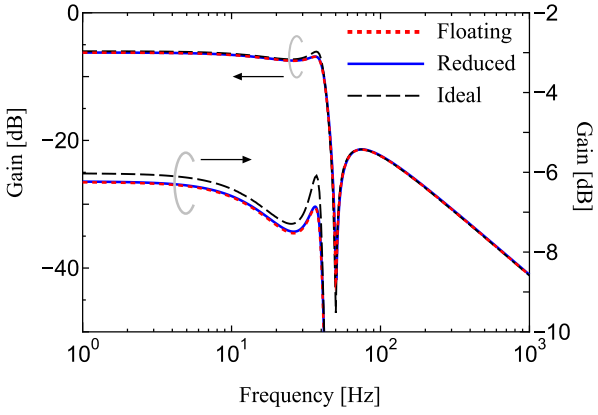


Fig. 11 Gain of frequency characteristics of low-pass notch filters.

parallel connections of transistors comprising the Z terminal is N-1 for the CCII+ and N for the CCII−.

5.2 Simulation Results

Figure 11 illustrates the gain of frequency characteristics with the enlarged view of the passband characteristics. The scaling factor N is set to 10. In this case, one-tenth of the values given by Eq. (2) is used. In this figure. the curve labeled 'ideal' represents the characteristic of the frequency-scaled passive LC ladder filter. Similarly, the curves labeled 'Floating' and 'Reduced' represent the characteristics of the circuit in Fig. 6 and one employing the proposed technique shown in Fig. 7, respectively.

Frequency tunability to compensate for active filter cut-off frequency variations caused by PVT variations was verified. The frequency responses of OTA with g_m values of 0.5, 1, and 2 times are illustrated in Fig. 12.

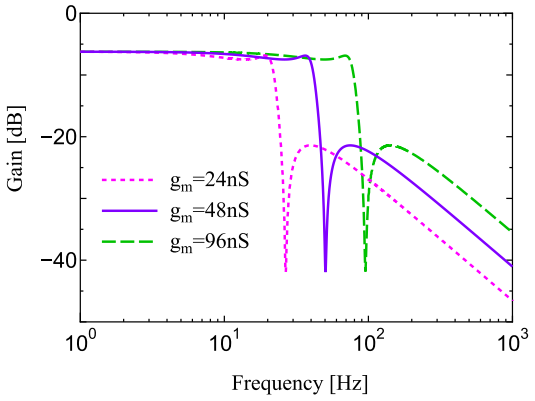


Fig. 12 Tuning cutoff frequency of low-pass notch filter.

Table 1 Primary result of filters.

	Ideal	Floating	Reduced
f_0	40 Hz	39.0 Hz	39.1 Hz
f_n	50 Hz	50.2 Hz	50.3 Hz
A_{min}	15.4 dB	15.2 dB	15.2 dB
A_{max}	1.25 dB	1.28 dB	1.26 dB
P	-	3.73 µW	2.14 µW

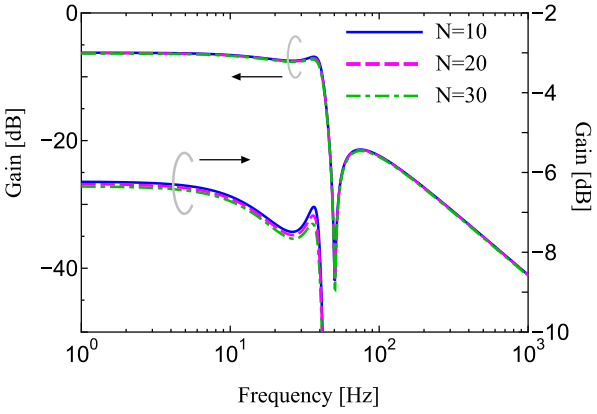


Fig. 13 Gain of low-pass notch filters with varying scaling factor.

Table 1 summarizes primary result values, where P is power consumption. It is shown that the proposed technique reduces much power consumption by 42.7% from the conventionally designed filter. Consequently, it is proved that the proposed reduce capacitance multiplier technique is useful and effective to reduce power consumption.

Figure 13 illustrates the frequency responses for the proposed circuit shown in Fig. 7 with varying scaling factor, $N = 10, 20$, and 30. This figure shows that the frequency response is generally good even when N is increased, but the overall gain gradually decreases. Table 2 shows the total capacitance value required to configure the filter and the overall power consumption of the filter at each value of N. It is confirmed that using the proposed method to increase the capacitance scaling factor reduces the overall capacitance

Table 2 Total capacitance and power consumption.

	$N = 10$	$N = 20$	$N = 30$
Capacitance	92.8 pF	46.4 pF	30.9 pF
Power	2.14 µW	3.22 µW	4.30 µW

value of the filter, but conversely increases the power consumption of the filter. Therefore, it is important to consider the balance between chip area and power consumption in the filter design.

6. Conclusion

In this letter, design consideration of integrated low-frequency low-pass notch filter to process biosignals in a field of biomedical engineering has been discussed. An elliptic filter that is a superior low-pass notch filter has floating capacitance. Its capacitance should be multiplied by capacitance multiplier for low-frequency application in consideration of suppression of limited chip area. This letter has presented two techniques. Firstly, a new floating capacitance multiplier has been proposed. The proposed circuit has simpler structure than the conventional circuits proposed until today. Further, it can be utilized to design not only elliptic filters but also other low-frequency circuits. Secondly, as only for the elliptic filters, a technique to reduce the number of capacitance multipliers has been proposed. These proposed techniques were examined by LTspice simulation, which shows effectiveness of the proposed techniques. In this study, the order of the filter was three (3rd order). The proposed techniques can be applied to higher-order filters, and further high effect can be obtained. Future works are expansion of the proposed techniques to higher order filter, confirmation of the effect, and chip implementation.

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