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FOREWORD

Special Section on Design Methodologies for System on a Chip

The application area of Information and Communication Technology has been extending from conventional computation/communication services to Internet of Things, Artificial Intelligence, robots, self-driving cars and beyond, which is supported by the constant evolution of LSI circuit and design technologies. In integrating a giga-scale system on a chip using nano-scale transistors for supporting sophisticated and complex ICT services, we are confronted with a lot of issues at each design stage such as design complexity, variation, power concentration, dependability, etc. This series of special sections started four years ago, and since then it has been providing good opportunities for researchers to publish and learn about their latest leading-edge works on design methodologies for System on a Chip.

For this special section, we have received 11 papers including 2 letters. We made thorough review and the paper selection meeting with all editorial committee members, and finally selected 6 papers including 2 letters.

On behalf of the guest editorial committee, I would like to express our sincere appreciation to all authors of papers submitted to this special section. I would also like to express my thanks to all members of the guest editorial committee and all reviewers for their work on judging the quality of papers. I should thank Professor Ittetsu Taniguchi from Osaka University, Yukihide Kohira from the University of Aizu, and Professor Hiroshi Tsutsui from Hokkaido University for their work as Guest Editors. Thanks are also due to the IEICE headquarters for the support to this special section.

Mineo Kaneko, Guest Editor-in-Chief

Mineo Kaneko *(Senior Member)* received Bachelor of Engineering, Master of Engineering, and Doctor of Engineering degrees in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1981, 1983, and 1986, respectively. From 1986 to 1996, he was a research associate, a lecturer and an associate professor with Tokyo Institute of Technology. In 1996, he moved to Japan Advanced Institute of Science and Technology (JAIST), Ishikawa, Japan, and he is currently a professor with Graduate School of Information Science, JAIST. His research interests include circuit theory, CAD for VLSI circuits, combinatorial optimization, etc. He is a member of IEEE, IEICE, IPSJ and ACM.