Soft-Error Resilient and Margin-Enhanced N-P Reversed 6T SRAM Bitcell

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PAPER
Soft-Error Resilient and Margin-Enhanced N-P Reversed 6T SRAM Bitcell

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SUMMARY   This paper describes a soft-error tolerant and margin-enhanced nMOS-pMOS reversed 6T SRAM cell. The 6T SRAM bitcell comprises pMOS access and driver transistors, and nMOS load transistors. Therefore, the nMOS and pMOS masks are reversed in comparison with those of a conventional bitcell. In scaled process technology, The pMOS transistors present advantages of small random dopant fluctuation, strain-enhanced saturation current, and small soft-error sensitivity. The four-pMOS and two-nMOS structure improves the soft-error rate plus operating margin. We conduct SPICE and neutron-induced soft-error simulations to evaluate the n-p reversed 6T SRAM bitcell in 130-nm to 22-nm processes. At the 22-nm node, a multiple-cell-upset and single-bit-upset SERs are improved by 34% and 51% over a conventional 6T cell. Additionally, the static noise margin and read cell current are 2.04× and 2.81× improved by leveraging the pMOS benefits.
key words: robust SRAM, soft error rate, neutron particle, single bit upset, multiple cell upset, nucleus reaction

1. Introduction

Process scaling continuously decreases an SRAM cell area by a factor of two in every technology generation, as presented in Fig. 1 [1], [2]. To scale CMOS transistors down to a 45-nm process or less, it is important to use compressive and tensile strain engineering for pMOS and nMOS, respectively, thereby increasing the drain current [3]. Particularly, for a pMOS, embedded SiGe (eSiGe) in a source and drain boosts its saturation current (I_{satp}). The strain engineering is thereby more effective against I_{satp} than that in an nMOS (I_{satn}). Current enhancement using eSiGe strain for the pMOS increases more effective with the process scaling: +30% and +45% in a 45-nm and 22-nm processes [3], [4]. Figure 2 shows the trend of the saturation current ratio of an nMOS to a pMOS (= I_{satn}/I_{satp}) along with a process node [5], [6]. The ratio becomes unity because I_{satp} is comparable with I_{satn} at a 22-nm node. In addition, the pMOS has less threshold voltage variation (V_{th} variation) because of lesser dopant fluctuation [7]. The standard deviation of the threshold voltage (σ_{Vth}) of the pMOS is 25% less than that of nMOS [7].

The nanoscaled integrated circuits are susceptible to particle-induced single event effects because of their low signal charge [8]. Multiple cell upsets (MCUs) are caused by a collection of charge produced by secondary ions in a
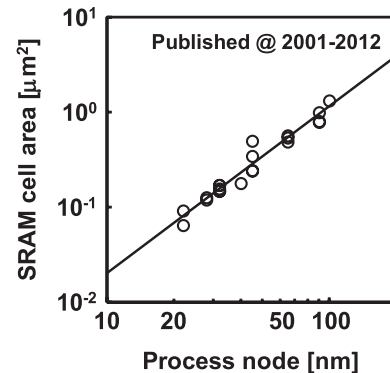

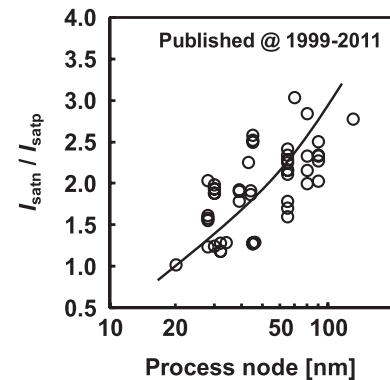**Fig. 1** Process scaling trends of 6T SRAM cell areas published during 2001–2012 [1], [2].

Fig. 2 Trend of saturation current ratios of I_{satn} to I_{satp} in 1999–2011 [3]–[6].

neutron-induced nuclear reaction. The ratio of the MCUs to single-event upsets (SEUs) is predicted to increase drastically in nanoscaled SRAMs [9]–[11]. Reportedly, the pMOS has less sensitivity to soft error effect than the nMOS [12]. The linear energy transfer threshold (LET_{th}) of the pMOS is 1/4 of that of the nMOS. Figures 3(a), 3(b) and 3(c) respectively show a schematic, a layout and read waveforms of the conventional six transistor (6T) SRAM cell. The conventional 6T cell comprises pMOS load transistors (PL0 and PL1), nMOS driver transistors (ND0 and ND1), and nMOS access transistors (NA0 and NA1). The shared nMOS diffusion area (ND and NA) is larger than that of the pMOS (PL). The large nMOS is strongly affected by radiation strikes. In addition, the sensitive nMOS nodes are in the same p-well in the horizontal direction. Horizontal up-
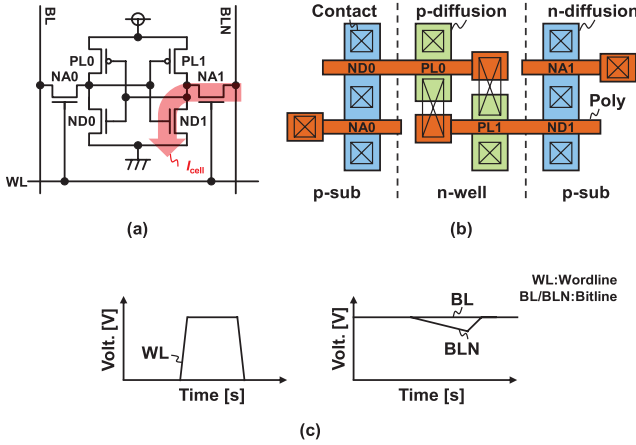
Fig. 3 (a) Schematic, (b) layout and (c) read waveforms of a conventional 6T SRAM cell. Cell current (I_{cell}) flows through nMOS access and driver transistors in read operation.

Fig. 4 (a) Schematic, (b) layout and (c) read waveforms of the proposed n-p reversed 6T SRAM cell. Cell current (I_{cell}) flows through pMOS load and nMOS access transistors in read operation.

sets can be incurred easily in the conventional 6T SRAM. An earlier report [13] describes that the nMOS-centered 6T SRAM cell can suppress the horizontal MCU by 67–98% because the horizontally adjacent nMOS nodes are separated by the n-well. However, the nMOS-centered 6T cell has area overhead because shared contacts cannot be applied [13].

As described above, the conventional 6T cell suffers from the shortcomings of the large V_{th} variation and the soft-error vulnerability in the nMOS driver transistors. To cope with these nMOS problems and to leverage the pMOS benefits, we propose using pMOS access and driver transistors instead: an n-p (nMOS-pMOS) reversed structure. A static noise margin, cell current, and soft-error tolerance are enhanced in the proposed n-p reversed 6T SRAM cell in future 22-nm node or advanced ones. Moreover, the horizontal MCU can be improved by the intrinsic nMOS-centered structure without area overhead.

The remainder of this paper is organized as follows. Section 2 presents the proposed n-p reversed 6T SRAM cell and setups for SPICE and soft-error simulations. In Sect. 3, simulation results are introduced with consideration of process scaling. Finally, Sect. 4 concludes this paper.

2. Proposed N-P Reversed 6T SRAM Cell and Simulation Setups

2.1 N-P Reversed 6T SRAM Cell

Figures 4(a), 4(b), and 4(c) respectively depict a schematic, a layout, and read waveforms of the proposed nMOS-pMOS (n-p) reversed 6T SRAM cell. The 6T cell consists of nMOS load transistors (NL0 and NL1), pMOS driver transistors (PD0 and PD1), and pMOS access transistors (PA0 and PA1). The number of transistors and the poly-gate alignment are similar, as depicted in Fig. 3(b), although the n- and p-diffusions are swapped. The shared contacts are applicable for both 6T cells. Therefore, the proposed cell has
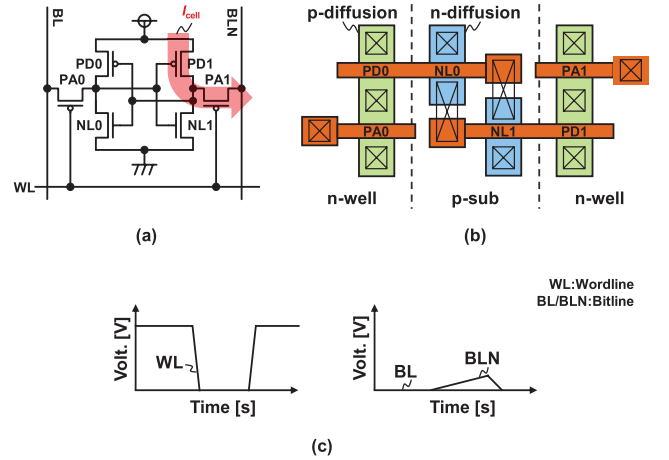
no area overhead over the conventional one. In a read operation, either bitline (BL or BLN in Fig. 4(a)) is pulled up by a cell current flowing through a pMOS access transistor. Generally, the read current of the proposed cell is degraded because I_{satp} is smaller than I_{satn}. However, as presented in Fig. 2, the saturation current ratio of I_{satn} to I_{satp} becomes smaller in the scaled process. Moreover, the random dopant fluctuation of the pMOS is less than that of the nMOS. Consequently, the cell current of the proposed cell will be larger than that of a conventional cell. This paper also investigates the breakpoint. The proposed cell decreases the soft-error rate because it has a 33% smaller nMOS diffusion area than a conventional cell. Moreover, the intrinsic nMOS-centered structure has horizontal-MCU resilience, which is similar to a previous study [13]. The horizontal pitch of the sensitive nMOS nodes is larger than those of conventional ones. Horizontally adjacent nMOSes do not share the same p-substrate.

2.2 Simulation Setups for HSPICE and PHITS

Table 1 presents simulation parameters for the HSPICE circuit simulator and a particle transport code (PHITS) [14]. The supply voltage (VDD) and equivalent oxide thickness (EOT) for each process node are referred from ITRS 2001–2011 [15]. The standard deviations of the threshold voltages for nMOS and pMOS (σ_{Vthn} and σ_{Vthp}) are normalized at the 65-nm node with the Stalk equation ($\sigma_{Vth} \propto EOT/\sqrt{}$ (channel area: width × length)) [16]. At the 65-nm node, σ_{Vthn} and σ_{Vthp} are 40 mV and 30 mV, respectively, for the minimum transistors, as derived from measurements of test chips [7]. The saturation current ratios (I_{satn}/I_{satp}) and cell area are obtained using the fitting curves in Figs. 2 and 1. The critical charge is calculated at each node according to related reports [17], [18].

Figure 5 shows the circuit setup for HSPICE to estimate static noise margins (SNMs) of the conventional and proposed cells. The SNM is defined as a minimum square

Table 1   Parameters in HSPICE and PHITS simulations.

Process node [nm]	VDD[*1] [V]	EOT[*1] [Å]	σ_{Vthn}[*2] [mV]	σ_{Vthp}[*2] [mV]	I_{sat} ratio[*3] (I_{satn} / I_{satp})	Cell area[*4] [μm^2]	Critical[*5] charge [fC]
22	0.9	12	83.8	62.9	1.01	0.0813	0.224
32	1.0	15	64.6	48.5	1.40	0.1562	0.285
45	1.0	19	51.2	42.9	1.84	0.2830	0.430
65	1.1	21	40.0	30.0	2.26	0.5369	0.793
90	1.2	24	32.3	24.2	2.70	0.9465	1.700
130	1.2	27	25.7	19.3	3.08	1.7960	3.300

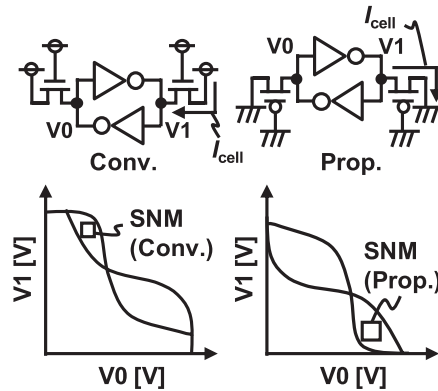[*1][10], [*2][7,11], [*3]Fitting in Fig. 2, [*4]Fitting in Fig. 1, [*5][17,18]

Fig. 5   Circuit setup for Static Noise Margin (SNM) and I_{cell} estimation. The read margin is defined as a minimum square in butterfly curves.
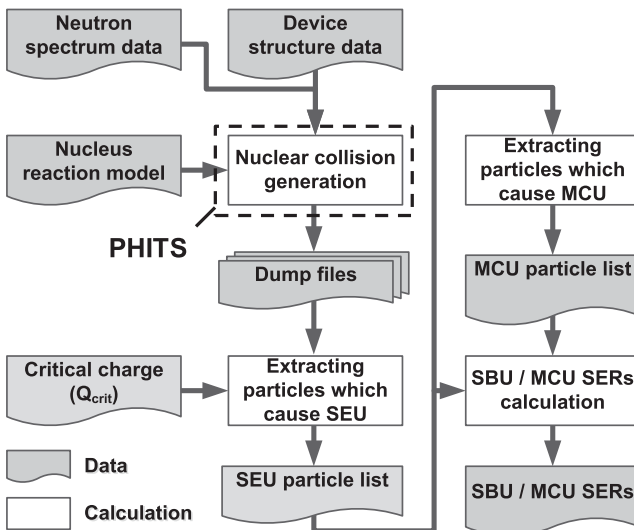

Fig. 6   Flow chart of the soft-error rate simulator [20] using PHITS [9].

Fig. 7   Cosmic-ray neutron flux normalized to ground level in New York City. Flux is calculated with EXPACS [16].
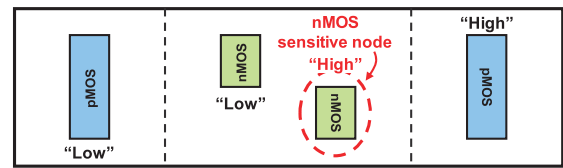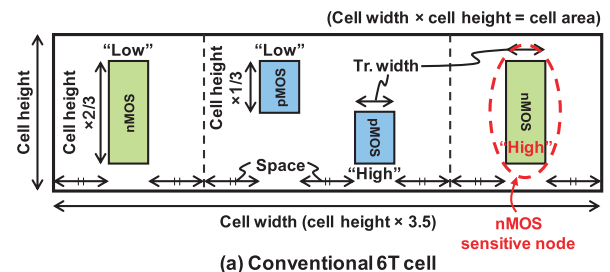
Fig. 8   Models of SRAM cell width, height, and positions of sensitive nodes in 22-nm to 130-nm processes using parameters in Table 2.

Table 2   Size and position parameters in Fig. 8 for PHITS simulations.

	Process node [nm]					
	22	32	45	65	90	130
Cell area [μm^2]	0.081	0.156	0.283	0.537	0.947	1.796
Cell height [μm]	0.152	0.211	0.284	0.392	0.520	0.716
Cell width [μm]	0.533	0.739	0.995	1.371	1.820	2.507
Tr. width [μm]	0.044	0.064	0.090	0.130	0.180	0.260
Space [μm]	0.051	0.069	0.091	0.122	0.157	0.210

in butterfly curves in Monte Carlo simulations (20 K trials) [19]. Furthermore, the cell current (I_{cell}) is taken from the minimum one by the SPICE Monte Carlo simulations, which reflects the readout speed.

Figure 6 illustrates a flow chart of our neutron-induced soft error simulator [20] using PHITS. The input data for PHITS are neutron spectrum data, device structure data, and nucleus reaction models.

The cosmic-ray neutron spectrum is calculated using an Excel-based Program for calculating Atmospheric Cosmic-ray Spectrum (EXPACS) [21], as shown in Fig. 7.
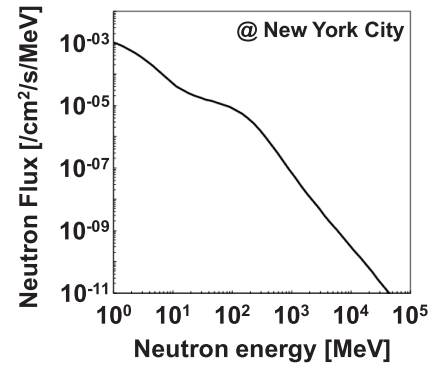
The device structure includes the cell property (width, height, and position of sensitive nodes), a cell-to-cell pitch in a cell array, and data patterns. The cell height, width, and position of the sensitive nodes are modeled as presented in Fig. 8. The ratio of the cell height to the cell width is set as 3.5. Each transistor width is doubled from the process node to suppress threshold voltage variation. The diffusion area is derived from the transistor width and the cell height. The clearances between diffusion edged are all equal. The parameters are presented in Table 2.

Figures 9(a)–9(d) respectively show four data patterns in a conventional memory cell array, with checkerboard
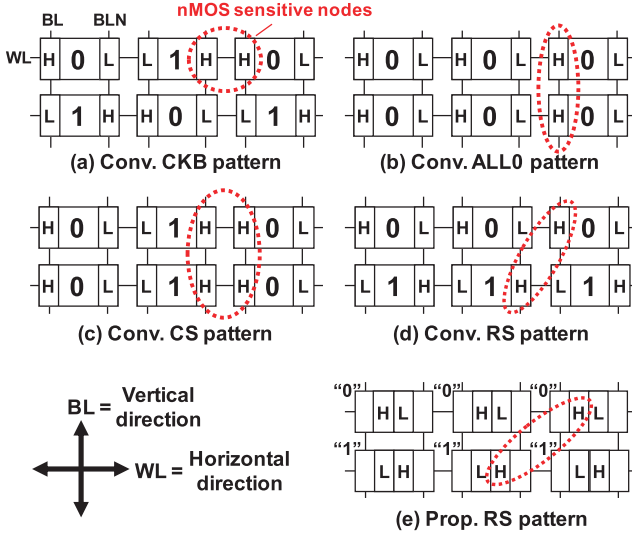
Fig. 9 Data patterns for soft-error evaluation: (a) checker board (CKB), (b) all 0 (ALL0), (c) column stripe (CS), (d) row stripe (RS) patterns in the conventional SRAM cell array and (e) RS patterns in the proposed one. The red circles show nMOS sensitive nodes.

(CKB), all 0 (ALL0), column stripe (CS), and row stripe (RS) patterns. The red circles show nMOS sensitive nodes. As described in Sect. 1, the nMOS nodes share the same p-substrate in the horizontal direction, which possibly causes horizontal MCUs. However, the n-p reversed 6T cell has the nMOS transistors in the center of the cell, as shown in Fig. 9(e). The structure obtains the horizontal-MCU tolerance as well as the previous nMOS-centered 6T cell [13].

As a nucleus reaction model, the intra-nuclear cascade (INC) model [22] and the generalized evaporation model (GEM) [23] are used with a nucleus database: Japanese Evaluated Nuclear Data Library (JENDL-4.0) [24].

PHITS simulates the nucleus reaction and particle transportation. In the simulation, dump files are exported. They include the secondary ion particle states: atomic weight, nucleus reaction point (X, Y, Z), velocity vector (dX, dY, dZ), and energy per nucleon. If a particle crosses the surface of the sensitive volume, then the particle state at the cross point is also exported to the dump file. The deposit energy ($E_{deposit}$) is calculated with the dump files in the respective sensitive nodes.

The deposit charge ($Q_{deposit}$) is calculated using the following equation, in which e is the elementary charge.

$$Q_{deposit} \text{ [C]} = \frac{e}{3.6} \times E_{deposit} \text{ [eV]} \tag{1}$$

When a secondary particle deposits more than a critical charge (Q_{crit}) to at least one memory cell, that particle is classified as a single-event-upset (SEU) particle. Finally, single-bit-upset and multiple-cell-upset soft-error rates (SBU and MCU SERs) are calculated at every SEU particle event.
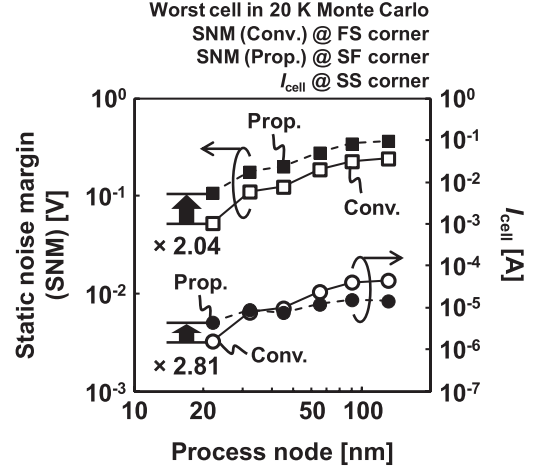

Fig. 10 SNM and I_{cell} comparisons between conventional and proposed cells.

3. Simulation Results

3.1 Static Noise Margin (SNM) and Cell Current (*Icell*) Estimations with HSPICE

The SNMs of the conventional and proposed 6T SRAM cells are calculated using the 20 K Monte Carlo HSPICE simulations at the worst process corners: The FS (nMOS = Fast; pMOS = Slow) corner for the conventional cell and the SF corner for the proposed cell. The I_{cell} is calculated at the SS corner. Figures 10 shows that the SNM and I_{cell} of the worst cell are decreasing continuously with process scaling attributable to the reduced VDD and the increased σ_{Vth}. The proposed cell, however, has a greater SNM and I_{cell} because the proposed cell has pMOS access and driver transistors and their σ_{Vthp} is smaller than the σ_{Vthn} in the conventional one. The SNM of the proposed cell is larger at every node and is 2.04 times as large at the 22-nm node. The I_{cell} in the proposed cell is larger than that in the conventional one at the 32-nm and less nodes and is 2.81 times as large at the 22-nm node. Simulation results show that the proposed n-p reversed 6T cell achieves greater read stability and faster readout operation than the conventional one in the scaled process.

3.2 Neutron-Induced Soft-Error Rate Calculation with PHITS

Figure 11 shows neutron-induced soft-error simulation results obtained using CKB, ALL0, CS, and RS patterns. Although the critical charge is decreasing, the SBU SER is also decreasing with process scaling thanks to the smaller critical area. The MCU SER exhibits a similar tendency at the 65-nm and less nodes. The proposed n-p reversed cell has 50% smaller nMOS diffusion area in our definition. Therefore, its SBU and MCU SERs are reduced respectively by 11–51% and 34–70% at the 22-nm node. Particularly for
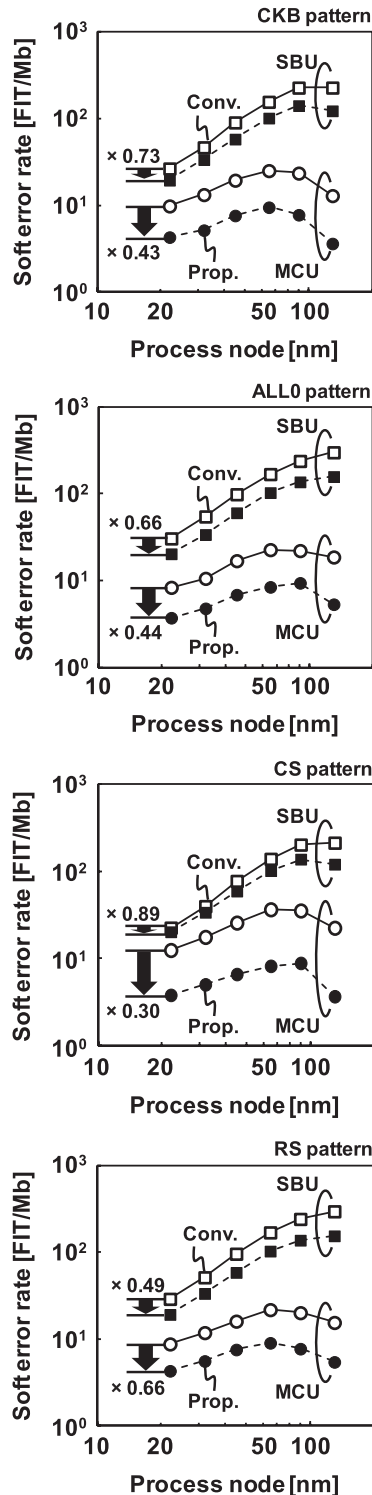
Fig. 11 SBU and MCU SERs of conventional and proposed cells in the CKB, ALL0, CS and RS patterns.

the column stripe pattern, the MCU SER is improved by 70% (but the SBU SER is decreased by only 11%) because nMOS diffusions in the conventional cells share the same p-substrate in the vertical direction and vertical MCUs occur easily. However, in the row stripe pattern, the MCU SER

improvement is the smallest, 34% (but the SBU SER improvement is the largest, 51%), because the distance from a sensitive nMOS node to another in the conventional cells is the longest among the four patterns.

Figures 12(a)–12(d) show MCU error patterns defined in this paper: (a) horizontal, (b) vertical, (c) angle, and (d) other MCU patterns. The horizontal MCU includes upsets in a single raw occurred in a wordline (= horizontal direction). The vertical MCU includes upsets in a single column occurred in a bitline (= vertical direction). The angle MCU includes horizontal MCU and more upsets. The other MCUs are categorized in the other type shown in Fig. 12(d). Figure 13 shows the normalized MCU SER (total MCU in the conventional SRAM equals 100%). The MCU SER including horizontal upsets (horizontal and angle MCUs) is improved by 91.8–97.9% using the n-p reversed 6T cell in CKB and CS patterns because horizontal upsets easily occurs in those patterns in the conventional cell array.

4. Conclusion

An n-p reversed 6T SRAM cell was proposed to improve the read stability, readout speed, and soft-error tolerance. Toward an advanced process node, a pMOS saturation current is enhanced with embedded SiGe strain technology, and a standard deviation of a pMOS threshold voltage is intrinsically smaller than that of nMOS. We leveraged the pMOS. The pMOS access and driver transistors are used in the proposed cell. Therefore, the soft-error sensitive nMOS transistors are centered on a shared p-substrate, which obviates the area overhead, extra mask, or design cost. At a 22-nm process, a static margin and cell current are improved, respectively, by factors of 2.04 and 2.81. Neutron-induced soft-error rates of the conventional proposed cells were investigated using the PHITS-based simulator. The proposed 6T cell improves the SBU and MCU soft-error rates by 11–51% and 34–70%, respectively, because the proposed n-p reversed cell has a 33% smaller nMOS diffusion than the conventional one and reduces a collected charge induced by a secondary ion. Moreover, the MCU SER, including horizontal upsets (horizontal and angle MCUs), is improved by 91.8–97.9% in CKB and CS patterns using the n-p reversed 6T cell.

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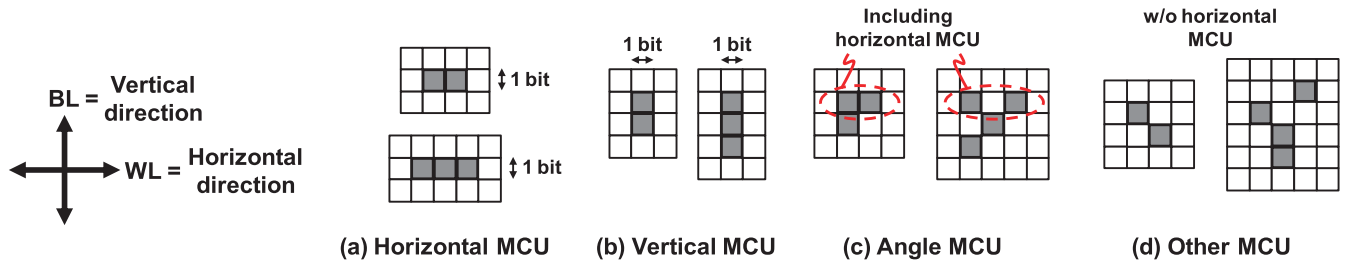
Fig. 12 MCU error patterns: (a) horizontal, (b) vertical, (c) angle, and (d) other MCUs.
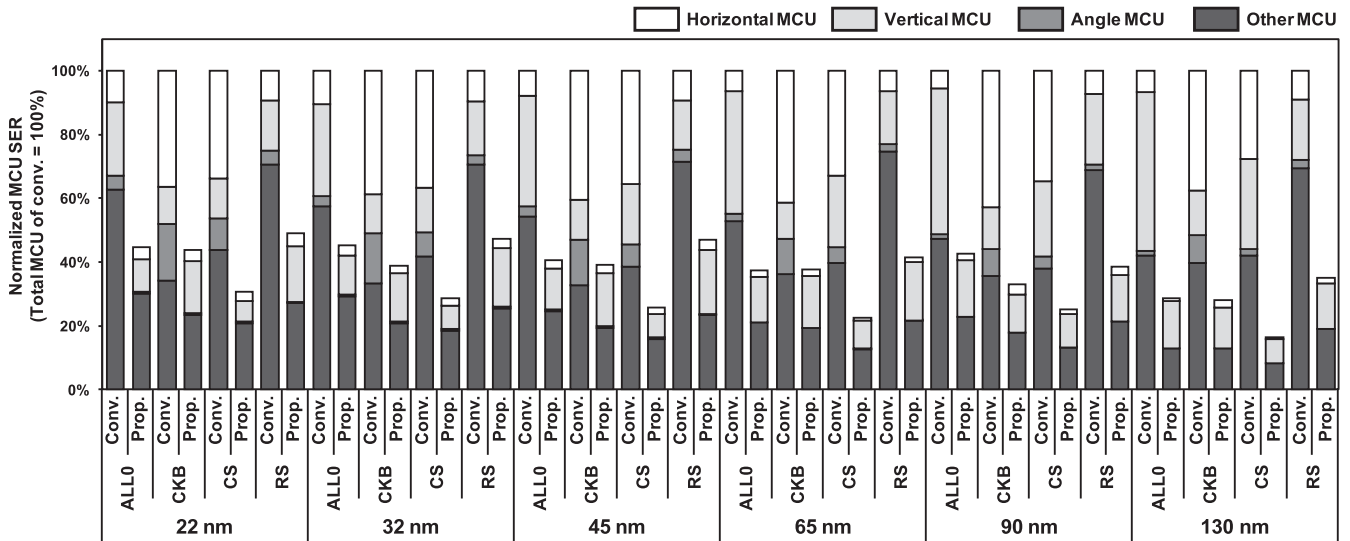

Fig. 13 Normalized MCU SERs at 22-nm to 130-nm process nodes.

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