# Optimized Adder Cells for Ternary Ripple-Carry Addition 

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#### Abstract

SUMMARY The unique characteristic of Ternary ripple-carry addition enables us to optimize Ternary Full Adder for this specific application. Carbon nanotube field effect transistors are used in this paper to design new Ternary Half and Full Adders, which are essential components of Ternary ripple-carry adder. The novel designs take the sum of input variables as a single input signal, and generate outputs in a way which is far more efficient than the previously presented similar structures. The new ripple-carry adder operates rapidly, with high performance, and low-transistor-count. key words: Ternary Full Adder, Ternary Half Adder, Ternary Ripple-Carry Adder, CNTFET, nanoelectronics


## 1. Introduction

While analog circuits are very fast, digital Binary circuits have the advantage of higher noise tolerance. Ternary logic makes a balance in between. This is the reason why it has attracted a great interest among VLSI designers. It benefits from higher computational speed compared with Binary logic, and an acceptable noise margin at the same time [1]. It also reduces the amount of wires inside and outside the chip bringing about higher integration level [2]. It is the most promising candidate as the replacement of Binary logic.

In [3], S.L. Hurst states that an e-based system (e = 2.718...) results in the most efficient implementation of switching systems. However, due to the limitations of hardware implementation, designers are obliged to use the natural numbers as the radices for computations. Therefore, amongst different Multiple-Valued Logics (MVL), Ternary is the most effective which leads to less product cost and also less complexity than Binary [3].

To make Ternary logic applicable, high-performance logic gates and arithmetic circuits need to be first realized. Addition is one of the most fundamental arithmetic units. Other operations such as subtraction, multiplication, and division are on the basis of this essential component. Therefore, it is crucial to have a fast, low-power, and area-efficient adder block. Ripple-carry addition is a well-known approach for computing the sum of two numbers [4].

In this paper, new Ternary 1 -bit adder cells are first

[^0]proposed. They are presented based on a method which provides more circuit robustness and higher performance in comparison with previous similar works. Afterwards, the single-bit Ternary Full Adder is specifically optimized for Ternary addition. The adder cells are cascaded to form a Ternary Ripple-Carry Adder (RCA). Carbon Nanotube Field Effect Transistors (CNTFET) [5] are utilized to implement the new structures. This new technology has the advantage of more flexibility in adjusting the desired threshold voltage when compared with the current MOSFET technology. This unique feature is highly appreciated in multi- $V_{t}$ MVL circuitry [6].

The rest of the paper is organised as follows: The previously presented adders are reviewed in Sect. 2. Section 3 introduces the new 1-bit Ternary adders. The primary simulation results are brought in Sect. 4. Ternary ripple-carry addition is discussed in Sect. 5. Finally, Sect. 6 concludes the paper.

## 2. Review of Previous Works

Ternary Half and Full Adders have been presented in [7] and [8] based on a concept which takes the sum of input variables as a single input signal, and generates the outputs in a parallel manner. This method of circuitry reduces transistor count dramatically compared to the regular structures presented in [9]-[11]. Table 1 and Table 2 show the truth table of Ternary Half Adder (THA) and Ternary Full Adder (TFA), respectively. Depending on what the sum of inputs ( Vin ) is, a special path connects the output node to the appropriate voltage source (Power supply or Ground). When $\Sigma$ in changes, the previous path disconnects and another path links the output node to the new voltage level. Both pulldown and pull-up networks have to be switched on in case the output equals the logic value ' 1 '.

The novel Ternary adders, which will be introduced in the next section, are also established upon a comparable method. Therefore, the previous adders are first reviewed in order to study and survey the characteristics, advantages, and drawbacks of each design in detail. This will be an introductory explanation of the new method as well.

### 2.1 Previous Ternary Half Adders

Figure 1 shows how the Ternary Half Adder presented in [7] generates the output signals (Sum and Carry). In this architecture, there are seven different paths connected to the

Table 1 Truth table of Ternary Half Adder (THA).

| Sin | Carry | Sum |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 0 | 2 |
| 3 | 1 | 0 |
| 4 | 1 | 1 |

Table 2 Truth table of Ternary Full Adder (TFA).

| Lin | Carry | Sum |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 0 | 2 |
| 3 | 1 | 0 |
| 4 | 1 | 1 |
| 5 | 1 | 2 |
| 6 | 2 | 0 |



Fig. 1 The core idea of THA presented in [7].
output node Sum. Each one charges or discharges the output node depending upon the sum of input variables ( Ein ). Two separate paths are required to connect the output node (Sum) to both $V_{d d}$ and Ground at the same time whenever it is equal to the logic value ' 1 '. Voltage divider elements (Resistors) perform voltage division and the result is $\frac{V_{d d}}{2}$, which represents the logic value ' 1 ' in digital electronics [12].

There is a special path for each value of $\Sigma$ in (Fig. 1 and Table 1). The times when paths are in the connecting state are also indicated in Fig. 1. Some transistors switch on above a specific value of $\Sigma \mathrm{in}$. Some others are ON if $\Sigma$ in is beneath a particular value (Fig. 1). Four inverters with different turning points are supplemented, so that the requirement of proper switching activity of the transistors within the main part (situated on the paths) is fulfilled. The appropriate location of the p-type and the n-type transistors are also because of the existence of these inverters.

The proposed THA in [7] is depicted in Fig. 2. Two capacitors perform the initial voltage division between the input signals, and the result is $\frac{\Sigma i n}{2}$. Capacitors are selected as voltage dividers in the first stage so that continuous current flow is eliminated [13]. On the other hand, resistors are better candidates to divide voltage in the main part, where the flow of current satisfies cell drivability. Both voltage divider elements (capacitors and resistors) are implemented by transistors. The whole structure has 28 transistors.


Fig. 2 THA presented in [7].


Fig. 3 The core idea of THA presented in [8].


Fig. 4 THA presented in [8].

Unlike the first design, the paths of the second structure presented in [8] are combined together for different values of $\Sigma \mathrm{in}$. Figure 3 reveals the logic behind this THA. When $\Sigma \mathrm{in}=0$, the output node (Sum) is connected to the ground through the pull-down network. When Ein increases from 0 to 1 , still the pull-down network has to be ON. Therefore, the previous path is kept unchanged. Another path within the pull-up network is established, and hence the output becomes ' 1 '. Subsequently, when Ein increases from 1 to 2, it is adequate to cut the pull-down path off. Therefore, the output node is only connected to the power supply.

Figure 4 shows the THA which has been proposed in [8]. In order to improve the driving power, inverted outputs ( $\overline{S u m}$ and $\overline{\text { Carry }}$ ) are first generated. Then, two Ternary inverters are added to obtain the non-inverted outputs. The technique of combining different paths has led to fewer transistors, which are 26.


Fig. 5 TFA presented in [7].


Fig. 6 TFA presented in [8]

### 2.2 Previous Ternary Full Adders

Ternary Full Adder takes three Ternary digITs (TIT) and returns two output signals which are the sum of the input variables. In [7] and [8], TFA cells have also been presented (Fig. 5 and Fig. 6). The one which has been introduced in [7] follows the same approach of THA, whereas the one presented in [8] is an indirect design. It consists of two cascaded THAs as well as a carry generator circuit which produces the final carry. The first one has 41 , and the second has 64 transistors.

## 3. New Single-Bit Ternary Adders

New Ternary adder cells are based on a similar idea introduced in [7], except that the main parts generate Binary signals instead of Ternary ones. The schema of the utilized method in this paper is depicted in Fig. 7.

There are two definitions of a Ternary function other than the Standard one. They are known as Positive (+) and Negative ( - ). The Standard Ternary is the average of the others (Eq. (1)). Two threshold sensitive circuits (Fig. 7) generate Positive $\overline{O u t}(\overline{O u t}+)$ and Negative $\overline{O u t}(\overline{O u t}-)$. Then, Binary inverters convert them to Out+ and Out-. Eventually, two transistors perform voltage division, and the Standard Ternary output (STOut) is achieved.

$$
\begin{equation*}
S \text { TOut }=\frac{(\text { Out }-)+(O u t+)}{2}=\frac{\overline{(\overline{O u t}+)}+\overline{(\overline{O u t}-)}}{2} \tag{1}
\end{equation*}
$$

### 3.1 New Ternary Half Adder

Table 3 shows the Standard, Negative, and Positive values


Fig. 7 The basic schema of the proposed method.

Table 3 Truth table of the Standard, Negative, and Positive Ternary definitions of Sum in THA.

| in | Sum | Sum - | Sum + | $\overline{\text { Sum }}+$ | $\overline{\text { Sum }}-$ | $\overline{\text { Sum }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 2 | 2 | 2 |
| 1 | 1 | 0 | 2 | 2 | 0 | 1 |
| 2 | 2 | 2 | 2 | 0 | 0 | 0 |
| 3 | 0 | 0 | 0 | 2 | 2 | 2 |
| 4 | 1 | 0 | 2 | 2 | 0 | 1 |


(a)

(c)

(b)

(d)

Fig. 8 Threshold Sensitive sub-circuits (THA), (a) Generates $\overline{S u m}-$, (b) Generates $\overline{S u m}+$, (c) Generates $\overline{S u m}-$ with correct locations of transistors, (d) Generates $\overline{S u m}+$ with correct locations of transistors.
of the output Sum in THA. Two threshold sensitive subcircuits are required to generate the mid-outputs ( $\overline{S u m}-$ and $\overline{S u m}+$ ), which are Binary signals. Therefore, they are either connected to the ground or to the power supply.

The following brief explanations illustrate how the first threshold sensitive sub-circuit creates $\overline{S u m}-$ (Fig. 8 (a)):
a) $\operatorname{\sum in}=0: T_{1}$ is $\mathrm{ON}, T_{3}$ is $\mathrm{ON}, T_{5}$ is ON , The rest are OFF $\rightarrow \overline{S u m}-={ }^{\prime}{ }^{\prime}$ '
b) $\operatorname{\Sigma in}=1 \mid 2: T_{1}$ switches OFF, $T_{2}$ switches $\mathrm{ON}, T_{3}$ is still $\mathrm{ON} \rightarrow \overline{\mathrm{Sum}}-=$ '0'
c) $\operatorname{\Sigma in}=3: T_{3}$ switches OFF, $T_{4}$ switches ON, $T_{5}$ is still $\mathrm{ON} \rightarrow \overline{S u m}-=$ ' 2 '
d) $\operatorname{\Sigma in}=4: T_{5}$ switches OFF, $T_{6}$ switches ON $\rightarrow \overline{S u m}-=$ ' 0 '

This is how the second sub-circuit works (Fig. 8 (b)):
a) $\operatorname{Ein}=0 \mid 1: T_{1}$ is $\mathrm{ON}, T_{3}$ is ON , The rest are $\mathrm{OFF} \rightarrow$ $\overline{S u m}+={ }^{\prime}$ ' $^{\prime}$
b) $\operatorname{\Sigma in}=2: T_{1}$ switches OFF, $T_{2}$ switches ON, $T_{3}$ is still $\mathrm{ON} \rightarrow \overline{\mathrm{Sum}}+={ }^{\prime} 0$ '
c) $\operatorname{\Sigma in}=3 \mid 4: T_{3}$ switches OFF, $T_{4}$ switches ON $\rightarrow \overline{S u m}+=$ '2'

In fact, a p-type transistor is responsible for cutting a path off. Its counterpart, an n-type transistor, sets a path up. The correct functionality depends on the proper adjustment of the threshold voltage of each transistor. Threshold voltages are determined by the fact that above a specific value of $\Sigma \mathrm{in}(\alpha)$, an nCNTFET switches on and a pCNTFET switches off (Fig. 8). The following description illustrates how the Threshold (TH) parameter is settled:
a) $\sin >\alpha$ : (nCNTFET is ON$) T H_{n}=\alpha+0.5$
b) $\sin <\alpha$ : $(\mathrm{pCNTFET}$ is ON$) T H_{p}=\alpha-0.5$

The first parameter (TH) determines the time when a transistor switches. The second parameter, Switching Threshold (ST), is calculated by Eq. (2) or Eq. (3) when the target circuit is THA or TFA, respectively. The initial voltage division in THA(TFA) is between two (among three) input signals.

$$
\begin{align*}
& S T_{T H A}=\frac{T H_{n \mid p}}{2}  \tag{2}\\
& S T_{T F A}=\frac{T H_{n \mid p}}{3} \tag{3}
\end{align*}
$$

The third parameter, $V_{S T}$, is a fraction of $\mathrm{V}_{d d}$ (Eq. (4)). It indicates the threshold voltage of the n-type (Eq. (5)) and the p-type (Eq. (6)) transistors.

$$
\begin{align*}
& V_{S T}=\frac{S T_{T H A \mid T F A} \times V_{d d}}{2}  \tag{4}\\
& V_{t, n}=V_{S T}  \tag{5}\\
& \left|V_{t, p}\right|=V_{d d}-V_{S T} \tag{6}
\end{align*}
$$

The diameter of CNT ( $\mathrm{D}_{C N T}$ ) is a function of chiral vectors ( $\mathrm{n}, \mathrm{m}$ ), which are nonnegative integer numbers (Eq. (7)) [10]. Finally, $\mathrm{D}_{C N T}$ sets the threshold voltage of the transistor (Eq. (8)) [6], [10].

$$
\begin{equation*}
D_{C N T}(n m) \approx 0.0783 \times \sqrt{n^{2}+m^{2}+n \times m} \tag{7}
\end{equation*}
$$



Fig. 9 The proposed THA.


Fig. 10 The proposed TFA.

$$
\begin{equation*}
V_{t} \approx \frac{0.43}{D_{C N T}(n m)} \tag{8}
\end{equation*}
$$

There are some misplaced $n(p)$-type transistors in the pull-up(pull-down) network. The threshold related to the ones which are put in the wrong place is between two and three $(2<\Sigma \mathrm{in}<3)$. An inverter with turning point of 2.5 , the average, is added to the sub-circuits (Fig. 8 (c) and 8 (d)) to replace the misplaced transistors with the correct ones. The proposed THA is depicted in Fig. 9, where $\mathrm{D}_{C N T}$ and

Table 4 Truth table of the Standard, Negative, and Positive Ternary definitions of Sum in TFA.

| Ein | Sum | Sum - | Sum + | $\overline{\overline{S u m}}+$ | $\overline{S_{u m}}-$ | $\overline{\text { Sum }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 2 | 2 | 2 |
| 1 | 1 | 0 | 2 | 2 | 0 | 1 |
| 2 | 2 | 2 | 2 | 0 | 0 | 0 |
| 3 | 0 | 0 | 0 | 2 | 2 | 2 |
| 4 | 1 | 0 | 2 | 2 | 0 | 1 |
| 5 | 2 | 2 | 2 | 0 | 0 | 0 |
| 6 | 0 | 0 | 0 | 2 | 2 | 2 |

the number of nanotubes (\#Tubes) are indicated. The latter is set suitably with the aim of minimizing the Power-Delay Product (PDP), based on the transistor sizing procedure presented in [14]. The entire circuit has 24 transistors.

### 3.2 New Ternary Full Adder

The same method is employed to form a new Ternary Full Adder, depicted in Fig. 10. The values of Sum+ and Sumin TFA are shown in Table 4, where there are two more rows ( $\Sigma \mathrm{in}=5$ and $\Sigma \mathrm{in}=6$ ) in comparison with THA. In TFA, the highest boundary of $\Sigma \mathrm{in}$ is six. Transistor count is 35 for the proposed design. It has six fewer transistors than the structure presented in [7], and 29 fewer ones than the design given in [8].

## 4. Simulation Results

All THAs are simulated by Synopsys HSPICE with 32nm CNTFET technology [15] in three different power supply voltages and 100 MHz operating frequency at room temperature. Input Ternary buffers [7] as well as 2 fF load capacitors are also considered to measure performance parameters in a realistic simulation setup. Delay, average power consumption, and PDP of THAs are reported in Table 5. The best results are highlighted in boldface. In this paper, PDP is the product of the average power consumption and the maximum delay. It is an important evaluation factor which makes a balance between the power and the delay.

Other than these three important efficiency parameters, total width of the adder cells is also calculated (Eq. (9)) as a reasonable approximate criterion of area competence. Transistor width of a CNTFET can be calculated by Eq. (10) [16], in which $W_{\text {min }}$ is the minimum width of the gate, and Pitch is the distance between the centres of two adjacent CNTs. The latter is 20 nm for all transistors, except for the ones that implement capacitors $($ Pitch $=4 n m)$.

$$
\begin{align*}
& \text { TotalCellWidth }=\sum_{i} \operatorname{Width}\left(T_{i}\right)  \tag{9}\\
& W_{\text {gate }} \approx \operatorname{Max}\left(W_{\text {min }}, \# \text { Tubes } \times \text { Pitch }\right) \tag{10}
\end{align*}
$$

Since the static power dissipation is a large portion of power consumption in Ternary logic, average static power is also measured separately in 0.7 V power supply.

Simulation results demonstrate the superiority of the

Table 5 Simulation results of THAs.

| Design | Proposed | Previous [7] | Previous [8] |
| :---: | :---: | :---: | :---: |
| \#Transistors | $\mathbf{2 4}$ | 28 | 26 |
| Total Width $(\mathrm{nm})$ | 7520 | $\mathbf{6 2 2 0}$ | 6820 |
| Static Power $(\mu W)$ | 1.5095 | $\mathbf{1 . 1 4 5 8}$ | 4.9001 |
| $V_{d d}=0.75 \mathrm{~V}$ |  |  |  |
| Delay $(\mathrm{psec})$ | $\mathbf{5 2 . 0 8 9}$ | 133.40 | 66.122 |
| Power $(\mu W)$ | 4.0476 | $\mathbf{3 . 2 7 4 1}$ | 8.4359 |
| PDP $(\mathrm{fJ})$ | $\mathbf{0 . 2 1 0 8}$ | 0.4368 | 0.5578 |
| $V_{d d}=0.7 \mathrm{~V}$ |  |  |  |
| Delay $(\mathrm{psec})$ | $\mathbf{6 0 . 6 5 4}$ | 156.80 | 69.320 |
| Power $(\mu W)$ | 2.3485 | $\mathbf{1 . 9 7 6 6}$ | 5.7591 |
| PDP $(\mathrm{fJ})$ | $\mathbf{0 . 1 4 2 4}$ | 0.3099 | 0.3992 |
| $V_{d d}=0.65 V$ |  |  |  |
| Delay $(\mathrm{psec})$ | $\mathbf{6 4 . 3 4 8}$ | 216.41 | 89.769 |
| Power $(\mu W)$ | 1.3267 | $\mathbf{1 . 1 7 9 2}$ | 3.9354 |
| PDP $(\mathrm{fJ})$ | $\mathbf{0 . 0 8 5 4}$ | 0.2552 | 0.3533 |

proposed design in terms of delay and PDP. Ternary inverters in [8] result in sufficient driving power for charging and discharging large output loads. The lack of these inverters in [7] causes poor driving capability. In addition, the small size of transistors intensifies slow operation, although it leads to the least occupied area and power consumption amongst the three adder cells.

The Half Adder presented in [8] consumes the highest amount of power due to the fact that there are parallel active paths between $\mathrm{V}_{d d}$ and Ground making it easier for the current to flow. For example when Sum has to be ' 1 ', $\overline{S u m}$ is ' 1 ' as well. Thus, current flows through two parallel paths. One of the paths is inside the main part, and the other one is within the Ternary inverter. Unlike this architecture, there is only one path in the proposed design through which current flows. The main parts, the threshold sensitive sub-circuits, are not ternary. They generate Binary signals. Therefore, average power consumption decreases considerably. In addition, Binary inverters bring adequate power for driving capacitor loads.

To measure how robust the designs regarding possible $\mathrm{D}_{C N T}$ variations are, Monte Carlo transient analysis with a reasonable number of 30 iterations for each simulation is performed. The statistical significance of 30 iterations is quite high. If a circuit operates properly for all the 30 iterations, there is $99 \%$ probability that over $80 \%$ of all the possible component values operate properly [17]. A standard derivation of 0.04 nm to 0.2 nm is taken into account for each mean diameter value [18].

The maximum PDP variation versus the $\mathrm{D}_{C N T}$ variation assuming Gaussian with 8 -sigma and 6 -sigma distributions are plotted in Fig. 11 (a) and Fig. 11 (b), respectively. The proposed design has the lowest sensitivity to process variation in comparison with the previous ones, though the utilized methods are quite the same. This is because Binary signals have higher noise margins, and are less likely to be distorted. Most signals generated within the given structure are Binary. The adder cell presented in [8] is the most intolerable one.

Ternary Full Adders are also simulated under the same


Fig. 11 Maximum PDP variation of THAs versus $\mathrm{D}_{C N T}$ variation, (a) 8 -sigma distribution, (b) 6-sigma distribution.

Table 6 Simulation results of TFAs.

| Design | Proposed | Previous [7] | Previous [8] |
| :---: | :---: | :---: | :---: |
| \#Transistors | $\mathbf{3 5}$ | 41 | 64 |
| Total Width $(\mathrm{nm})$ | $\mathbf{9 9 2 0}$ | 11140 | 18740 |
| Static Power $(\mu W)$ | $\mathbf{1 . 3 8 1 3}$ | 1.8135 | 17.426 |
| $V_{d d}=0.75 V$ |  |  |  |
| Delay $(\mathrm{psec})$ | 134.78 | 202.18 | $\mathbf{8 8 . 9 3 4}$ |
| Power $(\mu W)$ | $\mathbf{4 . 5 9 6 9}$ | 5.2271 | 26.910 |
| PDP $(\mathrm{fJ})$ | $\mathbf{0 . 6 1 9 6}$ | 1.0568 | 2.3932 |
| $V_{d d}=0.7 \mathrm{~V}$ |  |  |  |
| Delay $(\mathrm{psec})$ | 153.23 | 210.28 | $\mathbf{9 7 . 5 2 0}$ |
| Power $(\mu W)$ | $\mathbf{2 . 7 3 8 5}$ | 3.1127 | 18.895 |
| PDP $(\mathrm{fJ})$ | $\mathbf{0 . 4 1 9 6}$ | 0.6545 | 1.8427 |
| $V_{d d}=0.65 V$ |  |  |  |
| Delay $(\mathrm{psec})$ | 175.43 | 231.44 | $\mathbf{1 1 0 . 5 0}$ |
| Power $(\mu W)$ | $\mathbf{1 . 5 9 1 7}$ | 1.8201 | 14.144 |
| PDP $(\mathrm{fJ})$ | $\mathbf{0 . 2 7 9 2}$ | 0.4212 | 1.5629 |

conditions as THAs were simulated. Simulation results are demonstrated in Table 6. The proposed TFA has the fewest number of transistors. It occupies $11 \%$ and $47 \%$ less area in comparison with the designs presented in [7] and [8], respectively. Performance factors (Delay and power) are in an excellent balance. Consequently, it has the highest efficiency.

## 5. Ternary Ripple-Carry Addition

Ripple-carry adder is a well-known circuit for performing addition of two numbers. A Ternary RCA is quite similar to a Binary one. A THA is employed to add the least significant Ternary digits. The rest are summed up by TFAs (Fig. 12). As mentioned before, Ternary Full Adder adds three Ternary input variables. However, the output carry in THA never becomes ' 2 ' (Table 1). As a result, the highest boundary of $\Sigma \mathrm{in}$ in the following TFA is 5 , not 6 . Subsequently, the output carry of TFA becomes ' 2 ' only if $\Sigma$ in is 6 (Table 2), which never happens in Ternary RCA.

### 5.1 Pseudo-TFA

As it is shown in Fig. 12, the highest boundary of $\Sigma$ in is always 5 in TFAs whose application is ripple-carry addition. Therefore, it is possible to optimize TFA circuit for this exclusive application. Figure 13 shows the proposed pseudoTFA, which is designed on the basis of the truth table of TFA (Table 2) from which $\Sigma i n=6$ is eliminated. Eight transistors are eliminated from the proposed TFA cell (Fig. 10) to


Fig. 12 Ternary ripple-carry adder (RCA).


Fig. 13 The proposed pseudo-TFA.

Table 7 Simulation results of the Pseudo-TFA.

| Design | Proposed TFA | Pseudo-TFA |
| :---: | :---: | :---: |
| \#Transistors | 35 | $\mathbf{2 7}$ |
| Total Width $(\mathrm{nm})$ | 9920 | $\mathbf{9 1 8 0}$ |
| Static Power $(\mu W)$ | 1.3813 | $\mathbf{1 . 3 3 3 6}$ |
| $V_{d d}=0.75 \mathrm{~V}$ |  |  |
| Delay $(\mathrm{psec})$ | 134.78 | $\mathbf{6 4 . 1 6 6}$ |
| Power $(\mu W)$ | 4.5969 | $\mathbf{4 . 5 1 2 9}$ |
| PDP $(\mathrm{fJ})$ | 0.6196 | $\mathbf{0 . 2 8 9 6}$ |
| $V_{d d}=0.7 \mathrm{~V}$ |  |  |
| Delay $(\mathrm{psec})$ | 153.23 | $\mathbf{7 8 . 7 5 0}$ |
| Power $(\mu W)$ | 2.7385 | $\mathbf{2 . 6 9 8 9}$ |
| PDP $(\mathrm{fJ})$ | 0.4196 | $\mathbf{0 . 2 1 2 5}$ |
| $V_{d d}=0.65 \mathrm{~V}$ |  |  |
| Delay $(\mathrm{psec})$ | 175.43 | $\mathbf{1 1 0 . 0 7}$ |
| Power $(\mu W)$ | 1.5917 | $\mathbf{1 . 5 5 9 2}$ |
| PDP $(\mathrm{fJ})$ | 0.2792 | $\mathbf{0 . 1 7 1 6}$ |

reach the pseudo-TFA. This optimization improves all performance parameters (Table 7).


Fig. 14 Input patterns which are fed to the Ternary ripple-carry adders to measure the maximum delay.

Table 8 Simulation results of Ternary RCAs.

| Design | Proposed | Previous [7] | Previous [8] |
| :---: | :---: | :---: | :---: |
| \#Transistors | $\mathbf{1 8 6}$ | 274 | 332 |
| Total Width $(\mathrm{nm})$ | $\mathbf{6 2 6 0 0}$ | 73060 | 119260 |
| Delay $(\mathrm{psec})$ | 392.26 | 654.57 | $\mathbf{3 3 9 . 8 6}$ |
| Power $(\mu W)$ | $\mathbf{9 . 9 2 4 5}$ | 12.299 | 90.321 |
| PDP $(\mathrm{fJ})$ | $\mathbf{3 . 8 9 2 9}$ | 8.0505 | 30.696 |

### 5.2 Simulation Results

The proposed THA and six pseudo-TFAs are put together in order to form a 7 -tit RCA. To measure worst-case delay, different input patterns are fed to the adder block (Fig. 14) so that a transition propagates from the input of the first stage $\left(\mathrm{a}_{0}\right)$ to the outputs of the last stage ( $\mathrm{s}_{6}$ or $\mathrm{c}_{7}$ ). Moreover, this input pattern is designed in a way that it causes all possible transitions in the output Sum of the last stage happen ( $\mathrm{s}_{6}$ : $0 \rightarrow 1,0 \rightarrow 2,1 \rightarrow 0,1 \rightarrow 2,2 \rightarrow 0$, and $2 \rightarrow 1$ ).

A long duration of iterative input pattern is also fed to the adder blocks to measure average power consumption. Simulation results of Ternary ripple-carry adders are reported in Table 8. The proposed RCA operates a bit slower than the structure formed by THA and TFAs presented in [8]. Other than that, the proposed adder block is by far the most efficient one.

For the sake of completeness, another survey is conducted to observe how efficient a Ternary adder is in comparison with a Binary one, also to study the advantages and disadvantages of each one.

To conduct a fair comparison, both adders should cover approximately the same data range in the decimal numeral system. By considering seven Ternary digits, the largest possible number is $3^{7}-1=2186$. Eleven bits are required in Binary logic to reach nearly the same number ( $2^{11}-1=2047$ ). Therefore, four more Full Adders are required in Binary logic to add two numbers with the same data range (Fig. 15). The Full Adder cell presented in [19] is selected to form the Binary ripple-carry adder. This selection is because of its high efficiency and its resemblance to the Ternary adders presented in this paper. In a similar manner, it takes the sum of input variables and generates the output signals.


Fig. 15 Ripple-carry adders, (a) The 11-bit Binary RCA, (b) The 7-tit Ternary RCA.

Table 9 Simulation results of ripple-carry adders.

| Design | 7-tit RCA | 11-bit RCA |
| :---: | :---: | :---: |
| \#Transistors | $\mathbf{1 8 6}$ | 206 |
| Total Width $(\mathrm{nm})$ | $\mathbf{6 2 6 0 0}$ | 87200 |
| \#Pins | $\mathbf{2 2}$ | 34 |
| Delay $(\mathrm{psec})$ | $\mathbf{3 9 2 . 2 6}$ | 614.26 |
| Power $(\mu W)$ | 9.9245 | $\mathbf{5 . 5 0 6 5}$ |
| PDP $(\mathrm{fJ})$ | 3.8929 | $\mathbf{3 . 3 8 2 4}$ |
| Data Range of the Result | $\mathbf{0 - 4 3 7 2}$ | $0-4094$ |

A conventional CMOS Half Adder is taken into account to implement the first stage of Binary ripple-carry addition. Simulation results in 0.7 V power supply are shown in Table 9. In terms of power consumption, Binary circuits are far more efficient than Ternary ones. This is due to the static current flow which is inevitable in the unbalanced Ternary circuits, where logic value ' 1 ' is implemented by $\frac{V_{d d}}{2}$.

In terms of speed, Ternary logic surpasses Binary. Higher computational speed is achieved on account of the fact that a single Ternary digit has more information than a bit. Therefore, fewer stages with a shorter critical path are needed to add the same input numbers. Not only is the proposed Ternary adder faster than the Binary one, but it also covers higher data range for the final result.

Eventually, the Ternary ripple-carry adder outperforms its Binary counterpart in terms of area, the number of transistors, and the number of input/output pins.

## 6. Conclusion

New high-performance Ternary Half and Full Adders have been proposed in this paper. They are utilized to realize a Ternary ripple-carry adder. TFA has been optimized for Ternary ripple-carry addition in a way to reach a fast and compact circuit. The usage of Ternary circuits leads to faster computational speed as well as denser integrated chips than Binary circuits by paying the price of higher power consumption. This has been demonstrated in this paper for the ripple-carry adder which has been implemented by similar structures of Binary and Ternary 1-bit adder cells.

## References

[1] E. Dubrova, "Multiple-valued logic in VLSI: Challenges and opportunities," Proc. NORCHIP'99, pp.340-349, Nov. 1999.
[2] R. Ho, W. Mai, and M.A. Horowitz, "The future of wires," Proc. IEEE, vol.89, no.4, pp.490-504, April 2001.
[3] S.L. Hurst, "Multiple-valued logic, its status and its future," IEEE Trans. Comput., vol.C-33, no.2, pp.1160-1179, Dec. 1984.
[4] C.J. Fang, C.H. Huang, J.S. Wang, and C.W. Yeh, "Fast and compact dynamic ripple carry adder design," Proc. IEEE Asia-Pacific Conf. ASIC, pp.25-28, 2002.
[5] R. Martel, T. Schmidt, H.R. Shea, T. Hertel, and P. Avouris, "Singleand multi-wall carbon nanotube field-effect transistors," Appl. Phys. Lett., vol.73, no.17, pp.2447-2449, Oct. 1998.
[6] S. Lin, Y.-B. Kim, and F. Lombardi, "A novel CNTFET-based ternary logic gate design," IEEE 52nd Int. Midwest Symp. Circuits and Systems, pp.435-438, Cancun, Aug. 2009.
[7] M. Maleknejad, R. Faghih Mirzaee, K. Navi, and O. Hashemipour, "Multi- $\mathrm{V}_{t}$ ternary circuits by carbon nanotube field effect transistor technology for low-voltage and low-power applications," J. Computational and Theoretical Nanoscience, vol.11, no.1, pp.110-118, Jan. 2014.
[8] R. Faghih Mirzaee, M.H. Moaiyeri, M. Maleknejad, K. Navi, and O. Hashemipour, "Dramatically low-transistor-count high-speed ternary adders," 43rd Int. Symp. Multiple-Valued Logic, pp.170175, Toyama, May 2013.
[9] S. Lin, Y.-B. Kim, and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," IEEE Trans. Nanotechnology, vol.10, no.2, pp.217-225, March 2011.
[10] M.H. Moaiyeri, A. Doostaregan, and K. Navi, "Design of energyefficient and robust ternary circuits for nanotechnology," IET Circuits, Devices \& Systems, vol.5, no.4, pp.285-296, July 2011.
[11] S.A. Ebrahimi, P. Keshavarzian, S. Sorouri, and M. Shahsavari, "Low power CNTFET-based ternary full adder cell for nanoelectronics," Int. J. Soft Computing and Engineering, vol.2, no.2, pp.291295, May 2012.
[12] J.A. Mol, J. van der Heijden, J. Verduijn, M. Klein, F. Remacle, and S. Rogge, "Balanced ternary addition using a gated silicon nanowire," Appl. Phys. Lett., vol.99, no.26, pp.263109.1-263109.3, Dec. 2011.
[13] M.H. Moaiyeri, R. Faghih Mirzaee, A. Doostaregan, K. Navi, and O. Hashemipour, "A universal method for designing low-power carbon nanotube FET-based multiple-valued logic circuits," IET Computers \& Digital Techniques, vol.7, no.4, pp.167-181, July 2013.
[14] C.H. Chang, J. Gu, and M. Zhang, "A review of $0.18 \mu \mathrm{~m}$ full adder performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol.13, no.6, pp.686-695, June 2005.
[15] J. Deng, Device modelling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nanotube field effect transistors, Ph.D. Thesis, Stanford University, 2007.
[16] Y.B. Kim and Y.-B. Kim, "High speed and low power transceiver design with CNFET and CNT bundle interconnect," IEEE Int. SOC Conf., pp.152-157, Sept. 2010.
[17] S. Lin, Y.-B. Kim, and F. Lombardi, "Design and analysis of 32 nm PVT tolerant CMOS SRAM cell for low leakage and high stability," Integration, VLSI J., vol.43, no.2, pp.176-187, April 2010.
[18] H. Shahidipour, A. Ahmadi, and K. Maharatna, "Effect of variability in SWCNT-based logic gates," Proc. Int. Symp. Integrated Circuits, pp.252-255, 2009.
[19] K. Navi, H. Hossein Sajedi, R. Faghih Mirzaee, M.H. Moaiyeri, A. Jalali, and O. Kavehei, "High-speed full adder based on minority function and bridge style for nanoscale," Integration, the VLSI Journal, vol.44, no.3, pp.155-162, June 2011.


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