

LETTER

A 10.4-Gs/s High-Resolution Wideband Radar Sampling System Based on TIADC Technique

Jingyu LI[†], Student Member, Dandan XIAO^{††}, and Yue ZHANG^{†††a)}, Nonmembers

SUMMARY A high-speed high-resolution sampling system is the crucial part in wideband radar receivers. A 10.4-GS/s 12-bit wideband sampling system based on TIADC technique is designed in this letter. The acquisition function is implemented on a VPX platform. The storage function is implemented on a standard 19-inch rack server. The sampled data is transmitted at high speed through optical fibers between them. A mixed calibration method based on perfect reconstruction is adopted to compensate channel mismatches of wideband TIADC system. For sinusoidal signals from 100 MHz to 5000 MHz, more than 46-dB SNDR and 56-dB SFDR can be obtained in this sampling system. This letter provides a high-speed and high-resolution acquisition scheme for direct intermediate frequency sampling wideband digital receivers.

key words: TIADC, wideband sampling system, mismatch calibration

1. Introduction

Sampling system with high speed, high resolution and large bandwidth is the core component of wideband digital receivers, measurement instruments, and high-speed communication systems [1]. With the development of analog-to-digital converter (ADC) and high-speed storage technology, the direct intermediate frequency sampling (DIFS) of wideband radar has been widely used in engineering. The DIFS of wideband radar requires a large signal dynamic range, especially for high-resolution imaging radars. The number of quantized bits of the ADC for sampling echo signals is at least 10 bits. Increasing the bandwidth will narrow the signal beam and improve the resolution. According to Nyquist sampling theorem, the sampling rate is at least twice of the bandwidth. If the bandwidth of the signal is large enough, the analog-to-digital conversion cannot be realized by a single chip correctly. Time-Interleaved ADC (TIADC) technique can effectively solve this problem. Several ADCs with lower sampling rate are used to acquire the signal in parallel at the same clock frequency but different clock phases [2]. Finally, the sampling sequences of sub-ADCs are combined as the output of the system to increase the sampling rate.

The sampling rate can be multiplied using TIADC

technology, but channel mismatches are brought in. In TIADC systems, channel mismatches seriously degrade the signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) [3]. A mixed calibration method based on perfect reconstruction is adopted to compensate channel mismatches in wideband TIADC system. In Sect. 2, system hardware based on VPX platform is designed, and calibration method for wideband TIADC system is presented. The experimental result is obtained in Sect. 3. Section 4 gives the summary of this work.

2. System Design

The hardware design of the TIADC system based on the VPX platform is described in this section. Four sub-ADCs in two ADC chips are time-interleaved in this system. The overall block diagram is shown in Fig. 1. There are two sampling cards, a field programmable gate array (FPGA) carrier board, an input output (IO) board, a clock board, a receiving board, a backplane and a standard 19-inch rack storage server in the system. The sampling card is designed in the form of FPGA Mezzanine card (FMC). Analog signal is interfaced to a power divider and transmitted to two FMCs respectively. The reference clock is interfaced to the clock board. The FMC is driven by the sampling clock and SYSREF generated from the clock board. The circuit boards are interconnected by the backplane. The sampled data is cached in DDR3 firstly, and transmitted via multi-gigabit

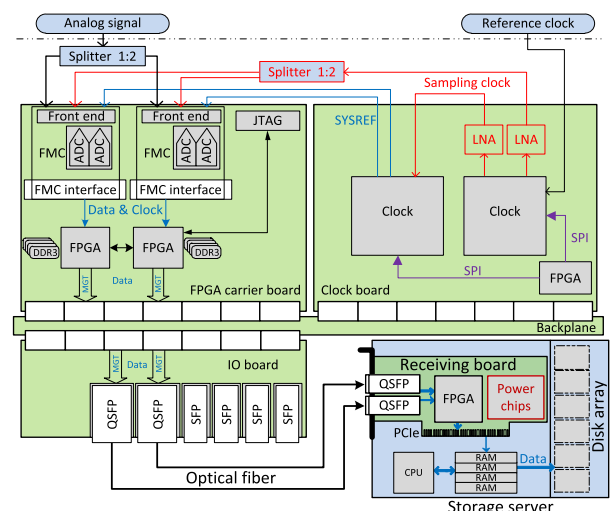


Fig. 1 Block diagram of the TIADC system.

Manuscript received May 19, 2019.

Manuscript publicized April 20, 2020.

[†]The author is with College of Advanced Interdisciplinary Studies, National University of Defense Technology, Changsha, 410073, China.

^{††}The author is with Communication Petty Officer Academy, Army Engineering University of PLA, Chongqing, 400035, China.

^{†††}The author is with National Key Laboratory of Science and Technology on ATR, National University of Defense Technology, Changsha, 410073, China.

a) E-mail: zhangyue.2018@126.com

DOI: 10.1587/transinf.2019EDL8100

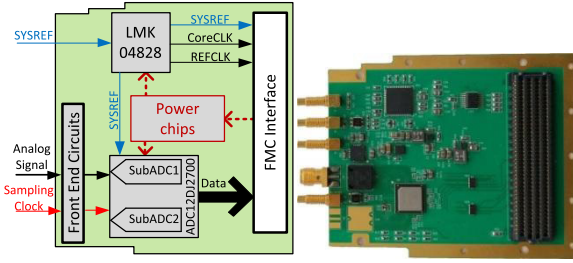


Fig. 2 Structure and object of the FMC

transceiver (MGT). Optical transceivers in the IO board convert the sampled data from electrical signal to optical signal which is passed through optical fiber to receiving board of storage server. There is a receiving board with a peripheral component interconnect express (PCIe) interface installing in the storage server. Storage of sampled data and TIADC channel mismatch calibration are implemented on the storage server. The design of the major circuit boards is described below.

2.1 FMC Design

A commercial ADC (ADC12DJ2700) introduced by Texas Instruments in 2018 is employed to implement the 5.2-GS/s FMC. The structure and object of the FMC are shown in Fig. 2. Maximum sample rate of the ADC chip is 5.4 GS/s, resolution is 12 bits, and bandwidth is 8 GHz [5]. Two sub-ADCs alternately sample data in the ADC chip. A variable delay line (VDL) is in the clock path of each sub-ADC, which can be used to compensate the timing mismatch. The ADC works in the mode of JESD204B subclass1, and SYSREF is used for data synchronization. The LMK04828 is a clock chip, which operates in 0-delay mode and provides SYSREF for FPGA and ADC. It also provides reference clock for MGT and clock for JESD204B IP core. The single to differential conversion and impedance match are implemented by the front end circuit.

2.2 FPGA Carrier Board Design

Two Xilinx Virtex-7 FPGAs (XC7VX690T) are integrated on the FPGA carrier board. Generally, echo signal of wide-band radar is sampled at a certain duty cycle, and the peak data rate is very high, so large capacity data cache is needed. There are two groups of DDR3 caches interconnected with each FPGA. High-speed multi-channel serial communication between FMC and FPGA is through a FMC interface. Data acquisition control, data alignment and format conversion are accomplished in FPGAs. Then the data is delivered to the IO board via P3 and P4. The structure and object of the FPGA carrier board are shown in Fig. 3.

2.3 Clock Board Design

Clock board is designed to generate the sampling clock and reference clock (SYSREF) required by multiple FMCs. The

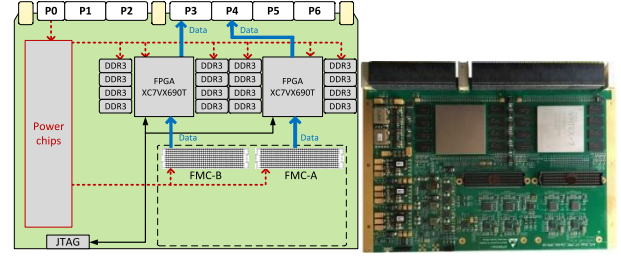


Fig. 3 Structure and object of the FPGA carrier board

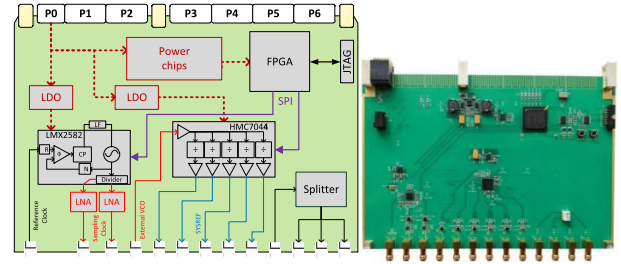


Fig. 4 Structure and object of the clock board

output clock should meet the needs of frequency, amplitude, clock jitter and phase synchronization. The sampling rate of FMC is 5.2 GS/s, and the corresponding sampling clock and SYSREF frequencies are 2.6 GHz and 10 MHz respectively. The amplitude of sampling clock and SYSREF needed by FMCs are approximately 8 dBm and 5 dBm respectively. Clock jitter is generally portrayed by its root mean square (RMS). Signal-to-noise ratio (SNR) is an important index to appraise the performance of an ADC. On the basis of the relationship between SNR and jitter, the SNR can be evaluated by formula (1). If $f_{in} = 5000$ MHz and $SNR > 45$ dB, the t_{jitter} should be less than 178 fs.

$$SNR = -20 \lg(2\pi f_{in} t_{jitter}) \quad (1)$$

The required frequency and sampling clock jitter can be satisfied by the clock chip (LMX2582). The LMX2582 has two outputs. One is for the voltage-controlled oscillator (VCO) of HMC7044, and the other is for the 2.6-GHz sampling clock of the FMCs. After passing through the splitter, the amplitude of sampling clock is reduced by about 4 dB. The LMX2582 cannot meet the requirement of amplitude, and a low noise amplifier (LNA) is added to its output. Both clock chips are programmed by a FPGA via the serial peripheral interface (SPI). The structure and object of the clock board are shown in Fig. 4.

2.4 IO Board Design

The IO board extends the interface of the FPGA carrier board. The structure and object of the IO board are shown in Fig. 5. Its main interfaces include two quad small form-factor pluggable (QSFP) optical transceivers, small form-factor pluggable (SFP) optical transceivers and a J30J. Sampled data is transmitted to receiving board through QSFP optical transceivers. Two QSFP transceivers consist of eight

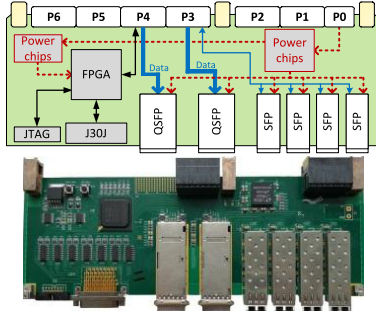


Fig. 5 Structure and object of the IO board

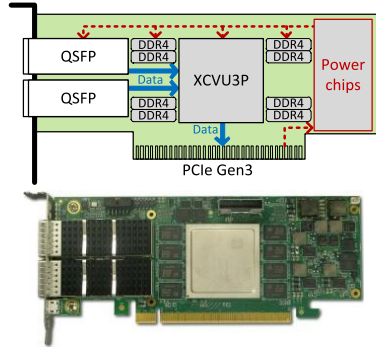


Fig. 6 Structure and object of the receiving board

lanes, each of which can support a maximum transmission rate of 10 Gb/s. SFP optical transceivers can be used to receive sampling control information, which is passed to the FPGA carrier board via P3. The J30J can be used to receive RS-422 signals such as sync signals, which are passed to the FPGA carrier board via P4.

2.5 Receiving Board Design

The structure and object of the Receiving board are shown in Fig. 6. The receiving board integrates two QSFP optical transceivers, a Xilinx Virtex UltraScale Plus FPGA (XCVU3P) and two sets of DDR4 caches. QSFP optical transceivers are used to receive sampled data from the IO board. The sampled data is cached in DDR4 and then sent by the FPGA to the memory of the storage server through the PCIe interface. Finally, the data is stored in the disk array.

2.6 Calibration Method

The offset mismatch, timing mismatch and gain mismatch have the greatest degradation on system sampling performance for a TIADC system consisting of multiple ADC chips. When sampling large bandwidth signals, the gain mismatch and timing mismatch of each channel are functions of frequency, which cannot be treated as fixed values. The offset mismatch does not vary with the input signal frequency. It can be evaluated from the noise data of each sub-ADC and rectified by the subtraction operation without dif-

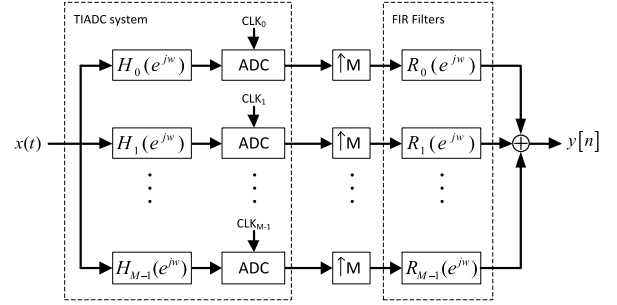


Fig. 7 Perfect reconstruction model of M -channel TIADC system

ficulty.

The phases of four sub-ADCs in this system are about 0, 90, 180 and 270 degrees. The VDL inside ADC is used to adjust the phase relationship of each channel of TIADC system. The VDL register value of ADC can be calculated by the relationship between sampling period and VDL step. Then the sampled data of each channel is subjected to a FIR filter to complete the wideband TIADC channel mismatch calibration. Here is how to get this FIR filter.

Perfect reconstruction model of M -channel TIADC system is represented as Fig. 7. $H_m(e^{j\omega})$ is the transmission function of each channel. $CLK_0 \cdots CLK_{M-1}$ is sampling clock, whose phase difference is $2\pi/M$ in sequence. The sampling rate of sub-ADC is $1/M$ of the system sampling rate. This is equivalent to down sampling $x(t)$. Then zeros are interpolated into the sampled data. The discrete sampled data of each channel is transmitted to the corresponding FIR filter $R_m(e^{j\omega})$ respectively after M times up sampling. The compensated data $y[n]$ can be obtained by adding the output of each filter. The coefficients r_m of compensation FIR filters can be gotten using $H_m(e^{j\omega})$ by the perfect reconstruction algorithm [4].

3. Result

The experimental setup is shown in Fig. 8. Four 2.6-GS/s sub-ADCs in two FMCs operate as a 10.4-GS/s TIADC system. A signal generator (SMJ100A) provides the 100-MHz reference clock to the clock board. Another signal generator (E8257D) produces analog sinusoidal test signals. The Fig. 9 depicts spectrum comparison of the 2253 MHz sine signal before and after calibration. After the channel mismatch compensation, the spurious signals caused by channel mismatches are effectively decreased. The SNDR is enhanced from 34.7 dB to 51.3 dB and the SFDR is raised from 34.8 dB to 64.7 dB.

A multi-tone power ratio (MTPR) experiment is executed on the TIADC system. Multi-tone sine signal from 453 MHz to 4653 MHz is infused to the TIADC system. The Fig. 10 displays spectrum comparison of the multi-tone signal before and after calibration. After channel mismatch compensation, the spurs are significantly suppressed, which shows the validity of the calibration method.

Dynamic performance test results between the TIADC

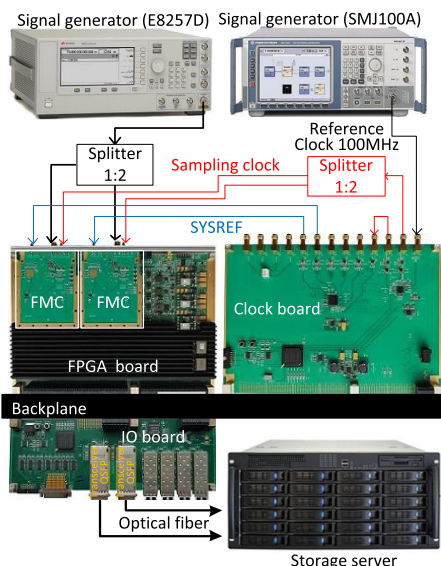


Fig. 8 Experimental setup for the 10.4-GS/s TIADC system

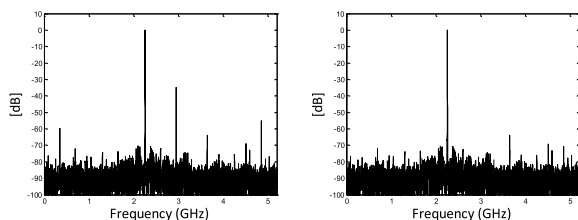


Fig. 9 The spectrum of 2253 MHz sine signal

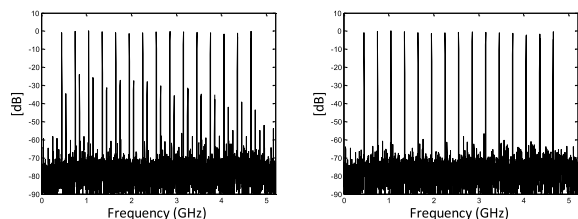


Fig. 10 The spectrum of multi-tone signal

sampling system and its sub-ADC are plotted in Fig. 11. The SNDR and SFDR of the sampling system is almost the same as that of its sub-ADC. At 10.4-GS/s sampling rate, the SNDR above 46 dB and SFDR above 56 dB for a sinusoidal input signal from 100 MHz to 5000 MHz can be obtained by this TIADC system.

4. Conclusion

In this letter, a 10.4-GS/s 12-bit wideband sampling sys-

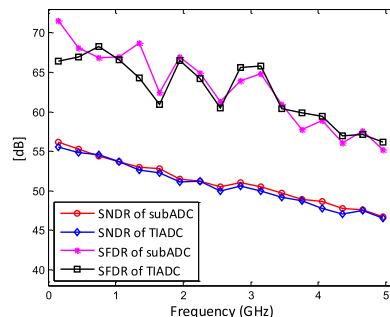


Fig. 11 Test result of SNDR and SFDR

tem based on TIADC technique is implemented. The major system hardware is described. The calibration method of wideband TIADC system is acquired. For sine signals from 100 MHz to 5000 MHz, more than 46-dB SNDR and 56-dB SFDR can be obtained in this sampling system. Under this system architecture, the number of FMC can be easily extended to reduce duplication of hardware development. This design provides a high-speed and high-resolution acquisition scheme for direct intermediate frequency sampling or direct radio frequency sampling of wideband digital receivers.

Acknowledgments

This work is supported by the National Natural Science Foundation of China (No. 6157010118).

References

- [1] C.-Y. Lin, Y.-H. Wei, and T.-C. Lee, "A 10-bit 2.6-GS/s Time-Interleaved SAR ADC With a Digital-Mixing Timing-Skew Calibration Technique," *IEEE J. Solid-State Circuits*, vol.53, no.5, pp.1508–1517, 2018. DOI: 10.1109/JSSC.2018.2793535
- [2] W.C. Black and D.A. Hodges, "Time interleaved converter arrays," *IEEE J. Solid-State Circuits*, vol.15, no.6, pp.1022–1029, 1980. DOI: 10.1109/JSSC.1980.1051512
- [3] A. Buchwald, "High-speed time interleaved ADCs," *IEEE Commun. Mag.*, vol.54, no.4, pp.71–77, 2016. DOI: 10.1109/MCOM.2016.7452269
- [4] J. Li, J. Pan, and Y. Zhang, "Automatic Calibration Method of Channel Mismatches for Wideband TI-ADC System," *Electronics*, vol.8, no.56, pp.1–13, 2019. DOI: 10.3390/electronics8010056
- [5] Texas Instruments, "ADC12DJ2700 5.4-GSPS single-channel or 2.7-GSPS dual-channel, 12-bit, RF-sampling analog-to-digital converter (ADC)," 2018. <http://www.ti.com/lit/ds/symlink/adc12dj2700.pdf>.