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# LETTER Master-Slave FF Using DICE Capable of Tolerating Soft Errors Occurring Around Clock Edge

**SUMMARY** This letter reveals that an edge-triggered master-slave flipflop (FF) using well-known soft error tolerant DICE (dual interlocked storage cell) is vulnerable to soft errors occurring around clock edge. This letter presents a design of a soft error tolerant FF based on the master-slave FF using DICE. The proposed design modifies the connection between the master and slave latches to make the FF not vulnerable to these errors. The hardware overhead is almost the same as that for the original edge-triggered FF using the DICE.

key words: soft error, DICE (the dual interlocked storage cell), masterslave flip-flop, clock edge

#### 1. Introduction

Soft errors (also referred as single-event-upsets (SEUs)) are transient-induced events on storage elements caused by several reasons such as striking of high energy neutron radiation. In the recent high density VLSI the soft error issue becomes of more serious [1]. To resolve this issue, many researchers have studied soft error tolerant techniques. For memory systems, such as SRAM, ECCs (error control codes) are well-used [2]. For storage elements (latches and flip-flops (FFs)) in logic circuits, soft error tolerant latches and FFs have been proposed, e.g. the built-in soft error resilience (BISER) [3] and the soft error hardened (SEH) latch [4]. The dual interlocked storage cell (DICE) is a well-known primitive class of soft error tolerant storage elements [5].

We can construct an edge-triggered master-slave FF by using two latches as master and slave latches. This letter analyzes an edge-triggered master-slave FF using the DICE latches. This analysis reveals the following issue: the FF using the DICE latches is vulnerable to soft errors occurring around clock edge. To resolve this issue, this letter presents a design of a FF capable of tolerating soft errors occurring around clock edge based on the master-slave FF using the DICE latches.

This letter is organized as follows: Section 2 reviews the DICE as preliminary. Section 3 gives a new analysis and clarifies the issue on the master-slave FF with DICE. Sections 4 and 5 present and evaluate the proposed design. Section 6 concludes this letter.

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VDD CLK Q1<sub>d</sub>  $\underline{Q3}_{d}$ 4B Q2B Q3 01 O2B 03  $\overline{O}4B$ 04B CLKB CLKB GND Fig. 1 Construction of DICE.

#### 2. Dual Interlocked Storage Cell (DICE)

Figure 1 illustrates the construction of the DICE. The DICE has four nodes Q1, Q2B, Q3 and Q4B. For CLK = 0 and CLKB = 1, the nodes Q1 and Q3 keep stored values; the nodes Q2B and Q4B keep their inverted values. The DICE is capable of tolerating single-node-upsets (SNUs). For example, if an error  $0 \rightarrow 1$  occurs on Q3, the node Q2B is connected to both  $V_{DD}$  and GND, and then incompletely discharged. The remaining nodes (Q1 and Q4B) keep the correct value and then they correct the values of Q3 and Q2B finally.

The DICE has good trade-off between soft error tolerant capability and performance and then many researchers have studied its extension. For example, F-DICE [6], Delta DICE [7] and DONUT latches [8], [9] have multiple-nodeupset (MNU) tolerant capability while the original DICE is capable of tolerating only SNUs. The DF-DICE [10] and the FF of [11] is capable of tolerating single-event-transients (SETs) as well as SEUs by using delay elements.

# 3. Analysis of Soft Errors Occurring on FF with DICE around Clock Edge

This section presents simulation results for the master-slave FF using DICE latches. We can construct the FF by using DICE latches as the master and slave latches. Figure 2 illustrates the outline of the master-slave FF with DICE. The DICE (shown in Fig. 1) is used as the rectangle labeled as "DICE" in Fig. 2. We can construct a DICE latch (i.e. the master or slave latch in Fig. 2) by adding two three-state

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Fig. 2 Outline of original master-slave FF using DICE latches.



Fig. 3 Clock buffer.

buffers to a DICE. The FF uses the clock buffer shown in Fig. 3. The buffer generates CLK and CLKB from the clock signal supplied at the clock input of the FF. The phase of CLK is the same as the original clock signal and that of CLKB is inverted. The DICE is connected to the D-input through three-state inverters. The three-state inverters do not have the inverter that generates inverted enable signal unlike general three-state gates. Instead, they use CLK or CLKB (generated in the clock buffer) as the inverted enable signal. The proposed FF, which will be presented in the next section, is based on this FF. For distinction, we call the FF shown in Fig. 2 as "the original FF."

First, we consider the critical charge for soft errors occurring on the original FF around clock rising. The critical charge is obtained by HSPICE simulation using the 16 nm Predictive Technology Model (PTM) library [12]–[14] in the typical process variation, with supply voltage of 0.7 V and at the room temperature of 27°C. This simulation uses the double exponential model (with the same parameters as the simulation of [15]) as the soft error occurrence model. The clock falls at time 0 and never changes after time 0. An error occurs at  $\Delta t$  ns ( $-1 \leq \Delta t \leq 0.5$ ). The critical charge means the maximal charge which the FF can tolerate. High critical charge means that the FF has high soft error tolerant capability. We regards that the FF tolerates an error if the output value is equal to the correct value at 500 ps. Critical charges are measured for errors (SNUs) on any nodes on inverter loops and for any stored and input values. The figure shows the worst (minimal) critical charge among these cases.

A simulation result (the graph is omitted) indicates that the critical charge is very high (higher than 20 fC for any  $\Delta t$ ). This indicates that soft errors occurring on the original FF around clock rising is tolerable.

Next, we consider soft errors occurring around clock falling. Figure 4 shows the critical charge of the original FF. The critical charge is low if an error occurs just before clock falling. The minimal value of the critical charge is 2.54 fC at  $\Delta t = -0.15$  ns. This low critical charge is caused by errors occurring on the master latch. The critical charge for errors on the slave latch is very high.



Fig.4 Critical charge of original master-slave FF using DICE for soft errors occurring around clock falling.



Fig. 5 Waveform for original master-slave FF using DICE.

Figure 5 provides an HSPICE simulation waveform for the original FF to demonstrate the behavior for errors on the master latch before clock falling. In the simulation, an error with the charge of 10 fC was applied to Q3 in the master latch at -0.18 ns (i.e. just before clock CLK falls). The error transiently flips the value of Q2B (i.e. the output value) in the master latch. The flipped value is input to the slave latch and then the values of all nodes (Q1, Q2B, Q3, Q4B) in the slave latch are incorrectly flipped. The output value of the master latch is corrected after a short time by the soft error tolerant capability of the master latch. If the clock kept high, the value of the slave latch would be overwritten with the corrected value of the master latch. However, in the waveform, the clock falls at time 0, i.e. before the overwritten, and then the value of the slave latch keeps the flipped value. Finally the output value of the original FF is never corrected.

As mentioned above, the critical charge is low if an

error occurs just before clock falling. The period regarded as "just before clock falling" is too long to ignore. Figure 4 indicates that the original FF is vulnerable to even errors occurring 0.4 ns before the clock falling. This means that, for clock frequency of 1 GHz or faster, the original FF is almost always vulnerable when the clock is high.

# 4. Proposed FF Capable of Tolerating Soft Errors Occurring Around Clock Edge

As mentioned in Sect. 3, the original master-slave FF using the DICE latches is vulnerable to soft errors occurring on the master latch before clock falling. This section presents a design of a FF capable of tolerating soft errors occurring before clock falling.

Figure 6 illustrates the construction of the proposed FF. The FF uses the clock buffer shown in Fig. 3. The D-input of the DICE latch is connected to two nodes Q1 and Q3 through three-state buffers. In the original FF in Fig. 2, both the nodes are connected to the Q2B of the master DICE (through three-state buffers). In contrast, in the proposed FF, Q3 of the slave DICE is connected to Q4B (and not Q2B) of the master DICE.

Next we explain error correction for errors (SNUs) occurring on the master latch before clock falling. Figure 7



Fig. 6 Outline of proposed FF.



Fig. 7 Waveform for proposed FF.

shows an HSPICE simulation waveform for the proposed FF. An error with the charge of 10 fC was applied to O3 in the master latch at -0.18 ns. The error affects the output values of the master latch, just like the original FF. A soft error on the master latch of the proposed FF flips the value of only either (not both) Q2B or Q4B (Q2B in the waveform). The other output (O4B) keeps the correct value. When the clock is high, the slave latch is in a transparent state. The inverted values of O2B and O4B in the master latch are copied into Q1 and Q3 in the slave latch, respectively. Hence, just after error occurrence, the value of either Q1 or Q3 in the slave latch keeps the correct value while the value of the other node is flipped. Then, either Q2B or Q4B (Q4B in the waveform) is incompletely (dis-)charged and the other node (Q2B) keeps the correct value. Just after the clock falling, every node in the slave latch is left in the previous state. Thus, in the slave latch, the value of either Q1 or Q3 is incorrect, either node Q2B or Q4B has been incompletely (dis-)charged, and the remaining two nodes keep their correct values. This is the correctable state by the error tolerance capability of the DICE (as mentioned in Sect. 2). Finally, the output value of the proposed FF is corrected.

## 5. Evaluation

Our simulation (the graph is omitted) indicates that the critical charge of the proposed FF is very high (higher than 20 fC for any  $\Delta t$ ) for errors (SEUs) on the master and slave latches around clock rising and falling. Table 1 summarizes the error tolerant capability of the normal, original and proposed FFs. Here "the normal FF" means an ordinary master-slave FF not capable of tolerating soft errors [16]. The proposed FF has the strongest soft error tolerant capability.

Table 2 shows the comparison of area (the number of transistors) and dynamic power consumption of the proposed FF with those of the original and normal FFs. The comparison uses a 1 GHz clock signal and an input pattern with data activity of 0.1. Table 3 shows the comparison of AC characteristics (CLK-Q delay, setup and hold time). The power consumption and the AC characteristics are measured using HSPICE and the 16 nm Predictive Technology Model (PTM) library in all PVT variations (TT, FF, SS, FS, SF pro-

 Table 1
 Error tolerant capability.

clock	normal	original	proposed
stable	not tolerable	tolerable	tolerable
before rising	not tolerable	tolerable	tolerable
after rising	not tolerable	tolerable	tolerable
before falling	not tolerable	not tolerable	tolerable
after falling	not tolerable	tolerable	tolerable

Table 2Area (# of transistors) and dynamic power consumption ( $\mu W$ ).

	# of	power	
	transistors	peak	average
normal	24	200	1.63
original	44	256	2.50
proposed	44	264	2.49

**Table 3**AC characteristics (ps).

	CLK-Q delay		setup	hold	
	min	avg.	max	time	time
normal	12.2	23.7	70.1	44.8	-4.15
original	13.1	26.8	81.7	39.0	-2.24
proposed	13.1	26.7	81.3	39.3	-2.30

cesses,  $V_{\text{DD}} = 0.63$ , 0.7, 0.77 V and temperature of 0, 27, 100°C). The hardware overhead for the proposed FF is almost the same as the original FF. This means that the proposed design resolves the issue revealed in Sect. 3 with little penalty to hardware overhead.

# 6. Conclusion

This work has considered an edge-triggered master-slave FF with the DICE, and analyzed the effect of soft errors occurring around clock edge. This letter has revealed the following issue: The FF is vulnerable to soft errors occurring before clock falling. Furthermore, this letter has presented a new design of a soft error tolerant FF to resolve this issue. The proposed FF is based on the master-slave FF with the DICE. The connection between the master and slave latches differs from the original FFs. The evaluation result indicates that the proposed design resolves the issue with little penalty to hardware overhead.

This letter deals with only the master-slave FF with the DICE. However, we can construct soft error tolerant masterslave FFs using any soft error tolerant latches. There exist many soft error tolerant latches other than the DICE. The FFs with these latches may have a similar issue. Future work will resolve this issue.

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