

PAPER

Construction of Soft-Error-Tolerant FF with Wide Error Pulse Detecting Capability**

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SUMMARY In the recent high-density and low-power VLSIs, the occurrence of soft errors has become a significant problem. Recently, soft errors frequently occur on not only memory system but also logic circuits. Based on this standpoint, some constructions of soft-error-tolerant FFs were proposed. A conventional FF consists of some master and slave latches and C-elements. In the FF, soft error pulses occurring on combinational parts of logic circuits are corrected as long as the width of the pulses is narrow, that is within a specified width. However, error pulses with wide width are neither detected nor corrected in the FF. This paper presents a construction of soft-error-tolerant FFs by modifying the conventional soft-error-tolerant FF. The proposed FFs have the capability to detect error pulses having wide width as well as the capability to correct those having narrow width. The proposed FFs are also capable of detecting hard errors. The evaluation shows the soft-error-tolerant capability, AC characteristics, area overhead and power consumption of the FFs.

key words: soft error, wide pulse, flip-flop, C-element, delay element

1. Introduction

In recent high-density and low-power VLSIs, soft errors frequently occur during system operations from several reasons, e.g. radiation-induced transient pulses caused by neutrons from cosmic rays and alpha particles from packaging material [1]–[3]. Traditionally, soft errors occurring on only memory system seriously affect the operation of VLSI systems. In order to tolerate soft errors on memory system, error control coding has been studied by many researchers and widely used [4]. However, in recent VLSI systems, soft errors also frequently occur on logic circuits. Therefore, the occurrence of soft errors on logic circuits has become a significant problem.

From this standpoint, many soft-error-tolerant methods for soft errors occurring on logic circuits were proposed [5]. Logic circuits are composed of combinational parts and latches. To tolerate soft errors occurring on latches, the following methods were proposed: Dual Interlocked storage Cell (DICE) [6], soft error hardened latch scheme [7], Delay-Assignment-Variation (DAV) based optimization method [8], and methods using C-elements [9], [10]. Meanwhile, for soft errors occurring on combina-

tional parts, the following error tolerant methods have been proposed: methods using time redundancy [11]–[16], ones using pass transistors [17] and ones using Schmitt triggers [18].

In [10], constructions of soft-error-tolerant FFs capable of correcting soft errors occurring on latches as well as those on combinational parts has been proposed. The FFs are based on master-slave FFs and consist of some latches and C-elements. In the FFs, soft error pulses occurring on combinational parts of logic circuits are corrected as long as the width of the pulses is narrow within a specified range. However, soft error pulses having wide width outside the specified range are neither detected nor corrected in the FFs. In addition, the FFs do not tolerate hard errors that occur during system operations.

In recent VLSI, such error pulses with wide width sometimes occur due to several reasons such as power-supply noise as analyzed in [19] and experimentally shown in [20], and thus they are not negligible. Therefore, it is necessary to detect or correct such error pulses occurring in a system. In [21], a method detecting radiation particle strikes causing soft errors including ones with wide error pulses has been proposed. However, the methods only detect but do not corrected soft errors. So, system operations cannot be continued without recomputation if soft error occurs, even if it is frequent narrow pulses. Moreover, it detects only radiation-induced transient pulses. Hard errors also sometimes occur during system operations due to several reasons such as heavy ionized particle strikes [22]. From this, it is important to tolerate hard errors as well as soft errors.

This paper presents a construction of soft-error-tolerant FFs. The proposed FF is capable of correcting error pulses with narrow width occurring on the combinational parts and ones occurring in the FF. Moreover, it is capable of detecting error pulses with wide width and hard errors occurring on the combinational parts. The proposed FFs are constructed by modifying the conventional soft-error-tolerant FFs [10].

The rest of this paper is organized as follows: Section 2 shows construction and problem of the two conventional soft-error-tolerant FFs [10] related to the proposed FF. Section 3 explains the proposed FFs, and evaluation results of the proposed methods are given in Sect.4. Finally, Sect.5 concludes the paper.

Manuscript received January 30, 2009.

Manuscript revised April 13, 2009.

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^{**}The earlier version of this paper was presented at the 23rd IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'08).

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DOI: 10.1587/transinf.E92.D.1534

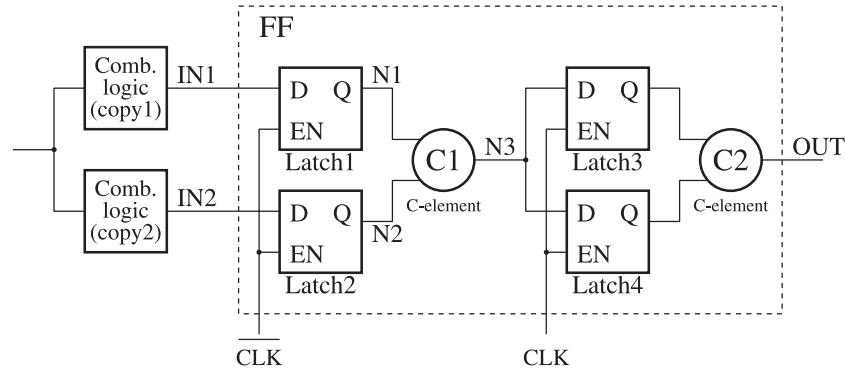


Fig. 1 Construction of soft-error-tolerant FF using duplication [10].

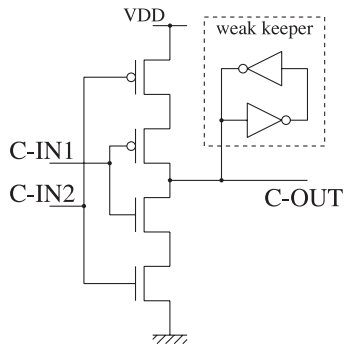
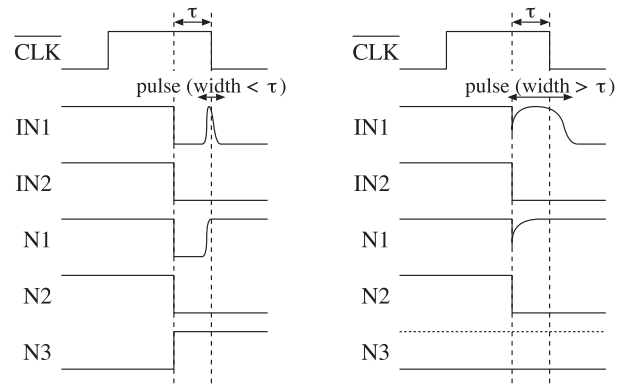


Fig. 2 Structure of C-element.

Table 1 Truth table of C-element.

C-IN1	C-IN2	C-OUT
0	0	1
1	1	0
0	1	previous value retained
1	0	previous value retained



(a) correctable error pulse (b) uncorrectable error pulse

Fig. 3 Correctable and uncorrectable error pulse on conventional FFs using duplication [10].

2. Previous Works Behind Proposed One

The proposed FF is constructed based on two types of conventional soft-error-tolerant FFs: namely ones using duplication and ones using time-shifted outputs [10]. This section shows a brief description and a problem of the conventional FFs.

2.1 Error Correction Using Duplication

Figure 1 shows the construction of the conventional soft-error-tolerant FFs using duplication [10]. The FFs are capable of correcting soft errors occurring in combinational logic circuits and latches. The FF is based on a master-slave FF and comprises four latches; Latch1, Latch2, Latch3 and Latch4. Latch1 and Latch2 function as master latches. Meanwhile, Latch3 and Latch4 function as slave latches. The FF also comprises two C-elements; C1 and C2. The structure of the C-element is illustrated in Fig. 2. Table 1 shows the truth table of the C-elements. Every C-element has two inputs, and it works as an inverter if the values of both inputs are the same. If they differ from each other, the output of the C-element retains the previous logic value kept by weak keepers (loops of two inverters). In circuits using the FF, the clock cycle has to be set to be longer than $T + \tau$, where T is the maximal propagation delay time of the combinational logic circuit and τ is a time longer than the expected maximal time of correctable soft error pulse

width.

Figure 3(a) shows an example of a waveform chart in case that a soft error pulse with width of narrower than τ occurs on combinational parts of circuits using the FF. The figure illustrates waveforms of inverted clock signals CLK; output signals of the combinational logic circuit (i.e. the input signal of the master latches Latch1 and Latch2), namely signals IN1, IN2; the output of the master latches N1, N2; and the output of the C-element C1 connected to the slave latches, namely N3. In the example, the soft error occurs at IN1, but the C-element C1 outputs correct value (logic 1, in the example). Like the example, even if soft errors occur on combinational parts, only if the width of the pulses is narrower than τ , the errors are corrected and do not affect the operation of the circuit. It is because there is always a period longer than τ after the output values of the combinational

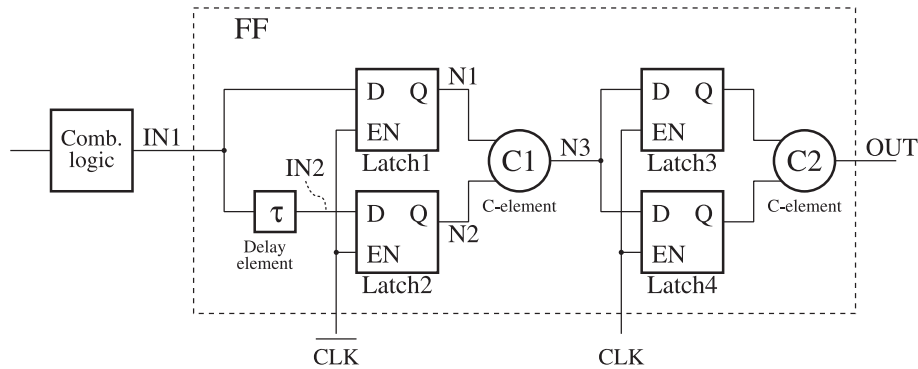


Fig. 4 Construction of soft-error-tolerant FF using time-shifted outputs [10].

logic circuits are decided and before the master latches are closed. As a result, even if such a pulse occurs, there is always a period that the both input values of the C-element C1 correspond to the correct value at least once before closing of the master latches. So, even if the value of either N1 or N2 becomes incorrect after the closing, N3 keeps correct value using the weak keeper of C1. In addition, even if soft errors occur in the FF, it is corrected by the C-elements and thus they do not affect the operation. The detail reason is explained in [10].

Figure 3 (b) illustrates an example of a waveform chart in case that a soft error pulse with width wider than τ occurs at the input of the FF. In the example, the error pulse starts before the output values of the combinational logic circuit are decided and ends after the clock signal changes from 1 to 0 closing the master latches. There is not a period that the both input values of C1 correspond to the correct value after the output values of the combinational logic circuit are decided and before the master latches are closed. Then, the output values of C1 and the FF (i.e. values of N3) end up with incorrect value. As the example, error pulses with width wider than τ are not always corrected in the FFs.

2.2 Error Correction Using Time-Shifted Output

Figure 4 shows the construction of the conventional soft-error-tolerant FFs using time-shifted outputs [10]. The construction is similar to the FF shown in Fig. 1. Unlike Fig. 1, the combinational logic circuit is not duplicated and a delay element of delay τ is inserted at the input of one of master latches (Latch 2, in Fig. 4). In circuits using the FF, the clock cycle is set to be longer than $T + 2\tau$.

The FF is capable of correcting soft errors with width narrower than τ occurring on combinational logic circuits and latches, like the FF in Fig. 1. The detail reason is explained in [10]. Figure 5 (a) shows an example of a waveform chart in case that a soft error pulse with width of narrower than τ occurs on combinational parts of circuits using the FF. The C-element C1 outputs the correct value.

Figure 5 (b) illustrates an example of a waveform chart in case that a soft error pulse with width wider than τ occurs in the combinational logic circuit. There is a period that error pulses appear at the inputs of both latches simul-

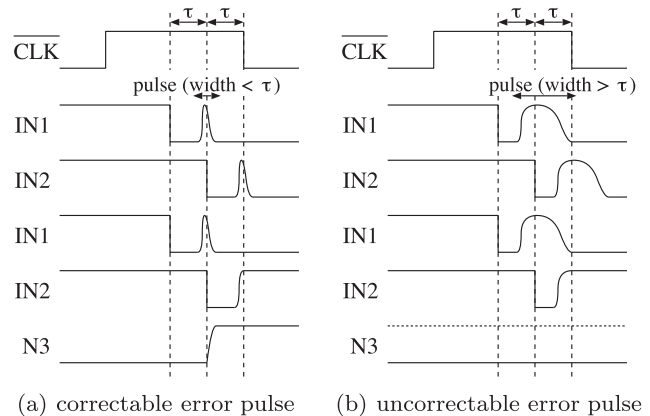


Fig. 5 Correctable and uncorrectable error pulse on conventional FFs using time-shifted outputs [10].

taneously, and thus there is not a period that the both input values of C1 correspond to the correct value after the output values of the combinational logic circuit are decided and before the master latches are closed. So, the output values of C1 and the FF end up with incorrect value.

3. Proposed Flip-Flop

Figure 6 shows a structure of the proposed soft-error-tolerant FF capable of detecting wide error pulse with width wider than τ . It is based on a master slave FF and comprises six latches; M1, D1, M2, D2, S1 and S2. The latches M1, D1, M2 and D2 function as a master latch while the latches S1 and S2 function as a slave latch. The FF also comprises three C-elements; C1, C2 and C3. Signal CLK is expressed as the inversion of clock signal CLK. While the slave latch part of the proposed FF is constructed in the same manner as the conventional FF shown in Fig. 4, the master latch part of proposed FF is constructed by duplicating the master latch part of the conventional FF in Fig. 4. Concretely speaking, M1, D1 and C1 form the same construction of the master latch part of the conventional FF. In addition, M2, D2 and C2 also form the same construction. The outputs of the C-elements C1 and C2 are connected to the inputs of a two-input XOR gate. The XOR gate detects uncorrectable wide error pulses. The output value becomes 1 only when uncor-

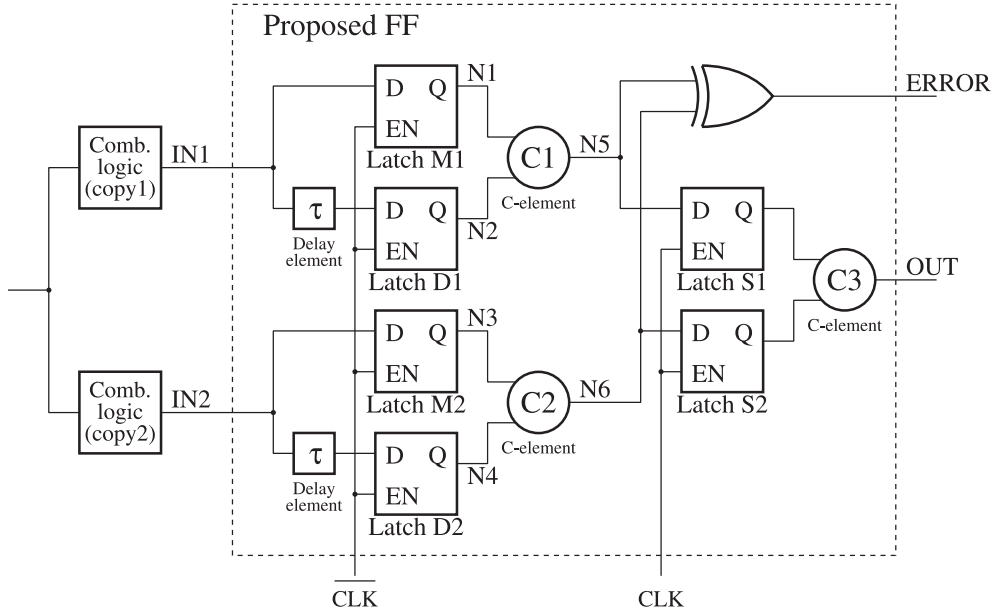


Fig. 6 Construction of proposed soft-error-tolerant FF.

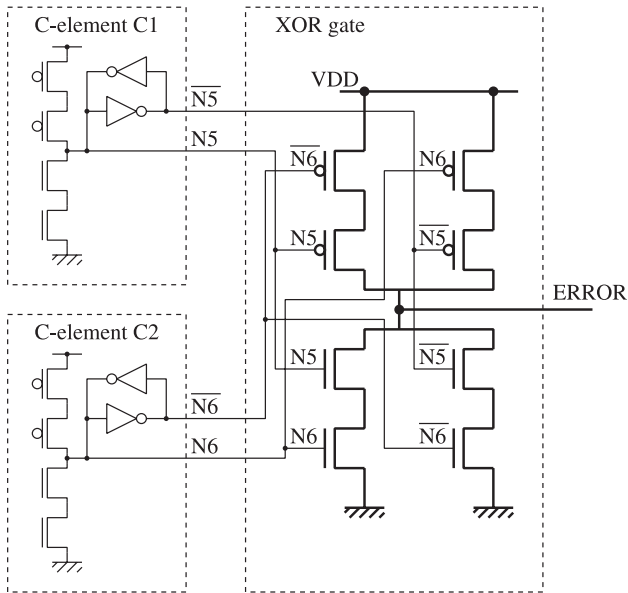


Fig. 7 XOR gate and C-elements in proposed FF.

rectable errors occur. The XOR gate can be constructed as shown in Fig. 7. The XOR gate requires not only the signals $N5$, $N6$ but also the inverted signals $\overline{N5}$, $\overline{N6}$ as inputs. The C-elements C1 and C2 includes weak keepers, and the inverted signals $\overline{N5}$, $\overline{N6}$ obtained by the inverter in the weak keeper can be used as the inputs of the XOR gate.

Next, how to correct and/or detect soft errors are explained.

(1) Soft error pulses with width narrower than τ :

The master latch part of the proposed FF is composition by duplicating the master latch part of the conventional FF using time-shifted outputs introduced in 2.2. Needless to say,

each of them works just like the master latch part of the conventional FF. So, even if soft error pulses with width narrower than τ appear at the input of the FF, the output values of the master latch part, i.e. the output values of the C-elements C1 and C2, become correct. So, the input and output values of S1, S2 and the C-element C3 also become correct. Moreover, both input values of the XOR become the same correct values and no errors are detected. In sum, the FF works correctly.

(2) Soft error pulses occurring in FF:

The pair of latches in the FFs, (M1, D1), (M2, D2), and (S1, S2), certainly takes the same value when no errors occur. Therefore, the soft error pulses can be corrected like the conventional FFs.

(3) Soft error pulses with width wider than τ /Hard errors:

Suppose an error pulse occurs on the combinational logic circuit copy1, without loss of generality. Since M1, D1, and the C-element C1 form the same construction as the master latch part of the conventional FF using time-shifted outputs, from the discussion in 2.2, the output values of the C-element C1, i.e. values of $N5$, may become incorrect. Needless to say, the output value of the C-element C2, i.e. values of $N6$, is correct because it does not depend on the output of copy1. If the output value of the C-element C1 is correct, the FF works correctly like the case (1). If it is incorrect, both input values of the XOR gate, i.e. values of $N5$, $N6$, differ from each other and the error is detected.

This paper does not discuss operation after the detection. It will be decided by system designers. For example, the designers can construct a fail-safe system with the proposed FF to stop the system in a harmless fashion after the detection. They can also construct a recomputation system to recover the system.

4. Evaluation

4.1 Simulation Environment

To evaluate the proposed FFs, simulations are made for the following three FFs: the proposed FFs, the FFs using duplication [10], and the FFs using time-shifted outputs [10]. Various efficient delay elements have been designed [23]. In this paper, as the delay elements in the proposed FFs and the conventional FFs using time-shifted outputs; six, eight and ten inverters connected in series are used. In this section, the proposed FFs using the six, eight and ten inverters are expressed as PFF_I6, PFF_I8, and PFF_I10, respectively. Similarly, the conventional FFs using time-shifted outputs are expressed as TFF_I6, TFF_I8, and TFF_I10, respectively. The conventional FFs using duplication is expressed as “Dual FF”. Every FF is designed in an industrial $0.18\mu\text{m}$ technology with Virtuoso Layout Editor and simulated by HSPICE. The gate widths of PMOS and NMOS are set to $5.0\mu\text{m}$ and $2.0\mu\text{m}$, respectively, except the inside inverter in the weak keeper (i.e. the inverter whose output is the output of the weak keeper). The gate lengths of both PMOS and NMOS are set to $0.18\mu\text{m}$ except the inside inverter. The driving capability of C-elements strongly depends on the size of the inside inverter. The gate widths of PMOS and NMOS in the inside inverters are set to $2.0\mu\text{m}$ and $0.80\mu\text{m}$, respectively. The gate lengths of both PMOS and NMOS are set to $0.50\mu\text{m}$. Supply voltage is 1.8 V and a clock cycle is 4.0 ns. In this section, the FFs are evaluated from the viewpoint of soft-error-tolerant capability, AC characteristics, area overhead and power consumption.

4.2 Soft-Error-Tolerant Capability

Figure 8 illustrates the waveforms obtained by the simulation of the proposed FFs using the delay elements with ten inverters, namely PFF_I10. The figure shows the waveforms of the following signals: the inverted clock signals $\overline{\text{CLK}}$; the output signals of the combinational logic circuits (i.e. the input signals of the master latches Latch1 and Latch2), namely the signals IN1 and IN2; the output of the C-elements C1 and C2, namely the signals N5 and N6; and the output of the XOR connected back to the C-elements C1 and C2, namely the signal ERROR. The horizontal axis illustrates time (ns), and the vertical axis illustrates voltage (V). Figures 8 (a), (b) and (c) show the simulation results for soft error pulses with widths of 0.36 ns, 0.595 ns and 0.80 ns, respectively. Figure 8 (d) shows the results that a hard error occurs. The soft error pulses occur at the output of the combinational logic circuit copy1, namely the signal IN1. It means that the error pulses affect the output of the C-element C1 and do not affect that of the C-element C2. The pulse occurs at the time about 7–8 ns. In the time, the correct value is zero and the pulses change the value from zero to one.

In the example shown in Fig. 8 (a), a narrow soft error pulse with the width of 0.36 ns occurs. The waveform at the

output of the C-element C1 is very similar to that of the C-element C2. It means that the soft error pulse is corrected. Similar results are obtained for soft error pulses with the width of 0.01–0.594 ns.

In the example shown in Fig. 8 (b), a soft error pulse with the width of 0.595 ns occurs. Like this, in case that soft error pulses with the width of 0.594–0.599 ns, for just a moment, the output voltages of the C-element C1 and the XOR gate change to about 1.4–1.8 V. However, they return to the correct voltages, soon. The change does not affect the output value of the FF and the circuits connected to the XOR gates. So, we can regard the soft error pulses are corrected.

In the example shown in Fig. 8 (c) and (d), a wide error pulse with the width of 0.80 ns and a hard error occur, respectively. The output value of the C-element C1 becomes incorrect and that of the XOR gate turns on. It means that the errors are detected. Similar results are obtained for soft error pulses with the width of 0.60 ns or wider and for hard errors.

As described above, the proposed FF PFF_I10 can correct error pulses with the width of 0.60 ns or narrower. The maximal width of correctable error pulses depends on delay elements. Table 2 shows the relationship of the number of inverters in the delay elements and correctable error pulse width for the proposed FFs.

4.3 Other Results

Table 3 shows AC characteristic of the each FFs with delay elements consisting of six, eight and ten inverters. The AC characteristic includes CLK-Q delay time, setup time and hold time. The CLK-Q delay times of the proposed FFs are shorter than those of the conventional FFs. It is because the inputs of the slave latches of the proposed FFs are supplied from different C-element (i.e. C-element C1 and C2) unlike the conventional FFs. The setup/hold times of the proposed FFs are longer than those of the conventional FFs using duplication. For the proposed FFs and the conventional FFs using time-shifted outputs, delay elements with long delay time bring large setup time. The setup/hold time of the proposed FFs are almost the same as those of the conventional FFs using time-shifted output with the same delay elements.

Table 4 shows area ratio to “dual FF” and dynamical power consumption of the each FF with delay elements consisting of six, eight and ten inverters. The power consumption means average power consumption in 0–14 ns (i.e. 3.5 clock cycles). The areas and power consumption of the proposed FFs are larger than those of the conventional FFs.

5. Conclusion

This paper presented a construction of soft-error-tolerant FFs. The proposed FFs have the capability to detect soft error pulses having wide width outside a specified range as well as the capability to correct those having narrow width within the specified one. The proposed FFs are also capable of detecting hard errors. The proposed FFs are evalu-

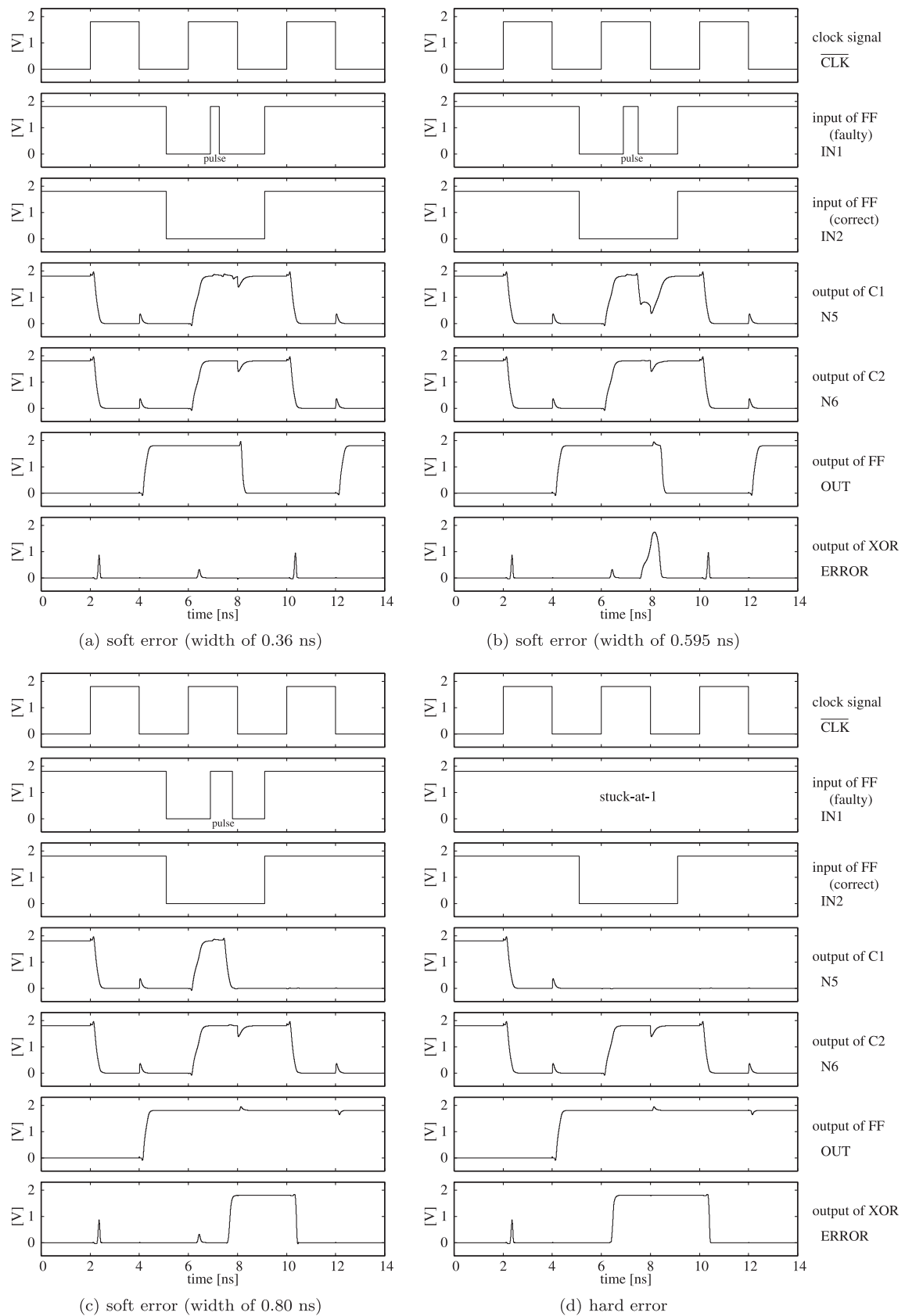


Fig. 8 Waveform of signals on proposed FF that soft/hard error occurs.

Table 2 Number of inverters in delay elements v.s. maximal width of correctable error pulses (ns).

FF	width
PFF_I6	0.45
PFF_I8	0.52
PFF_I10	0.60

Table 3 AC characteristic.

FF	CLK-Q delay (ns)		D-CLK time (ns)	
	rising	falling	setup	hold
Dual FF [10]	0.275	0.243	0.069	–0.067
TFF_I6 [10]	0.275	0.243	0.352	–0.349
TFF_I8 [10]	0.275	0.243	0.436	–0.433
TFF_I10 [10]	0.275	0.243	0.520	–0.517
PFF_I6	0.240	0.205	0.352	–0.349
PFF_I8	0.240	0.205	0.435	–0.433
PFF_I10	0.240	0.205	0.519	–0.516

Table 4 Area ratio and average power consumption.

FF	area ratio	power (mW)
Dual FF [10]	1.000	0.229
TFF_I6 [10]	1.281	0.277
TFF_I8 [10]	1.375	0.292
TFF_I10 [10]	1.469	0.306
PFF_I6	2.218	0.476
PFF_I8	2.406	0.507
PFF_I10	2.593	0.538

ated from the viewpoint of soft-error-tolerant capability, AC characteristics, area overhead and power consumption.

In the proposed FFs, soft error pulses with wide width are only detected but not corrected. Even if wide error pulses occur, we can recover systems using the detection capability as long as the systems support recomputations. However, in general, recomputations require large time overhead, and thus the proposed FFs are not suitable for critical mission systems that require a fast recovery from wide error pulses. For such critical mission systems, efficient soft-error-tolerant FFs capable of correcting wide error pulses should be presented in future works.

The authors assume that, like other soft-error-tolerant FFs, it is difficult to detect manufacturing defects occurring in the proposed FF, such that the defects affect only soft-error-tolerant capability but do not affect error-free normal operations. To clarify the testability of the proposed FF is an important future work. If it is difficult, development of manufacturing testing for the proposed FF is another important future work.

Acknowledgments

This work was supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation, Toppan Printing Corporation, Synopsys, Inc., Cadence Design Systems, Inc. and Mentor Graphics, Inc. This work was partially supported by the Grant-in-Aid for Scientific Research (C) No.19560335.

References

- [1] T. Karnik, P. Hazucha, and J. Patel, "Characterization of soft errors caused by single event upsets in CMOS processes," *IEEE Trans. Dependable & Secure Comput.*, vol.1, no.2, pp.128–143, 2004.
- [2] S. Mitra, N. Seifert, M. Zhang, Q. Sbi, and K.S. Kim, "Robust system design with built-in soft-error resilience," *IEEE Des. Test Comput.*, vol.38, no.2, pp.43–52, Feb. 2005.
- [3] L.T. Wang, C.W. Wu, and X. Wen, *VLSI test principles and architectures: Design for testability*, Morgan Kaufmann, 2006.
- [4] E. Fujiwara, *Code design for dependable systems: Theory and practical applications*, Wiley-Interscience, 2006.
- [5] M. Nicolaidis, "Design for soft error mitigation," *IEEE Trans. Device & Mater. Reliab.*, vol.5, no.3, pp.405–418, Sept. 2005.
- [6] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol.43, no.6, pp.2874–2878, Dec. 1996.
- [7] Y. Komatsu, Y. Arima, T. Fujimoto, T. Yamashita, and K. Ishibashi, "A soft-error hardened latch schemes for SoC in a 90 nm technology and beyond," *Proc. IEEE Custom Integr. Circuit Conf.*, pp.324–332, 2004.
- [8] Y.S. Dhillon, A.U. Diril, A. Chatterjee, and C. Metra, "Load and logic co-optimization for design of soft-error resistant nanometer CMOS circuits," *Proc. 11th IEEE Int'l On-Line Testing Symp.*, pp.35–40, 2005.
- [9] M. Fazeli, A. Patooghy, S.G. Miremadi, and A. Ejlali, "Feedback redundancy: A power efficient SEU-tolerant latch design for deep sub-micron technologies," *Proc. 37th Annu. IEEE/IFIP Int'l Conf. on Dependable Syst. & Netw.*, pp.276–285, 2007.
- [10] S. Mitra, M. Zhang, S. Waqas, N. Seifert, B. Gill, and K.S. Kim, "Combinational logic soft error correction," *Proc. IEEE Int'l Test Conf.*, pp.824–832, 2006.
- [11] M. Nicolaidis, "Time redundancy-based soft-error tolerance to rescue nanometer technologies," *Proc. IEEE VLSI Test Symp.*, pp.86–94, 1999.
- [12] R. Naseer and J. Draper, "The DF-DICE storage element for immunity to soft errors," *Proc. IEEE Int'l Midwest Symp. Circuit & Syst.*, pp.303–306, 2005.
- [13] K.J. Hass, J. Gambles, B. Walker, and M. Zampaglione, "Mitigating single event upsets from combinational logic," *Proc. 7th NASA Symp. VLSI Des.*, pp.4.1.1–4.1.10, 1998.
- [14] M. Zhang and N.R. Shanbhag, "Dual-sampling skewed CMOS design for soft-error tolerance," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol.53, no.12, pp.1461–1465, Dec. 2006.
- [15] W. Wang and H. Gong, "Edge triggered pulse latch design with delayed latching edge for radiation hardened application," *IEEE Trans. Nucl. Sci.*, vol.51, no.6, pp.3626–3630, Dec. 2004.
- [16] S. Krishnamohan and N.R. Mahapatra, "A highly-efficient technique for reducing soft errors in static CMOS circuits," *Proc. 22nd IEEE Int'l Conf. Comp. Des.*, pp.126–131, 2004.
- [17] J. Kumar and M.B. Tahoori, "A low power soft error suppression technique for dynamic logic," *Proc. 20th IEEE Int'l Symp. Defect Fault Tolerance VLSI Syst.*, pp.454–462, 2005.
- [18] Y. Sasaki, K. Namba, and H. Ito, "Soft error masking circuit and latch using Schmitt trigger circuit," *Proc. 21st IEEE Int'l Symp. Defect Fault Tolerance VLSI Syst.*, pp.327–335, 2006.
- [19] B. Narasimham, B.L. Bhuvu, R.D. Schrimpf, L.W. Massengill, M.J. Gadlage, O.A. Amusan, W.T. Holman, A.F. Witulski, W.H. Robinson, J.D. Black, J.M. Benedetto, and P.H. Eaton, "Characterization of digital single event transient pulse-widths in 130-nm and 90-nm CMOS technologies," *IEEE Trans. Nucl. Sci.*, vol.54, no.6, pp.2506–2511, Dec. 2007.
- [20] B. Narasimham, R.L. Shuler, J.D. Black, B.L. Bhuvu, R.D. Schrimpf, A.F. Witulski, W.T. Holman, and L.W. Massengill, "Quantifying the reduction in collected charge and soft errors in the presence of guard rings," *IEEE Trans. Device & Mater. Reliab.*,

vol.8, no.1, pp.203–209, March 2008.

- [21] C.A. Lisboa, F.L. Kastensmidt, E.H. Neto, G. Wirth, and L. Carro, “Using built-in sensors to cope with long duration transient faults in future technologies,” *Proc. IEEE Int’l Test Conf.*, pp.1–10, 2007.
- [22] R.G. Useinov, G.I. Zebrev, V.V. Emelianov, V.S. Persbenkov, and V.N. Ulimov, “Physical model of single heavy ion induced hard errors,” *Proc. 7th IEEE Eur. Conf. Radiat. & its Eff. Comp. & Syst.*, pp.249–252, 2003.
- [23] G. Kim, M.K. Kim, B.S. Chang, and W. Kim, “A low-voltage, low-power CMOS delay element,” *IEEE J. Solid-State Circuits*, vol.31, no.7, pp.966–971, July 1996.



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