PAPER

Design for Delay Fault Testability of Dual Circuits Using Master and Slave Scan Paths

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SUMMARY This paper proposes a scan design for delay fault testability of dual circuits. In normal operation mode, each proposed scan flip flop operates as a master-slave flip flop. In test mode, the proposed scan design performs scan operation using two scan paths, namely master scan path and slave scan path. The master scan path consists of master latches and the slave scan path consists of slave latches. In the proposed scan design, arbitrary two-patterns can be set to flip flops of dual circuits. Therefore, it achieves complete fault coverage for robust and non-robust testable delay fault testing. It requires no extra latch unlike enhanced scan design. Thus the area overhead is low. The evaluation shows the test application time of the proposed scan design is 58.0% of that of the enhanced scan design, and the area overhead of the proposed scan design is 13.0% lower than that of the enhanced scan design. In addition, in testing of single circuits, it achieves complete fault coverage of robust and non-robust testable delay fault testing. It requires smaller test data volume than the enhanced scan design in testing of single circuits.

key words: *dual circuits, master and slave scan paths, delay fault testing, concurrent error detection, DFT*

1. Introduction

As technology advances into the deep-submicron regime, designs are becoming increasingly more sensitive to various noise sources [1], [2]. Excessive noise can cause performance degradation and signal integrity problems. It can corrupt the system-level data integrity. It can also significantly affect the timing performance.

Concurrent error detection techniques with dual circuits are expected to ensure data integrity of today's deep submicron devices. Fault detection in such designs can be done by comparing output responses of dual circuits when identical input sequences are applied to them. (In this paper, single circuits mean conventional circuits without redundant circuits for fault detection.) Many works related to this have been presented. Mitra et al. analyzed the design diversity metric and reliability of concurrent error detection quantitatively [3]. They also presented the combinational logic synthesis for diversity of concurrent error detection [4]. Recently, [5] presented a soft error masking technique using a duplicated circuit. Pomeranz et al. analyzed the nature of fault recovery of concurrent-online testing [6], and online transition fault testing using identical circuits [7]. The author's group proposed concurrent online testing approaches using an embedded reconfigurable core [8], [9].

The amount of transistors on dual circuits is at least twice as large as that of a single circuit. This has a bad influence on test costs. Therefore, test cost reduction of dual circuits is more important than that of single circuit. It is now widely accepted that stuck-at fault testing can no longer satisfactorily test the functionality of fabricated integrated circuits in nanometer technologies. Unfortunately, traditional functional at-speed testing suffers from huge amount of test development costs, and limited effectiveness. Furthermore, limited test access to internal registers makes application of at-speed functional tests impractical. Therefore, scan based structural delay fault testing, which can significantly improve the controllability and observability, appears to be the practical approach for the delay fault testing. Some previous works related to the scan based delay fault testing are shown as follows. Broad-side testing, skewed-load testing, and enhanced scan testing are well-known scan based delay fault testing techniques [10], [11]. The broad-side and skewed-load testing use the standard scan design, and thus the area overheads for those methods are not high. However fault coverage is low because those methods permit the application of only strongly limited test patterns to circuit under test (CUT). The enhanced scan design achieves complete fault coverage [10]. However, the scan flip flop for the scan design requires additional redundant latches. This additional latches give bad influence on the area overhead. A scan design with the flip flops for delay fault testing without extra latches was proposed [12]. The important difference between the scan flip flop for the scan design and the standard scan flip flop is the manner of connecting to the adjacent scan flip flops. This scan design is almost equivalent to the enhanced scan design from the viewpoint of fault coverage, test application time, and required memory size for ATE in spite of having the same area overhead as standard scan design. However, the testability of dual circuits is not considered in these scan designs.

The dual circuits consumes additional area at least twice of the original circuit. Therefore, chip designers decide which cores or modules should be duplicated considering the critical parts and the limited area in general. Accordingly, scan design applied to the chip is desired to be able to test both dual circuits and single circuits.

This paper proposes a scan design for delay fault testability of dual circuits. In test mode, the proposed scan design performs scan operation using scan chains with two scan

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paths, namely master scan path and slave scan path. This scan architecture increases the delay fault testability of dual circuits. In testing of single circuits, it achieves complete fault coverage of robust and non-robust testable delay fault testing. In addition, it requires smaller test data volume than the enhanced scan design in testing of single circuits.

The rest of this paper is organized as follows. Section 2 presents the detail of the proposed scan design. Section 3 evaluates the effectiveness of the proposed scan design. Section 4 shows how to apply the proposed scan design to single circuits. Finally, Sect. 5 concludes this paper.

2. Scan Design for Delay Fault Testability of Dual Circuits

This section explains the proposed scan design. First, Sect. 2.1 describes an overview of the proposed scan design. Section 2.2 explains the architecture of the proposed flip flop and the scan design. Section 2.3 explains operation modes of the proposed scan design. Section 2.4 shows the delay fault testing using the proposed scan design.

2.1 Overview

Figure 1 shows dual circuits for concurrent error detection using the proposed scan design. It consists of two identical combinational circuits C_i ($i = 0, 1$), two sets of scan flip flops, $FF_{00}, FF_{10}, \cdots, FF_{0i}, FF_{1i}, \cdots, FF_{0(n-1)}, FF_{1(n-1)}$, and an error checker E. The combinational circuit C_i includes l primary inputs, $x_{i0}, \cdots, x_{i(l-1)}$, m primary outputs, $f_{i0}, \cdots, f_{i(m-1)}$, n state inputs, $y_{i0}, \cdots, y_{i(n-1)}$, and n state outputs, $z_{i0}, \cdots, z_{i(n-1)}$. The error checker circuit E has inputs from z_{ij} and f_{ij}, and an output line Err. In this figure, the input lines from f_{ij} are left out for the convenience of space. The output Err is activated if a fault occurs.

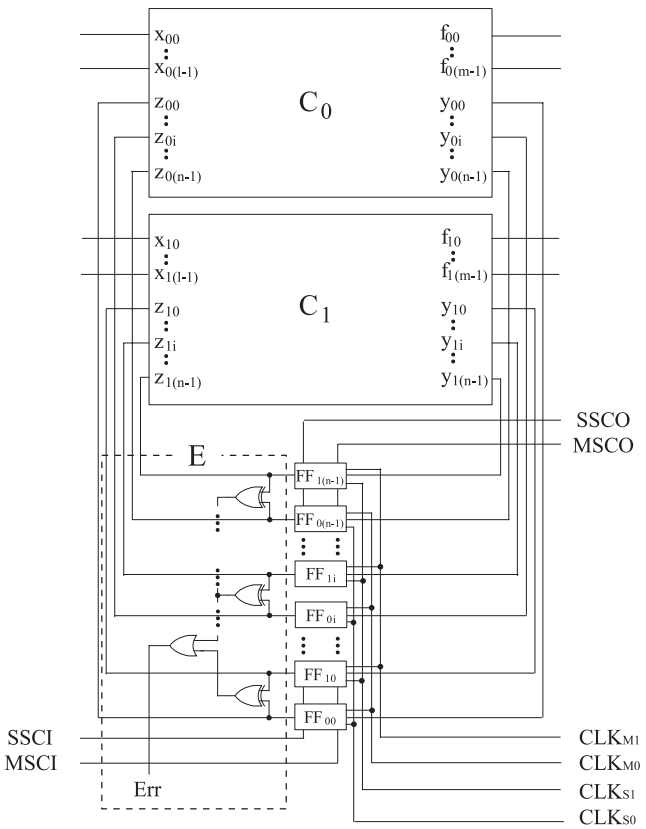

Fig. 1 Dual circuits using proposed flip flops.

2.2 Architecture of Proposed Flip Flop

The proposed scan flip flop FF_{ij} consists of a master latch L_{Mij} and a slave latch L_{Sij}. These latches are both positive latches, which capture input values when clock signal is 1, and keep the captured values when clock signal is 0. Figure 2 illustrates the detail of the proposed scan design. In this figure, $2n$ proposed flip flops, $FF_{00}, FF_{10}, \cdots, FF_{0i}, FF_{1i}, \cdots, FF_{0(n-1)}, FF_{1(n-1)}$, are arranged coincident with ones in Fig. 1. As shown with the two dotted lines in the figure, two scan paths, called master scan path and slave scan path, consisting of only master latches and of only slave latches are constructed, respectively. The master (slave) scan path is with a scan input MSCI (SSCI) and a scan output MSCO (SSCO), and 2 to 1 selectors. The inputs, $D_{00}, D_{10}, \cdots, D_{0i}, D_{1i}, \cdots, D_{0(n-1)}, D_{1(n-1)}$ are connected from $y_{00}, y_{10}, \cdots, y_{0i}, y_{1i}, \cdots, y_{0(n-1)}, y_{1(n-1)}$ in Fig. 1, and the outputs, $Q_{00}, Q_{10}, \cdots, Q_{0i}, Q_{1i}, \cdots, Q_{0(n-1)}, Q_{1(n-1)}$ are connected to $z_{00}, z_{10}, \cdots, z_{0i}, z_{1i}, \cdots, z_{0(n-1)}, z_{1(n-1)}$. One bit control signal SE controls the two 2 to 1 selectors. The four clocks, CLK_{M0}, CLK_{S0}, CLK_{M1}, CLK_{S1}, control L_{M0i}, L_{S0i} L_{M1i}, L_{S1i}, respectively. Note that these clocks are independent each other.

2.3 Operations in Proposed Scan Design

The proposed scan design has two operation modes, normal operation mode and test mode.

In normal operation mode, SE = 0, and each flip flop FF_{ij} operates as a master-slave flip flop. The clocks for master latches, CLK_{M0} and CLK_{M1}, are provided the same signal, while the clocks for slave latches, CLK_{S0} and CLK_{S1}, are provided the inverted signal of the clocks for master latches.

In test mode, SE = 1, and the proposed scan design performs scan operation using two scan paths, namely master scan path and slave scan path. Each pair of $\{L_{M0i}, L_{M1i}\}, \{L_{S0i}, L_{S1i}\}$ $(0 \le i \le n-1)$ plays the role of the master-slave flip flop for scan operation during test mode. Thus, the clock control of CLK_{M0} and CLK_{M1}, which control L_{M0i} and L_{M1i}, respectively, should be complementary. For same reason, the clock control of CLK_{S0} and CLK_{S1} should be complementary. Because of these clock controls, the value stored in a closed latch is equal to the one stored in the next opened latch. In the proposed scan design, testing using the proposed scan design, scan operations of master and slave scan path are performed simultaneously to reduce scan-in

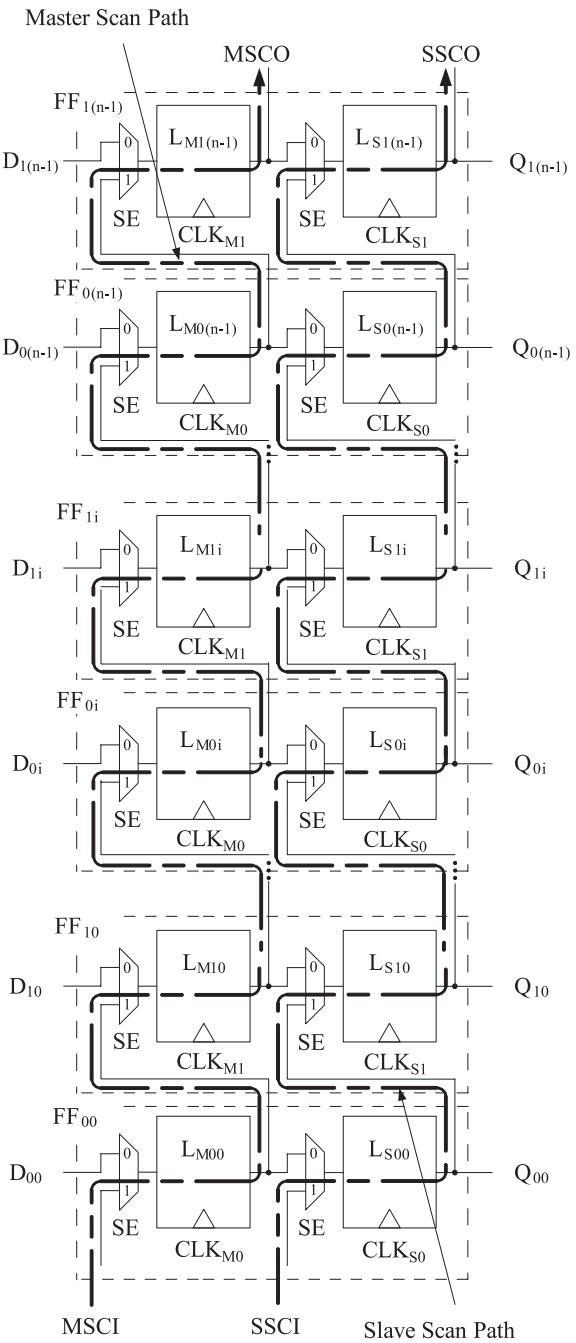

Fig. 2 Master scan path and slave scan path.

and scan-out time to the half.

2.4 Delay Fault Testing in Proposed Scan Design

In this subsection, delay fault testing with the proposed scan design is explained. First, we explain the sequence from the scan-in operation of a test vector to the scan-out operation of the test response. The test sequence is divided into the following four steps.

Step 1 The initial vector and transition vector of a two-patterns are scanned-in into slave scan path from SSCI and into master scan path from MSCI, respectively, after SE is set to test mode.

Step 2 Transitions are launched into the circuit under test, after SE is set to normal operation mode. One clock later, test responses are captured into the corresponding master latches.

Step 3 The test responses captured into L_{M1i} are transferred to the corresponding slave latches, L_{S1i}.

Step 4 Finally, SE is set to test mode again. After that, test responses are retrieved from MSCO and SSCO.

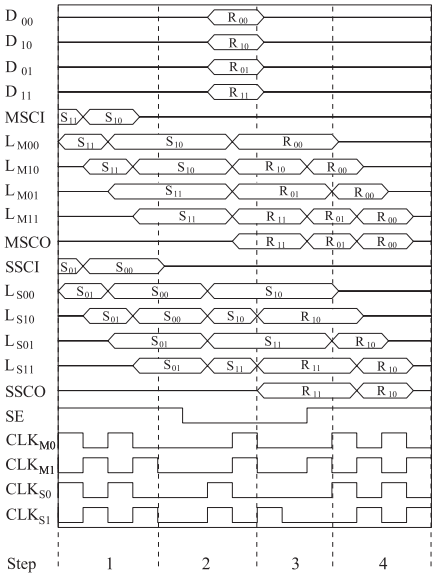

Fig. 3 Timing chart of the proposed delay fault test sequence for concurrent error detection.

Figure 3 shows the timing chart when $n = 2$ in Fig. 2. In Step 4, scan-out operations of master scan path and slave scan path are performed simultaneously. For the parallel scan-out operation, just only the test responses captured into L_{M1i} are transferred to the corresponding slave latches, L_{S1i} in Step 3. Therefore, as shown in the timing chart, CLK_{S1} is open, while CLK_{S0} is close during the first 0.5 cycles of Step 3. To make the phase of master scan path same as that of slave scan path for the scan-out operation in Step 4, CLK_{M1} is opened, and other clocks are closed at the last 0.5 clock cycle of Step 3. When the scan length is $2n$, Step 1 and Step 4 require n clocks, while Step 2 requires constant 2 clock, and Step 3 requires constant 1.5 clock. If these steps are executed sequentially, the test application time is $T_c = N_{tp}\,(2n+3.5)$, where N_{tp} is the number of test patterns. However, Step 1 for the next test pattern and Step 4 can be executed simultaneously. Therefore, the test application time T_c is formulated as follows.

$$T_c = N_{tp}(n + 3.5) + n. \tag{1}$$

In Step 1 and Step 4, scan operations of both master and slave scan paths are performed simultaneously. However, because the clock controls of these scan paths are independent each other, high accuracy of the clock synchronization

Table 1 Comparison of scan designs for robust path delay fault test in case of dual circuits.

	# of	TAT (clock)				TATO (%)				FC (%)	
	RTPDF	SS	ES	CS	PS	SS	ES	CS	PS	SS	ES,CS,PS
s298	343	766	2,204	2,489	1,292	34.8	100.0	112.9	58.6	66.8	100.0
s344	611	1,715	4,623	5,192	2,679	37.1	100.0	112.3	57.9	67.4	100.0
s349	611	1,698	4,687	5,264	2,716	36.2	100.0	112.3	57.9	67.3	100.0
s382	667	614	1,994	2,559	1,355	30.8	100.0	128.3	68.0	61.2	100.0
s386	413	934	1,896	2,433	1,289	49.3	100.0	128.3	68.0	84.0	100.0
s420.1	948	6,784	16,506	18,438	9,474	41.1	100.0	111.7	57.4	76.8	100.0
s444	586	1,861	4,905	5,339	2,741	37.9	100.0	108.8	55.9	58.2	100.0
s510	729	1,518	3,702	4,755	2,514	41.0	100.0	128.4	67.9	58.8	100.0
s526	694	1,953	5,785	6,299	3,231	33.8	100.0	108.9	55.8	62.8	100.0
s641	1,979	5,626	11,579	12,726	6,522	48.6	100.0	109.9	56.3	99.8	100.0
s713	1,184	3,085	5,619	6,170	3,169	54.9	100.0	109.8	56.4	100.0	100.0
s820	980	1,832	3,377	4,499	2,394	54.2	100.0	133.2	70.9	92.1	100.0
s832	984	1,846	3,413	4,547	2,419	54.1	100.0	133.2	70.9	92.4	100.0
s838.1	3,428	42,804	114,938	121,886	61,838	37.2	100.0	106.0	53.8	72.1	100.0
s953	2,302	12,739	29,669	31,631	16,084	42.9	100.0	106.6	54.2	78.0	100.0
s1196	3,581	13,718	29,088	32,139	16,466	47.2	100.0	110.5	56.6	100.0	100.0
s1238	3,589	13,438	26,656	29,451	15,090	50.4	100.0	110.5	56.6	100.0	100.0
s5378	37,058	-	472,499	477,658	239,619	-	100.0	101.1	50.7	-	100.0
s9234	33,034	-	540,210	544,812	273,167	-	100.0	100.9	50.6	-	100.0
s13207	41,222	-	64,989	64,847	32,949	-	100.0	99.8	50.7	-	100.0
s38417	16,134	-	53,446,412	53,510,890	26,764,834	-	100.0	100.1	50.1	-	100.0
s38584	160,914	-	3,442,156	3,446,166	1,724,764	-	100.0	100.1	50.1	-	100.0
Average	-	-				43.0	100.0	112.4	58.0	78.7	100.0

between the master clocks (CLK_{M0} and CLK_{M1}) and slave clocks (CLK_{S0} and CLK_{S1}) is not so much required.

On the other hand, high accuracy of the clock synchronization of CLK_{M0} with CLK_{M1} for the scan operations of the master scan path, and the one of CLK_{S0} with CLK_{S1} for the scan operations of the slave scan paths should be guaranteed. In addition, in Step 2, Step 3, and normal operation mode, high accuracy of the clock synchronization of CLK_{M0} with CLK_{S0}, and that of CLK_{M1} with CLK_{S1} should be guaranteed.

3. Evaluation

The proposed scan design is evaluated in the following subsections. In the evaluation, the proposed scan design is compared with the three conventional scan designs: the standard scan design, the enhanced scan design, and the Chiba scan design [12]. The Chiba scan flip flop has similar architecture to the proposed scan flip flop. The difference is the number of scan paths. The Chiba scan design has only the master scan path in test mode, while the proposed scan design has the master scan path and the slave scan path. Section 3.1 evaluates the test application time of the proposed scan design. Section 3.2 evaluates the area of the proposed flip flop and the circuits with the proposed scan design. Section 3.3 evaluates the clock accuracy for the scan operation.

3.1 Test Application Time

In the evaluation, the parameter of increase ratio of test application time, TATO, is introduced. It is calculated by the following formula:

$$\frac{\text{(TAT when applied the evaluated scan design)}}{\text{(TAT when applied ES)}}, \quad (2)$$

where TAT is test application time, and ES is the enhanced scan design. Delay fault test data sets for robust testable delay fault is generated by the ATPG implemented by C language. In this evaluation, the checker circuit E is not included in the circuit under test. The evaluation is performed with common number of scan channels. The number of scan channels is two in this evaluation.

The routing of the scan chains of the proposed scan design is shown in Fig. 2. The evaluation results of the standard scan design and the Chiba scan design depend on the routing of the scan chains. The evaluated circuits applied the Chiba scan design have one scan path routed via $FF_{00}, FF_{10}, \cdots, FF_{0(n/2-1)}, FF_{1(n/2-1)}$ and the other scan path routed via $FF_{0n/2}, FF_{1n/2}, \cdots, FF_{0(n-1)}, FF_{1(n-1)}$ sequentially. This routing permits to apply arbitrary two-patterns like the proposed scan design. The evaluated circuits applied the standard scan designs have one scan chain routed via $FF_{00}, \cdots, FF_{0(n-1)}$ and the other scan path routed via $FF_{10}, \cdots, FF_{1(n-1)}$ sequentially. The routing permits to test each circuit of dual circuits as a single circuit using both of broad-side testing and skewed-load testing method. On the other hand, the evaluation results of the enhanced scan design does not depend on the routing of the scan chains.

Table 1 shows the evaluation result on ISCAS89 benchmarks. The "# of RTPDF" column shows the number of robust testable paths. To get the number of robust testable paths, each path of the path list is checked whether it is robust sensitizable or not using the ATPG algorithm with infinite backtrack limit before test generation.

The TAT and TATO columns show the test application

time and the increase ratio of the test application time, respectively. The FC column shows the fault coverage. The subcolumns, SS, ES, CS, PS, show the result of the standard scan design, the enhanced scan design, the Chiba scan design, and the proposed scan design, respectively.

The test application time of the proposed scan design is lower than that of the enhanced scan design. It is because both the first pattern and second pattern can be scanned-in simultaneously in the proposed scan design. From the evaluation result, it is 58.0% of that of the enhanced scan design on average. On the other hand, because the test response stored in either even numbered flip flops or odd numbered flip flops are retrieved in the Chiba scan design, the test application time of the Chiba scan design is larger than that of the enhanced scan design on average. From the evaluation result, it is 112.4% of that of the enhanced scan design on average. The test application time of the standard scan design is 43.0% of the enhanced scan design, which is 15.0% smaller than that of the proposed scan design.

Arbitrary two-patterns can be applied to each of dual circuits using the enhanced scan design, the Chiba scan design, and the proposed scan design. Thus, the test generations for these scan designs are made under the same restrictions that arbitrary two-patterns can be applied to all flip flops. Therefore, under the assumption of using common ATPG algorithm, test data sets for the three scan designs are the same. On the other hand, because the second pattern of the standard scan based delay fault testing methods depends on the first pattern, arbitrary two-patterns cannot be applied to each of dual circuits using it.

Therefore, the enhanced scan design, the Chiba scan design, and the proposed scan design achieve complete fault coverage, while the standard scan design does not. In this evaluation, the fault coverage of the enhanced scan design, the Chiba scan design, and the proposed scan design are 100.0%, while the average value of the fault coverage of the standard scan design is 78.7%.

3.2 Area Overhead

This section evaluates the area overhead of the proposed scan flip flop and the scan design. The area overhead of the scan flip flop is calculated by the following formula:

$$\frac{\text{(Area of the evaluated scan flip flop)}}{\text{(Area of the normal flip flop)}} - 1.$$

The area overhead of the scan design is calculated by following formula:

$$\frac{\text{(Area of dual circuits with the evaluated scan design)}}{\text{(Area of dual circuits with no scan design)}} - 1.$$

Note that in this formula, the area of circuits does not include the error checker circuit E.

Each flip flop is implemented by the standard cells of Rohm 0.35 μm^2 design rule. Table 2 shows the evaluation result of the area overhead of the flip flops. The AR and AO columns show the area of each flip flop and the area overhead, respectively. The area overhead of the standard scan flip flop, the Chiba scan flip flop, the proposed scan flip flop, and the enhanced scan flip flop are 25.0%, 18.0%, 42.9%, and 64.4%, respectively. Therefore, the area overhead of the proposed scan flip flop is 17.9% larger than the standard scan flip flop, 24.9% larger than the Chiba scan flip flop, and 21.5% smaller than the enhanced scan flip flop.

Table 2 Comparison of area overhead of scan flip flops.

FF	AR	AO
Master Slave	693	0.0
Std. Scan	866	25.0
Chiba Scan	817	18.0
Prop. Scan	990	42.9
Enh. Scan	1139	64.4

AR: Area of FF (μm^2)
AO: Area overhead (%)

Table 3 Comparison of area overhead of scan design.

	ES		CS		PS	
	AR	AO	AR	AO	AR	AO
s5378	0.286	39.1	0.230	11.9	0.261	27.0
s9234	0.377	36.9	0.304	10.3	0.343	24.6
s13207	0.948	48.1	0.729	14.0	0.849	32.7
s15850	0.926	42.9	0.725	11.8	0.838	29.3
s35932	2.490	44.8	1.950	13.4	2.249	30.7
s38417	2.51	41.0	1.995	11.9	2.279	27.8
s38584	2.603	31.1	2.158	8.7	2.410	21.4

AR: Area of circuit (mm^2), AO: Area overhead (%)

Table 3 shows the evaluation result of the area overhead of the scan designs on ISCAS89 benchmarks. The ES, CS, PS columns show the evaluation result of the enhanced scan design, the Chiba scan design, and the proposed scan design, respectively. Each evaluation result column is divided into two subcolumns. The AR subcolumn shows the area with the evaluated flip flops. The AO subcolumn shows the area overhead. The area overhead of the Chiba scan design, the proposed scan design, and the enhanced scan design are 11.7%, 27.6%, and 40.6% on average, respectively. Therefore, the area overhead of the proposed scan flip flop is 15.9% larger than the one of the Chiba scan flip flop, and 13.0% smaller than the one of the enhanced scan flip flop.

3.3 Clock Accuracy

As described in Sect. 2.4, the proposed scan design requires high accuracy of the clock synchronization for the scan operation of each scan path. Here, for the quantitative estimation of the required clock accuracy, we calculate the clock margins of the master scan path and the slave scan path. In the proposed scan design, two clock lines control the scan operation for a scan path. One controls the master latches of the scan path. The other controls the slave ones. For example, in case of the master scan path of Fig. 2, CLK_{M0} controls the master latches, and CLK_{M1} controls the slave latches. Theoretically, no relative delay between CLK_{M0} and CLK_{M1} occurs, but in fact the relative delay between them does. In this evaluation, we analyze how much re-

lateive delay is permitted for the correct scan operation. We define the relative delay ΔT as the following formula:

$$\Delta T = T_{CLK_S} - T_{CLK_M},$$

where T_{CLK_M} is the propagation delay of the clock for the master latches, and T_{CLK_S} is that for the slave latches. We assume that the propagation delay of the clock for the master latches is fixed in this evaluation. For the evaluation we define the clock margin mrg as the following formula:

$$mrg = \Delta T_{max} - \Delta T_{min}, \quad (3)$$

where ΔT_{max} is the maximum relative delay of the slave clocks for normal operation, and ΔT_{min} is the minimum relative delay. If the relative delay is between ΔT_{max} and ΔT_{min}, the scan path works, otherwise does not.

For the calculation, we measure ΔT_{max} and ΔT_{min} with SPICE simulation. We measure those of the scan paths comprised of six proposed flip flops. The technology used in this evaluation is Rohm 0.35 μm. For the measurement, repetitive scan-in data of 4-bit sequence "1000" are shifted-in from the scan input continuously. We search ΔT_{max} and ΔT_{min} by sweeping the relative delay controlling the slave clock with 0.02 ns width and monitoring the output value of each latch of the measured scan path.

Table 4 shows the result. The column freq. shows the clock frequency. The columns "master scan path" and "slave scan path" show the evaluation results of each scan path. They have sub-columns ΔT_{max}, ΔT_{min}, and margin. The column margin shows the clock margin calculated by Eq. (3). The result shows that in all the evaluated clock frequencies ΔT_{max}s of the master scan path and the slave scan path are 0.16 ns and 0.14 ns, respectively. In all the evaluated clock frequencies, ΔT_{min}s of master scan path and slave scan path are constant value, −0.16 ns and −0.14 ns, respectively. Therefore, in any evaluated clock frequency, the clock margin of master scan path and slave scan path are 0.32 ns and 0.28 ns, respectively. The maximum delay of an inverter is 0.041 ns, and thus the permitted relative delays of the master scan path and the slave scan path are equal to about that of seven inverters and that of six inverters, respectively. The scan paths must be routed according to the clock margins.

Figure 4 shows the wave forms of a SPICE simulation of the master scan operation when the relative delays are around ΔT_{max} or ΔT_{min}. The clock frequency is 100 MHz. The relative delay of the wave forms (a) and (b) are ΔT_{min} −0.16 ns and −0.18 ns, respectively. On the other hand, the relative delay of wave forms (c) and (d) are ΔT_{max} 0.16 ns and 0.18 ns, respectively. Each wave form represents data signal. The lines, L_{M10}, L_{M11} L_{M12} are the output wave forms of the master latches. These latches work as the slave latches during the scan operation. The line MSCI is the wave form of the master scan input.

Both the wave forms (a) and (c) are normal. The scan-in data 1 is shifted from L_{M10} to L_{M12} correctly. The horizontal three arrows show the pulse width of the wave forms of L_{M10}, L_{M11} L_{M12}. You can observe that the pulse widths of these wave forms are equal to the clock width, and they do not overlap each other. Both the wave forms (b) and (d) are abnormal. Unlike the wave form (a), the positive edges of L_{M11}, L_{M12} of the corresponding wave forms (b) begin around 53.0 ns and 62.5 ns, respectively. Thus the pulse width of them are larger than the clock width. Unlike the wave form (c), the positive edges of L_{M10}, L_{M11}, L_{M12} of the corresponding wave forms (d) begin around 48.0 ns, 53.0 ns, 58.0 ns, respectively. Thus the pulse widths of them are larger than the clock width, too.

Table 4 Clock margin.

freq. (MHz)	master scan path			slave scan path		
	ΔT_{max}	ΔT_{min}	margin	ΔT_{max}	ΔT_{min}	margin
10	0.16 ns	−0.16 ns	0.32 ns	0.14 ns	−0.14 ns	0.28 ns
50	0.16 ns	−0.16 ns	0.32 ns	0.14 ns	−0.14 ns	0.28 ns
100	0.16 ns	−0.16 ns	0.32 ns	0.14 ns	−0.14 ns	0.28 ns

4. Delay Fault Test Sequence for Single Circuits

This section explains the delay fault test sequence and evaluation in case that the proposed scan design with two scan paths is applied to single circuits, that is, conventional single circuits, not dual circuits. Figure 5 illustrates a normal sequential circuit applied the proposed scan design. The circuit consists of a combinational circuit **C** and the proposed scan flip flops FF_i ($0 \leq i \leq n-1$). The clock CLK_{ME} controls the master latches of FF_{2i}, and CLK_{SE} controls the slave latches of FF_{2i}. The clock CLK_{MO} controls the master latches of flip flops FF_{2i+1}, and CLK_{SO} controls the slave latches of FF_{2i+1}. The combinational circuit **C** includes l primary inputs, $x_0, \cdots, x_{l-1}$, m primary outputs, $f_0, \cdots, f_{m-1}$, n state inputs, $y_0, \cdots, y_{n-1}$, and n state outputs, $z_0, \cdots, z_{n-1}$.

Delay fault test sequence from scan-in operation of a test vector to scan-out operation of the test response is as follows.

Step 1 The odd-numbered bits of an initial vector are scanned-in into slave scan path from SSCI, and the even-numbered bits of the initial vector are scanned-in into master scan path from MSCI simultaneously, after SE is set to test mode.

Step 2 The even-numbered bits of the initial vector stored in master latches are transferred into the corresponding slave latches, after SE is set to normal operation mode.

Step 3 A transition vector is scanned-in from MSCI, after SE is set to test mode again.

Step 4 Transitions are launched to the circuit under test, after SE is set to normal operation mode. When the proposed scan design is applied into single circuits, only either even-numbered flip flops FF_{2i} or odd-numbered flip flops FF_{2i+1} can launch transitions into the circuit under test exclusively. One clock later, the test responses are captured into the corresponding master latches.

Step 5 The test responses captured into L_{M2i+1} are transferred to the corresponding slave latches, L_{S2i+1}.

Step 6 The test responses are retrieved from MSCO, and SSCO, after SE is set to test mode again.

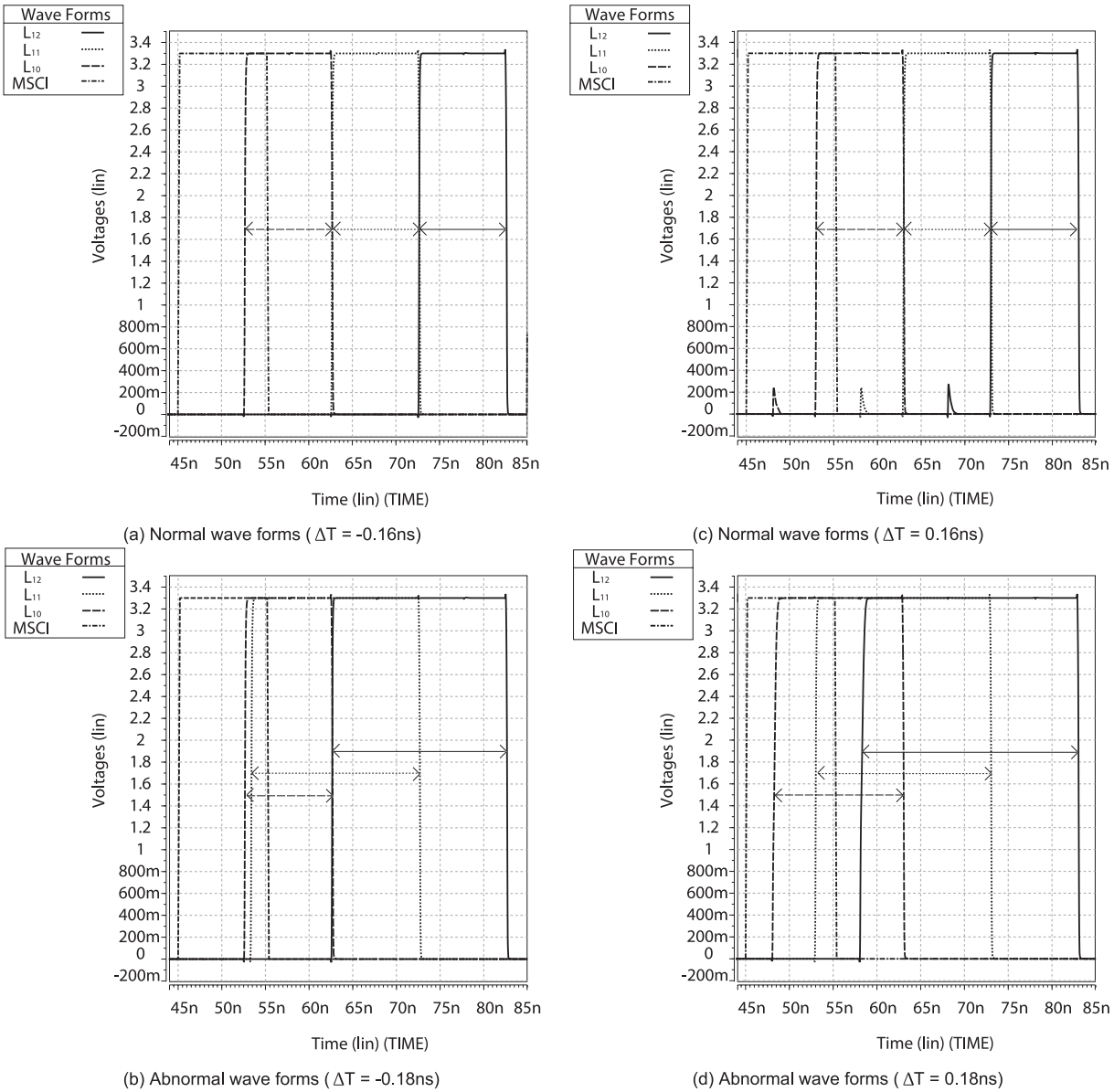

Fig. 4 Example of normal wave forms and abnormal wave forms. scan path: master scan path, clock frequency: 100 MHz, x range: 44–84 (ns).

When the proposed scan design is applied into dual circuits, each flip flops can launch arbitrary transitions. However, when the proposed scan design is applied into single circuits, only either even-numbered flip flops FF_{2i} or odd-numbered flip flops FF_{2i+1} can launch transitions into the circuit under test at a time. However, under the proposed scan design, arbitrary one bit transition can be launched at least. Thus complete fault coverage of robust and non-robust testable fault is guaranteed [13], [14]. Figure 6 shows the timing chart from Step 1 to Step 6, when $n = 4$.

We evaluate the number of test pattern, test data volume, test application time, and fault coverage when the proposed scan design is applied into single circuits. In this evaluation, the number of test patterns, and test data volume are evaluated using the parameter of the increase ratio of the number of test patterns and the test data volume, respectively. The increase ratio of the number of test patterns, TPO, is calculated by the following formula:

$$\frac{\text{(\# of TP when applied the evaluated scan design)}}{\text{(\# of TP when applied ES)}},$$

where TP is test patterns, and ES is the enhanced scan design.

The increase ratio of the test data volume, TDVO, is calculated by the following formula:

$$\frac{\text{(TDV when applied the evaluated scan design)}}{\text{(TDV when applied ES)}},$$

where TDV is the test data volume, and ES is the enhanced scan design. As the previous evaluation, the proposed scan

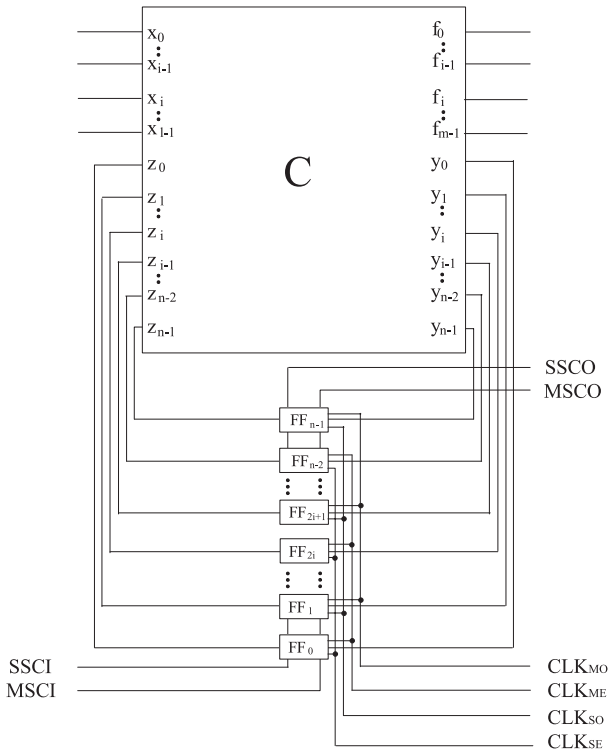

Fig. 5 Single circuit applied proposed flip flops.

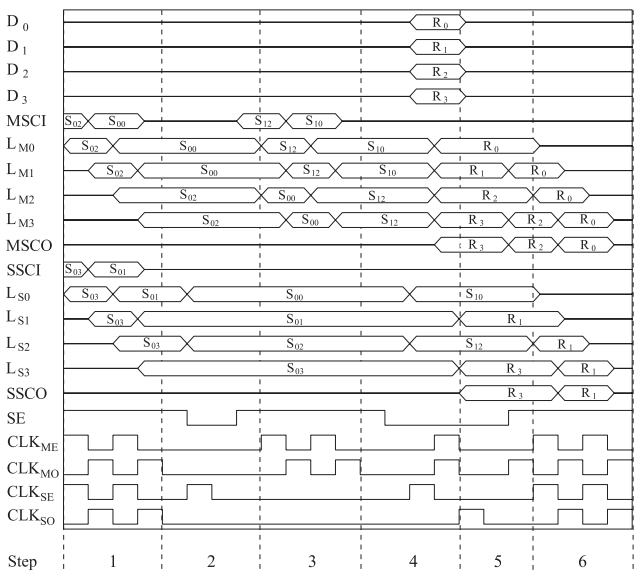

Fig. 6 Timing chart of the proposed delay fault test sequence for single circuits.

design is compared with the Chiba scan design and the enhanced scan design.

Table 5 shows the evaluation result of the number of test patterns and test data volume on ISCAS89 benchmarks. The first column shows each benchmark circuit name. The second column shows the number of test patterns. The third column TPO shows the increase of the number of test pattern. The column TDV shows the test data volume. The column TDVO shows the increase ratio of test data volume. The rows Max., Ave., Min. show the maximum, the average, the minimum TDVO in evaluated benchmark circuits, respectively.

The columns, # of test pattern, TPO, TDV, TDVO are divided into subcolumns, ES, CS, PS, respectively. The subcolumns ES, CS, PS show the results of the enhanced scan design, the Chiba scan design, and the proposed scan design, respectively.

According to the average value of TDVO, the test data volume of the proposed scan design is smaller than that of the enhanced scan design. This result shows that the proposed scan design has the effect of delay fault test data compression. One of the reasons why the proposed scan design has the effect is that the required test data volume per a test of the proposed scan design is smaller than that of the enhanced scan design. Therefore, the average value of TDVO of the proposed scan design tends to be smaller than 100.0%. The average value of TDVO of the proposed scan design is 93.4%, while that of the Chiba scan design is 108.1%.

Table 6 shows the evaluation result of the test application time and the fault coverage. The TAT and TATO columns show the test application time and the increase ratio of the test application time, respectively. The FC column shows the fault coverage. The rows Max., Ave., Min. show the maximum, the average, the minimum TATO in the evaluated benchmark circuits, respectively. The increase ratio of the test application time is calculated by Eq. (2). The fault coverage is 100.0% in every scan design. The average value of TATO shows that the test application time of the proposed scan design is longer than that of the enhanced scan design and the Chiba scan design. However, the average value of TATO is within 20%.

The result of s35932 shown in Tables 5 and 6 seems to be peculiar compared with those of other circuits. On this circuit, the parameters TPO, TDVO, TATO of the proposed scan design are more than 1.5 times as large as those of the enhanced scan design, respectively. As described before, when the proposed scan design is applied into single circuits, arbitrary two-patterns cannot be applied to circuits. Only either even-numbered flip flops FF_{2i} or odd-numbered flip flops FF_{2i+1} can launch transitions into the circuit under test at a time. From the evaluation results, the restriction gives bad influence on the test cost of s35932 compared with other evaluated circuits.

5. Conclusions

This paper proposes a scan design for delay fault testability of dual circuits. The most important difference between conventional scan design and the proposed scan design is scan operation using two scan paths, namely master scan path and slave scan path. In the proposed scan design, arbitrary two-patterns can be set to flip flops of the dual circuits. Therefore, it achieves complete fault coverage for robust and non-

Table 5 Number of test patterns and test data volume in case of single circuits.

	# of test pattern			TPO			TDV (bit)			TDVO (%)		
	ES	CS	PS	ES	CS	PS	ES	CS	PS	ES	CS	PS
s298	73	111	74	100.0	152.1	101.4	3,942	4,440	3,478	100.0	112.6	88.2
s344	144	199	137	100.0	138.2	95.1	10,656	11,810	9,179	100.0	110.8	86.1
s349	146	206	137	100.0	141.1	93.8	10,804	12,241	9,179	100.0	113.3	85.0
s382	142	201	132	100.0	141.5	93.0	10,650	10,957	8,580	100.0	102.9	80.6
s386	135	166	141	100.0	123.0	104.4	5,265	5,478	5,076	100.0	104.0	96.4
s420.1	485	518	499	100.0	106.8	102.9	41,225	35,742	38,423	100.0	86.7	93.2
s444	111	193	124	100.0	173.9	111.7	8,325	10,515	8,060	100.0	126.3	96.8
s510	264	326	256	100.0	123.5	97.0	16,632	18,582	15,360	100.0	111.7	92.4
s526	131	182	153	100.0	138.9	116.8	9,825	9,923	9,945	100.0	101.0	101.2
s641	289	325	256	100.0	112.5	88.6	43,639	43,074	36,352	100.0	98.7	83.3
s713	140	197	139	100.0	140.7	99.3	21,000	25,892	19,599	100.0	123.3	93.3
s820	281	364	282	100.0	129.5	100.4	19,670	23,865	19,176	100.0	121.3	97.5
s832	284	363	285	100.0	127.8	100.4	19,880	23,795	19,380	100.0	119.7	97.5
s838.1	1,741	1,806	1,774	100.0	103.7	101.9	287,265	240,198	264,326	100.0	83.6	92.0
s953	494	736	507	100.0	149.0	102.6	70,148	83,511	64,896	100.0	119.0	92.5
s1196	765	815	686	100.0	106.5	89.7	73,440	63,570	59,682	100.0	86.6	81.3
s1238	701	723	672	100.0	103.1	95.9	67,296	56,394	58,464	100.0	83.8	86.9
s5378	1,312	1,582	1,383	100.0	120.6	105.4	860,672	755,394	784,161	100.0	87.8	91.1
s9234	1,179	2,052	1,314	100.0	174.0	111.5	877,176	1,058,832	827,820	100.0	120.7	94.4
s13207	1,123	1,860	1,185	100.0	165.6	105.5	2,459,370	2,886,720	2,217,135	100.0	117.4	90.2
s35932	48	97	80	100.0	202.1	166.7	267,552	373,062	376,800	100.0	139.4	140.8
Max.	-	-	-	100.0	202.1	166.7	-	-	-	100.0	139.4	140.8
Ave.	-	-	-	100.0	136.9	104.0	-	-	-	100.0	108.1	93.4
Min.	-	-	-	100.0	103.1	88.6	-	-	-	100.0	83.6	80.6

Table 6 Test application time and fault coverage in case of single circuits.

	TAT (clock)			TATO (%)			FC (%)		
	ES	CS	PS	ES	CS	PS	ES	CS	PS
s298	1,175	1,447	1,450	100.0	123.1	123.4	100.0	100.0	100.0
s344	2,600	2790	2,817	100.0	107.3	108.3	100.0	100.0	100.0
s349	2636	2888	2,817	100.0	109.6	106.8	100.0	100.0	100.0
s382	3419	3825	3,509	100.0	111.9	102.6	100.0	100.0	100.0
s386	1083	1164	1,625	100.0	107.5	150.0	100.0	100.0	100.0
s420.1	8738	7256	10,737	100.0	83.0	122.9	100.0	100.0	100.0
s444	2675	3673	3,297	100.0	137.3	123.3	100.0	100.0	100.0
s510	2115	2284	2,947	100.0	108.0	139.3	100.0	100.0	100.0
s526	3155	3464	4,066	100.0	109.8	128.9	100.0	100.0	100.0
s641	6368	5530	6,282	100.0	86.8	98.6	100.0	100.0	100.0
s713	3090	3354	3,416	100.0	108.5	110.5	100.0	100.0	100.0
s820	2251	2550	2,964	100.0	113.3	131.7	100.0	100.0	100.0
s832	2275	2543	2,996	100.0	111.8	131.7	100.0	100.0	100.0
s838.1	59210	46964	66,541	100.0	79.3	112.4	100.0	100.0	100.0
s953	15823	18408	17,507	100.0	116.3	110.6	100.0	100.0	100.0
s1196	15309	13045	16,130	100.0	85.2	105.4	100.0	100.0	100.0
s1238	14029	11573	15,801	100.0	82.5	112.6	100.0	100.0	100.0
s5378	237,562	215,592	255,253	100.0	90.8	107.4	100.0	100.0	100.0
s9234	271,284	355,053	306,933	100.0	130.9	113.1	100.0	100.0	100.0
s13207	753,868	937,142	799,617	100.0	124.3	106.1	100.0	100.0	100.0
s35932	83,904	126,338	139,544	100.0	150.6	166.3	100.0	100.0	100.0
Max.	-	-	-	100.0	150.6	166.3	100.0	100.0	100.0
Ave.	-	-	-	100.0	108.5	119.6	100.0	100.0	100.0
Min.	-	-	-	100.0	79.3	98.6	100.0	100.0	100.0

robust testable delay fault testing unlike the standard scan based delay fault testing methods. In addition, it requires no extra latch, unlike the enhanced scan design. Thus the area overhead is low. The evaluation shows the test application time of the proposed scan design is 58.0% of that of the enhanced scan design, while the area overhead of the proposed scan design is 13.0% lower than that of the enhanced scan design.

In testing of single circuits, it achieves complete fault coverage of robust and non-robust testable delay fault testing of normal circuits with lower area overhead than the enhanced scan design. In addition, it requires smaller test data volume than the enhanced scan design. Thus when a test compression technique such as Illinois scan chain [15]

is applied, the circuits with the proposed scan design are expected to require smaller compressed data volume than those with the enhanced scan design. The evaluation is the future work.

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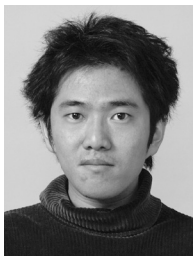

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