FOREWORD

Special Section on Test, Diagnosis and Verification of SOCs

The Seventeenth Asian Test Symposium (ATS'08) and the Ninth Workshop on RTL and High Level Testing (WRTLT'08) were held in Sapporo, Japan in November, 2008. A lot of excellent works on state-of-the-art test technologies were presented in ATS'08, while WRTLT'08 provided a forum for more frank discussion focusing on register transfer level and high level testing. Taking this opportunity, we planed this special section to solicit and encourage researches on test, diagnosis and verification of SOCs.

We had 11 submissions of full papers and the Editorial Committee selected 5 full papers for publication through careful reviews. The accepted works cover test power reduction, test data reduction, test pattern generation and analog testing.

The Guest Editors would like to appreciate all authors for their submissions and give our thanks to the reviewers for their professional and voluntary works. Finally we would like to express our appreciation to the Guest Associate Editors for their dedicated and continuous contributions to the editorial process. Their names and affiliations are listed below.

Guest Editors-in-Chief:
Kazumi Hatayama (STARC), Tsuyoshi Shinogi (Mie Univ.)
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Kazumi Hatayama and Tsuyoshi Shinogi, Guest Editors-in-Chief

Kazumi Hatayama *(Member)* received his B.S., M.S. and Ph.D. degrees in applied mathematics and physics from Kyoto University, Kyoto, Japan, in 1976, 1978 and 1982, respectively. He is now a Team Leader in Test & Diagnosis Group in Semiconductor Technology Academic Research Center (STARC). He is Asia Pacific Regional Chair of Test Technology Technical Council, IEEE Computer Society, IP Track Co-Chair of VLSI Test Symposium and Program Committee member of International Test Conference and other conferences. He is a senior member of IEEE and a member of IPSJ, ORSJ and REAJ. His research interests include DFT, BIST, ATPG, fault diagnosis and fault tolerant computing.

Tsuyoshi Shinogi *(Member)* received his B.S. and M.S. degrees in information science from Tokyo Institute of Technology, Tokyo, Japan, in 1977 and 1979, respectively. He received his Ph.D. degree in engineering from Mie University, Mie, Japan, in 1998. He is now a professor in Graduate School of Engineering, Mie University. He is a member of IEEE and IPSJ. His research interests include LSI testing and embedded systems.