LETTER

A Selective Scan Chain Activation Technique for Minimizing Average and Peak Power Consumption

Yongjoon KIM[†*a)], **Jaeseok PARK**[†], *Nonmembers*, *and* **Sungho KANG**[†], *Member*

SUMMARY In this paper, we present an efficient low power scan test technique which simultaneously reduces both average and peak power consumption. The selective scan chain activation scheme removes unnecessary scan chain utilization during the scan shift and capture operations. Statistical scan cell reordering enables efficient scan chain removal. The experimental results demonstrated that the proposed method constantly reduces the average and peak power consumption during scan testing.

key words: *design for testability (DfT), scan testing, scan cell reordering, low power test*

1. Introduction

In the modern semiconductor manufacturing process, a large proportion of the resources are devoted to testing which necessitate high costs. Therefore, most of the test methods fully utilize test resources to increase test efficiency. This maximal utilization of test resources causes another critical testing issue: power consumption [1]. Test modes require increased power consumption compared to normal operation mode since there are many test resources which are not executed during normal mode. Test patterns themselves also increase power consumption due to the minimization of correlation between successive patterns, which results in significant switching activities in both combinational and sequential elements.

Average power and peak power are two measures for estimating power consumption. The former is the amount of power consumed over a long period of operation, and the latter is the highest value of the instantaneous power, the amount of power consumed during a small instant of time. Excessive average power, which can lead to structural damage or decreased reliability, can be controlled by reducing the scan clock frequency. However, this can increase test time and thereby increase test costs. Therefore, several methods have been proposed to reduce average power [2]–[4]. A scan chain segmentation method [2] was proposed to reduce scan shift power. A scan chain is partitioned into multiple chains, and the clock gating scheme enables the scan chains that need to be accessed. An alternative scan chain disabling method has been proposed [3] which enables scan chains via a single selection input. Efficient scan chain disabling control schemes for low power testing have also been proposed for low power testing [4]. They are based on scan chain partitioning and circuit blocking during scan shift operations, but they cannot give a proper solution for low power capture operations. Unlike average power, excessive peak power may erroneously change the logic state, which causes some good dies to fail the test, thereby leading to yield loss. Therefore, peak power consumption should also be reduced. Many studies have been proposed for peak power minimization [5], [6]. However, they require significant hardware overhead or do not sufficiently reduce the power to be viable options.

In this paper, we present a new low power scan test method using a selective scan chain activation technique. A scan chain is reordered based on the statistical analysis of the specified bits for each scan cell. After the scan cell reordering, each test pattern is analyzed to remove the useless scan chains during scan shift and capture operations. Using this method, power consumption during scan shift and capture operations are dramatically reduced without a loss of fault coverage.

2. Proposed Power Reduction Technique

2.1 Selection of Removable Scan Chain

A test pattern is a bit stream of 0 s, 1 s, and many unspecified (X) bits, and recent research shows that the majority of test patterns are composed of 'don't care' bits [7]. Scan segmentation for scan chain removal is based on this characteristic of the test patterns. Figure 1 presents an example of scan chain removal. As shown in Fig. 1 (a), a single scan chain with 12 scan cells requires 12 scan shift operations followed by a capture cycle. However, if this scan chain is partitioned into three scan chains as presented in Fig. 1 (b), the second scan chain does not needed to be shifted in and out, since the test data are all Xs. To manage the scan operation of these partitioned scan chains, a scan input control scheme is required. Therefore, power consumption during the scan shift operations can be reduced using the scan segmentation technique. However, power consumption of the capture operations should also be considered for reducing peak power consumption.

To appropriately remove scan chains during shift and capture operations, the following requirements should be satisfied. Let C, N, and P be the number of scan cells, the number of scan chains, and the number of test patterns, respectively.

Manuscript received August 25, 2009.

[†]The authors are with the Dept. of Electrical & Electronic Eng., Yonsei University, Seoul, Korea.

a) E-mail: yjkim@soc.yonsei.ac.kr

DOI: 10.1587/transinf.E93.D.193

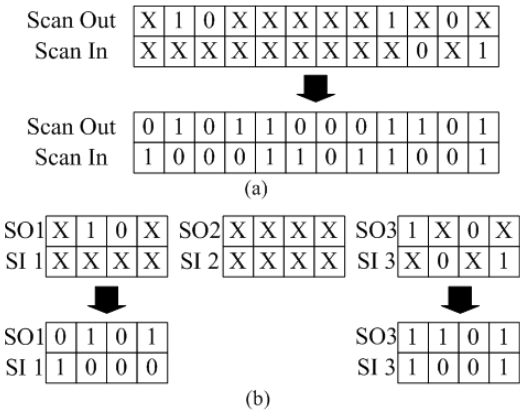

Fig. 1 An example of scan chain removal.

•(*Lemma* 1: Elimination of a scan cell the during capture cycle) If a scan cell S_k $(0 \leq k \leq C-1)$ is unspecified for a test response R_i $(0 \leq i \leq P-1)$, S_k can be disabled while applying the i-th capture operation.
•(*Lemma* 2: Elimination of a scan cell during the shift cycle) If a scan cell S_k $(0 \leq k \leq C-1)$ is unspecified for a test response R_i $(0 \leq i \leq P-1)$ and for the next input test vector T_i+1, S_k can be disabled while applying the (i+1)-th shift operation.
•(*Lemma* 3: Elimination of a scan chain) If all of the scan cells on the scan chain SC_m $(0 \leq m \leq N-1)$ can be disabled during the i-th capture (shift) operation, SC_m is disabled while applying the i-th capture (shift) operation.

If a scan chain satisfies *Lemma* 3, it can be disabled from the scan operation, leading to a reduction in power consumption and test application time.

2.2 Reordering of Scan Cells

To maximize scan chain removal, the proposed method reorders scan cells based on the characteristic of test pattern. Figure 2 (a) shows the number of specified bits of s13207 for each scan cell. The horizontal and vertical axes show the scan cell number and the number of specified bits in each scan cell, respectively. By observing Fig. 2 (a), we found that some scan cells were specified more frequently than others, and that those scan cells obstructed scan chain disablement. For example, if a scan chain is composed of 100 scan cells and only a scan cell is specified during the shift or capture operation, the scan should be included in the scan operation. Therefore, we executed the scan cell reordering based on a specified number of scan cells, as shown in Fig. 2 (b). Consequently, frequently specified scan cells were partitioned into the same scan chain, elevating the number of scan chains that could be disabled during the scan operation.

To minimize the peak power consumption of the capture power, scan cells were reordered based on a specified numbers of test responses, since the power consumption of the shift operation can be efficiently reduced by scan chain partitioning.

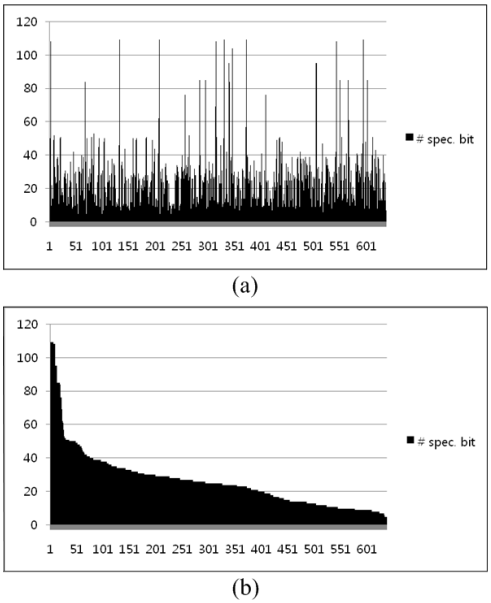

Fig. 2 The specified bit distribution of each scan cell.

2.3 Selective Scan Chain Activation Architecture

To reduce power consumption during a scan operation, a new scan chain activation architecture is presented in Fig. 3. The reordered scan chain is partitioned into N scan chains. All of the scan chains can share the scan input and output signals, because only a single scan chain is enabled during the scan shift operation. The mod N+2 counter controls the entire scan test procedure. The initial value of the counter (0) is assigned for the normal mode and for the scan capture operation. The next N states (1 to N) of the mod N+2 counter are assigned for the scan shift operation. The last state (N+1) of the mod N+2 counter is assigned in order to update the scan chains selector (SCS), which enables and disables the scan chains. The primary inputs of the mod N+2 counter are *reset*, which initializes the counter state as 0 and *inc*, which increments the counter state. The outputs of the decoding logic are the $update\_SCS$, *scan_en*, and the N-bit *chain_en* signals. Table 1 presents the control signals generated by the decoding logic. During shift mode, only *chain_en*[m] is enabled among the N *chain_en* signals to select a scan chain.

Using these control signals, scan chains are selected for the scan operation by the SCS which is composed of N SCS cells. Figure 4 shows the m-th SCS cell, which is connected to SC_m. The N flip-flops are concatenated in order to insert the information for enabling the scan chains. If the flip-flop of the m-th SCS holds a logic 0 (1), the scan cells in SC_m are not captured during the capture operation. The information is shifted during the update mode. During the update mode, all of the *se* signals are disabled, since $update\_SCS = 0$. Therefore, each scan chain is frozen while the scan chain selection data is shifted in. After completing

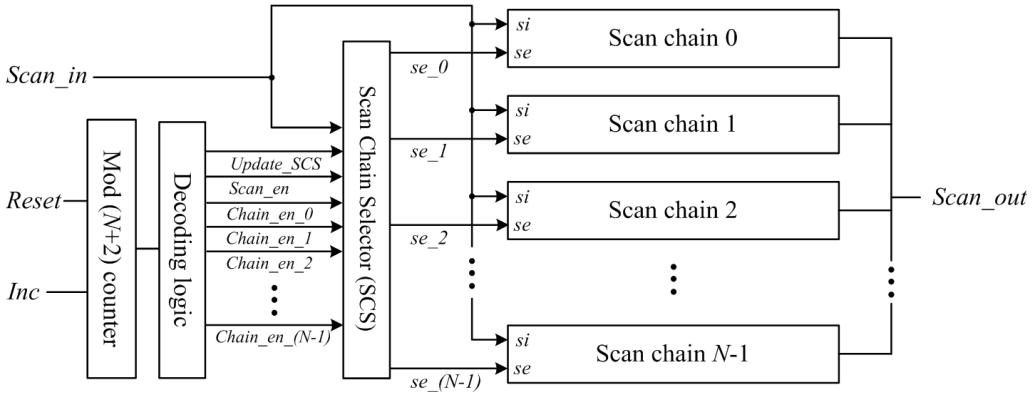

Fig. 3 The proposed scan architecture.

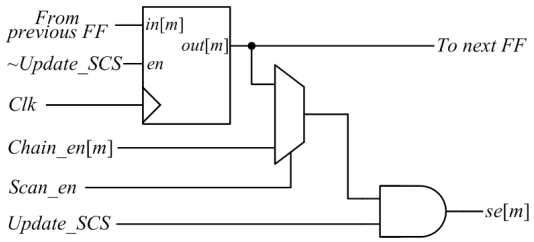

Fig. 4 The *m*-th SCS cell.

Table 1 Control signals generated by decoding logic.

Modes	Count.	*Scan_en*	*Update_SCS*	*Chain_en*[*m*]
Capture	0	0	1	0
Shift	*m*	1	1	1
Update	*N*-1	0	0	0

Table 2 SCS cell operation.

Modes	*Scan_en*	*Update_SCS*	*Chain_en*	*Out*	*Se*
Capture	0	1	X	D	D
Shift	1	1	D	X	D
Update	X	0	X	X	0

the update mode, the capture mode is executed based on the *out* signals while $update\_SCS = 1$ and $scan\_en = 0$. When $out[m] = 0$ (1), the SC_m is excluded (included) during the capture operation. In this way, many transitions within scan chain can be removed from the capture operation if the scan chain satisfies *Lemma* 3. In the shift mode, $update\_SCS = 1$ and $scan\_en = 1$, therefore, $chain\_en[m]$ is delivered directly to $se[m]$. Since only a single *chain_en* signal is enabled among the *N* signals, a scan chain is selected to be shifted in. If the selected scan chain satisfies *Lemma* 3, *inc* changes the counter state, and the shift operation of the scan chain is omitted. The SCS cell operation is presented in Table 2.

Consequently, both average and instantaneous power consumptions during the scan shift operation are reduced because only a single scan segment is enabled in a given test cycle. During the capture cycle, disabled scan segments do not consume any power. Therefore, overall power consumption during the scan shift and capture operations can be significantly reduced using the proposed scan architecture.

3. Experimental Results

To verify the effectiveness of the proposed method, we compared power consumption for various scan chain numbers. The large ISCAS'89 benchmark circuits were synthesized using the Synopsys Design compiler and the test patterns were generated using the Synopsys TetraMax. Table 3 shows the information about the benchmark circuits. Each column from the left presents the circuit name, the number of scan cells, the number of test patterns, and the specified bit ratio of the test vector. Table 4 shows the number of disabled scan segments. As shown in Table 4, the proposed scan cell reordering scheme increased the number of disabled scan chains during the scan operation, leading to a dramatic reduction in power consumption.

Table 5 presents the average power consumption comparisons. The unspecified bits were filled randomly. From the left, the circuit name, the number of transitions for the normal scan architecture, and the number of transitions for the proposed method are presented. Each number in the table shows the number of transitions, which is calculated using a weighted transition metric. As presented in Table 5, the average power can be easily reduced using the scan segmentation technique, since the remaining scan chains do not shift scan data while a scan chain is enabled. However, scan chain partitioning does not guarantee peak power reduction, since the scan segmentation has no influence on the power consumption of the capture operation. Therefore, another experimental result is introduced based on the peak power reduction.

Table 6 shows the comparisons of peak power consumptions for the two methods. Experiments were performed using three X-filling techniques: random-fill, zero-fill, and one-fill. The Zero- and one-fill techniques are widely used for low power testing and [6] presents the effectiveness of the zero- and one-filling techniques for reducing peak power consumption. As presented in Table 6, peak power consumption for the proposed method is reduced for every kind of X-filling technique. However, the zero- and

Table 6 Comparisons of peak power consumption.

Circuits	Fill	[6]		Proposed method					
				$SC = 4$		$SC = 8$		$SC = 16$	
		Trans.	red (%)	Trans.	red (%)	Trans.	red (%)	Trans.	red (%)
s13207	R-fill	638	-	343	46.2	33.	48.0	337	47.2
	0-fill	477	25.2	317	50.3	324	49.2	326	48.9
	1-fill	454	28.8	320	49.8	333	47.8	320	49.8
s15850	R-fill	534	-	306	42.7	295	44.8	287	46.3
	0-fill	417	21.9	267	50.0	263	50.4	262	50.9
	1-fill	337	36.8	320	40.1	291	45.5	310	41.9
s38584	R-fill	1426	-	762	46.6	769	46.1	754	47.1
	0-fill	1264	11.4	668	53.2	663	53.5	667	53.2
	1-fill	1053	26.2	673	52.8	681	52.2	706	50.5

Table 3 Information of ISCAS'89 benchmark circuits.

Circuits	No. of scan cells	No. of patterns	Specified ratio (%)	
			Input	Response
s13207	638	135	9.85	12.61
s15850	534	112	17.46	26.28
s38584	1,426	146	17.01	20.41

Table 4 Comparisons of disabled scan segments.

Circuits	No. of scan chains = 4			No. of scan chains = 8		
	Reorder		Ratio	Reorder		Ratio
	w/o	with		w/o	with	
s13207	53	189	3.57	138	515	3.73
s15850	61	125	2.05	149	317	2.13
s38584	8	43	5.38	20	128	6.40

Table 5 Comparisons of average power consumption.

Circuits	Normal	Proposed method					
		$SC = 4$		$SC = 8$		$SC = 16$	
	Tr.	Tr.	red	Tr.	red	Tr.	red
s13207	326	64	80.4	28	91.4	11	96.6
s15850	261	57	78.2	26	90.0	11	95.8
s38584	725	176	75.7	85	88.3	41	94.3

one-filling techniques do not fill the Xs to reduce the number of transitions for the capture operation. Therefore, peak power consumption for [6] is far higher than for the proposed method, as presented in Table 6. Consequently, the proposed method simultaneously reduces the average and peak power consumptions during the scan shift and capture operations.

4. Conclusions

In this paper, we proposed an selective scan chain activation technique which enables average and peak power reductions. Simple hardware architecture using a scan chain selector was also proposed, and the experimental results showed that the proposed method dramatically reduced the average and peak power consumptions, simultaneously. It is particularly noteworthy that a constant reduction of power consumption in peak power was accomplished, and this enabled effective low power testing without an unnecessary loss of yield.

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