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Optimization and Verification of Current-Mode Multiple-Valued Digit ORNS Arithmetic Circuits

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SUMMARY In this paper, optimization and verification of the current-mode multiple-valued digit ORNS arithmetic circuits are presented. The multiple-valued digit ORNS is the redundant number system using digit values in the multiple-valued logic and it realizes the full-parallel calculation without any ripple carry propagation. First, the 4-bit addition and multiplication algorithms employing the multiple-valued digit ORNS are optimized through logic-level analyses. In the multiplier, the maximum digit value and the number of modulo operations in series are successfully reduced from 49 to 29 and from 3 to 2, respectively, by the arrangement of addition lines. Next, circuit components such as a current mirror are verified using HSPICE. The proposed switched current mirror which has functions of a current mirror and an analog switch is effective to reduce the minimum operation voltage by about 0.13 volt. Besides an ordinary strong-inversion region, the circuit components operated under the weak-inversion region show good simulation results with the unit current of 10 nanoamperes, and it brings both of the lower power dissipation and the stable operation under the lower supply voltage.

key words: *multiple-valued logic, overlap resolution number system, current-mode circuit, weak-inversion region*

1. Introduction

According to the progress of semiconductor technologies and multimedia industries, the necessity of an advanced digital signal processor (DSP) is rising higher and higher. The fundamental arithmetic circuits such as an adder and a multiplier are particularly placed in the most important parts of the DSP. Almost all multipliers consist of adders, and the propagation delay of ripple carry signals is becoming an obstacle to a high-speed calculation with a long bit length. Accordingly, some parallel arithmetic circuits with the residue signal processing are studied actively.

Recently, a novel number system called "Overlap Resolution Number System (ORNS)" was proposed [1]–[3]. ORNS was a redundant number system on the basis of the signed Continuous-Valued Digit (CVD), and it could make the residue calculation without any ripple carry/borrow propagation. However, the circuitry employing ORNS had need of some high-precision digital-to-analog and analog-to-digital converters. Since the converters made a circuit scale larger and power dissipation higher, it was difficult to bring the advantages of ORNS into full play.

In order to solve the problem of ORNS, we have proposed "Multiple-Valued Digit ORNS (MVD-ORNS)" [4], [5]. Since a digit value of MVD is defined in a natural number, the current-mode MVD-ORNS arithmetic circuit can be composed of basic current-mode circuits such as a current mirror and an analog switch. On the other hand, a current-mode circuit is liable to increase power dissipation although low power dissipation is the important requirement for a long-life battery-driven application in addition to the calculation speed.

In this paper, the 4-bit addition and multiplication algorithms employing MVD-ORNS are optimized through the logic-level analysis, and the circuit components are reconsidered and verified using HSPICE simulator. In particular, the operation region of the weak-inversion is studied carefully in addition to the ordinary strong-inversion region, and a potential of the current-mode MVD-ORNS arithmetic circuit for coping with both low power dissipation and full-parallel high-speed calculation is discussed.

2. MVD-ORNS

2.1 Definition

MVD-ORNS is the redundant number system on the basis of the multiple-valued digit (MVD), and the digit value is defined as a logic level in the multiple-valued logic. Except for the complement representation, a k-bit binary number is generally expressed as Eq. (1).

$$(x)_2 = (x_{k-1}, \cdots, x_2, x_1, x_0)_2 = \sum_{m=0}^{k-1} x_m \cdot 2^m \tag{1}$$

where

$$m \in 0, 1, \cdots, k-1, \tag{2}$$

$$x_m \in 0, 1. \tag{3}$$

The MVD-ORNS number which corresponds to $(x)_2$ in Eq. (1) is defined as a follow.

$$(r(x))_{\mathrm{MVD}} = (r_{k-1}(x), \cdots, r_1(x), r_0(x), r_{-1}(x), \cdots, r_{-k+1}(x))_{\mathrm{MVD}}. \tag{4}$$

And, the digit values in Eq. (4) are given by Eq. (5).

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$$r_n(x) = \begin{cases} \left(\sum_{m=n}^{k-1} x_m \cdot 2^{m-n} \right) \bmod \mathrm{X} \\ \left(\sum_{m=-n}^{k-1} x_{k-m-n} \cdot 2^{k-m-n-1} \right) \bmod \mathrm{X} \end{cases} \text{when} \begin{cases} n \geq 0 \\ n < 0 \end{cases} \tag{5}$$

where n is the digit number as a follow.

$$n \in -k+1, \cdots, 0, \cdots, k-1. \tag{6}$$

In Eq. (5), X is the range of $(x)_2$ and is equal to 2^k. And, "mod X" is the modulo operation which subtracts X from the digit value when it is equal to X or higher. In the direct conversion, Eq. (5) can be simply rewritten as Eq. (7) because $r_n(x)$ is kept within X.

$$r_n(x) = \begin{cases} \sum_{m=n}^{k-1} x_m \cdot 2^{m-n} \\ \sum_{m=-n}^{k-1} x_{k-m-1} \cdot 2^{k-m-n-1} \end{cases} \text{when} \begin{cases} n \geq 0 \\ n < 0. \end{cases} \tag{7}$$

On the other hand, the inverse conversion is carried out as shown in Eqs. (8) and (9).

$$a_0 = \begin{cases} 1 & \text{when} \quad 2r_{-k+1} \geq 2^{k-1} \\ 0 & \text{when} \quad 2r_{-k+1} < 2^{k-1}, \end{cases} \tag{8}$$

$$a_h = \begin{cases} 1 & \text{when} \quad 2r_{h-k+1} - r_{h-k} \geq 2^{k-1} \\ 0 & \text{when} \quad 2r_{h-k+1} - r_{h-k} < 2^{k-1} \end{cases} \tag{9}$$

where h is the bit number as a follow.

$$h \in 1, 2, \cdots, 2k-2. \tag{10}$$

In both of the conversion and the inverse conversion, there is no process which spreads over three digits.

2.2 Addition Algorithm

The MVD-ORNS numbers can be added to each other in fully parallel as a follow.

$$r_n(x+y) = \{r_n(x) + r_n(y)\} \bmod \mathrm{X} \tag{11}$$

where $r_n(x)$ and $r_n(y)$ are the digit values of the n-th digit in the MVD-ORNS numbers which are converted from binary numbers, $(x)_2$ and $(y)_2$, respectively. From Eq. (5), Eq. (11) can be rewritten as Eq. (12).

$$r_n(x+y) = \begin{cases} \left[\sum_{m=n}^{k-1} (x_m + y_m) \cdot 2^{m-n} \right] \bmod \mathrm{X} \\ \left[\sum_{m=-n}^{k-1} (x_{k-m-1} + y_{k-m-1}) \cdot 2^{k-m-n-1} \right] \bmod \mathrm{X} \end{cases}$$
$$\text{when} \begin{cases} n \geq 0 \\ n < 0. \end{cases} \tag{12}$$

If $(y)_2$ is replaced with its 2's complement number before the binary-to-MVD conversion, the subtraction algorithm is carried out. A higher bit is used for representing a positive or a negative sign after the inverse conversion.

2.3 Multiplication Algorithm

The multiplication algorithm employing MVD-ORNS is defined as follows.

$$r_k(x \cdot y) = \left\{ \sum_{m=1}^{k-1} y_m \cdot r_{m-k+1}(x) \right\} \bmod \mathrm{X}, \tag{13}$$

$$r_h(x \cdot y) = \begin{cases} \left[\sum_{m=h}^{k-1} y_m \cdot r_{h-m}(x) \right] \bmod \mathrm{X} \\ \left[\sum_{m=-h}^{k-1} y_{k-m-1} \cdot r_{-k+m+h+1}(x) \right] \bmod \mathrm{X} \end{cases}$$
$$\text{when} \begin{cases} h \geq 0 \\ h < 0, \end{cases} \tag{14}$$

where k and h are the digit numbers of the most significant digit and other digits, respectively, and the digit length of the product runs up to $2k$ as a follow.

$$h \in 1, 2, \cdots, 2k-1. \tag{15}$$

In the algorithm, $(x)_2$ is the multiplicand and is converted into $(r(x))_{\mathrm{MVD}}$. On the other hand, $(y)_2$ is the multiplier and is just used in a binary number. No ripple carry occurs since the product on each digit is individually given by the weighted sum of $(r(x))_{\mathrm{MVD}}$ according to $(y)_2$.

3. Logic-Level Optimization and Verification

3.1 Addition Algorithm

Since all of decimal fractions are rounded off in the definition of the MVD-ORNS number, some logical errors come out in the arithmetical operation. And, some digits are not necessarily used.

In this section, the 4-bit addition algorithm employing MVD-ORNS is optimized and verified including the conversion and the inverse conversion. Lower five digits have relations to the addition operation because a bit length of the sum is equal to 5 at the maximum, and the maximum digit values of these five digits reach 14, 30, 24, 28 and 16 in order from a higher digit to the least significant digit after the digit-by-digit addition. Therefore, the 4-bit addition algorithm can be simply drawn as Fig. 1. BMC, mod, MBC in Fig. 1 are the binary-to-MVD converter, the modulo operation for 2^4, the inverse conversion, respectively. And, a solid circle and a hollow circle mean that the digit values are added to each other and the digit value is copied for two lines, respectively.

In the logic-level analysis, some errors such as -0.5 and -1 are observed in MBC, and it is sufficiently smaller than 4 which is a threshold of MBC. It has no incorrect binary result and no carry propagation beyond adjoining two digits.

When the 2's complement number of the input is added to one of BMCs, the algorithm as shown in Fig. 1 makes

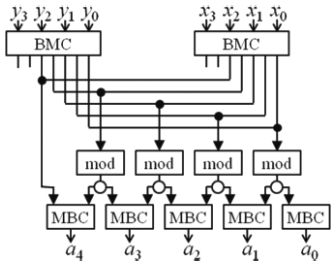

Fig. 1 Optimized addition algorithm employing MVD-ORNS.

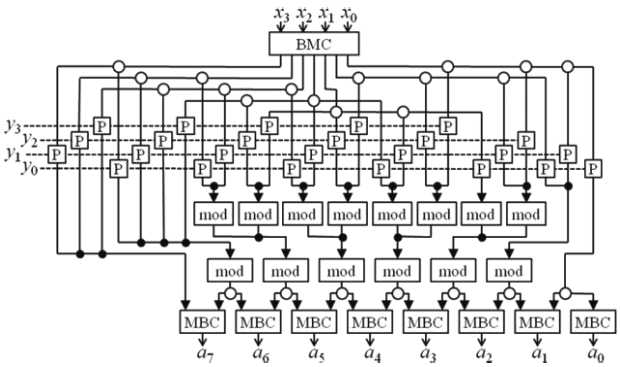

Fig. 2 Optimized multiplication algorithm employing MVD-ORNS.

the correct result for the 4-bit subtraction algorithm. The fifth bit of the result shows a positive or a negative sign in representation of the 2's complement.

3.2 Multiplication Algorithm

The 4-bit multiplication algorithm employing MVD-ORNS is optimized and verified through the logic-level analysis. If it makes the sum of digit values at a time, the maximum digit value reaches 49 and it needs triple modulo operations in series. By dividing the modulo operations into two parallel lines as shown in Fig. 2, the maximum digit value and the number of the modulo operations in series can be reduced from 49 to 29 and from 3 to 2, respectively. It is very effective in low power dissipation and high-speed calculation. In Fig. 2, P is the analog switch controlled by a binary input signal.

In the logic-level analysis, higher digits have some errors such as -0.5 and -1 in MBC. It is sufficiently smaller than a threshold of MBC and it does not have a bad effect on the calculation result.

4. Circuit Component

4.1 Current-Mode Circuit

In the current-mode MVD-ORNS arithmetic circuit, the digit values are replaced with multiples of the unit current, a digit-by-digit addition can be carried out by only connecting wires. A subtraction is the same as the addition of two signals in the opposite direction. The weighted summation

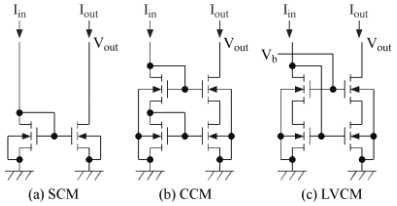

Fig. 3 Three types of current mirror.

Table 1 The output impedance and the minimum operation voltage of current mirrors operated under the strong-inversion region.

	Z_{out}	V_{min}
SCM	r_d	$2\sqrt{\frac{I_{in}}{K}} + V_T$
CCM	$2r_d + g_m r_d^2$	$2\sqrt{\frac{I_{in}}{K}} + V_T$
LVCM	$2r_d + g_m r_d^2$	$\sqrt{\frac{I_{in}}{K}}$

for a binary-to-MVD conversion is realized by a current mirror, and a comparison for the inverse conversion is drawn by a current comparator which is composed of two current mirrors. Accordingly, the current mirror is the most important circuit component for the current-mode MVD-ORNS algorithms circuit.

4.2 Current Mirror

Figure 3 shows three types of current mirror with n-channel MOSFETs. Types (a), (b) and (c) are called the single current mirror (SCM), the cascade current mirror (CCM) and the low-voltage current mirror (LVCM), respectively. CCM is composed of two SCMs in a cascade connection. LVCM is the improved circuit of CCM for the lower-voltage operation, and V_b is used for the bias control. When MOSFETs in the current mirror are operated under the ordinary strong-inversion region, the output impedance (Z_{out}) and the minimum operation voltage (V_{min}) on the output terminals are given as Table 1. All MOSFETs have the same gate sizes, and the substrate effect and the short channel effect are assumed to be sufficiently small. In Table 1, r_d and V_T are the drain resistance and the intrinsic threshold voltage of the MOSFET, respectively. g_m and K are referred as the mutual conductance parameter and the transconductance parameter, respectively. LVCM has both higher Z_{out} and lower V_{min} than others.

The characteristic of current mirrors is verified using HSPICE with CMOS 0.35 micrometer device parameters. The output current (I_{out}) characteristic seen from the variation in the output terminal voltage (V_{out}) is shown in Fig. 4. V_{min} and Z_{out} are listed in Table 2, and it is consistent with the theoretical analysis. The time response of I_{out} seen from the input current (I_{in}) variation is also listed in Table 2. t_{pos} and t_{neg} are defined as the delay times of I_{out} seen from I_{in} at a half of the maximum I_{in} when I_{in} is given as a step-up

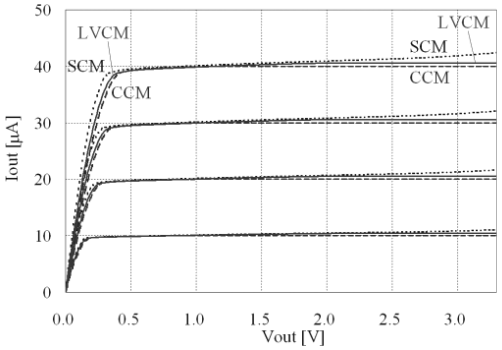

Fig. 4 V_{out}-I_{out} characteristic of current mirrors operated under the strong-inversion region.

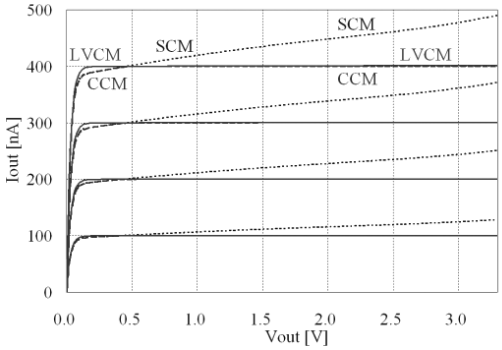

Fig. 5 V_{out}-I_{out} characteristic of current mirrors operated under the weak-inversion region.

Table 2 Simulation result of current mirrors operated under the strong-inversion region.

	I_{in} [μA]	V_{min} [V]	Z_{out} [MΩ]	t_{pos} [ns]	t_{neg} [ns]
SCM	10	0.47	2.8	2.5	1.5
	20	0.49	1.7	1.7	1.0
	30	0.51	1.3	1.4	0.8
	40	0.54	1.1	1.3	0.7
CCM	10	0.60	167	5.3	2.2
	20	0.66	20	3.4	1.5
	30	0.70	66	2.6	1.2
	40	0.74	22	2.1	1.0
LVCM	10	0.51	164	5.3	2.2
	20	0.55	26.0	3.4	1.5
	30	0.59	11.1	2.6	1.2
	40	0.64	5.0	2.1	0.9

Table 3 Simulation result of current mirrors operated under the weak-inversion region.

	I_{in} [nA]	V_{min} [V]	Z_{out} [GΩ]	t_{pos} [ns]	t_{neg} [ns]
SCM	100	0.32	0.10	87	20
	200	0.34	0.06	43	11
	300	0.35	0.04	31	8.8
	400	0.36	0.03	27	7.3
CCM	100	0.32	21.5	198	48
	200	0.34	14.0	113	27
	300	0.35	7.0	81	19
	400	0.36	5.6	64	16
LVCM	100	0.13	280	195	36
	200	0.13	72	107	17
	300	0.13	4.0	69	12
	400	0.13	2.2	53	9.1

function and a step-down function, respectively. A delay time becomes shorter with an increase of I_{in} although it is strongly related to the power dissipation.

Next, the current mirror which MOSFETs are operated under the weak-inversion region is taken up. If a drain-to-source current of the MOSFET is smaller than about one microampere, it is generally operated under the weak-inversion region, and the drain-to-source current is known as a follow.

$$I_{ds} = I_{ds0} \exp \frac{V_{gs}}{nV_{\theta}} \tag{16}$$

where, V_{gs} is the gate voltage seen from the source voltage, and n is the intrinsic parameter called the slope factor. I_{ds0} is the current of when V_{gs} is equal to zero. And, V_{θ} is the thermal voltage and is equal to 26 millivolts in a normal temperature. V_{min} of CCM and LVCM become about 8 V_{θ} and it is approximately equal to 208 millivolts. It means that the operation under the weak-inversion region is also effective in reduction of the power supply voltage.

Figure 5 and Table 3 show HSPICE simulation results of current mirrors operated under the weak-inversion region. LVCM copes with both the lowest V_{min} and the highest Z_{out}. The difference between I_{out} and I_{in} is kept within one nanoampere when V_{out} is equal to 0.18 volt or higher.

Accordingly, it is said that LVCM is the most suitable current mirror for the current-mode MVD-ORNS arithmetic circuit operated under both the strong-inversion region and the weak-inversion region. If the MOSFET has several microamperes, the operation spreads over the two regions. However, it brings no trouble to make a copy of I_{in} in a current mirror.

4.3 Switched Current Mirror

In the current-mode MVD-ORNS arithmetic circuit, an analog switch is sometimes placed between current mirrors. In order to prevent the power supply voltage from pushing up by the analog switch, the switched current mirrors with CCM and LVCM are proposed as shown in Figs. 6 (a) and (b), respectively, and are called SW-CCM and SW-LVCM, respectively. It has the CMOS inverter that the source terminal of a p-channel MOSFET is connected with the input terminal or the bias control voltage of the current mirror (V_b). When the control voltage of the switch (V_c) is higher than a threshold voltage of the CMOS inverter, the n-channel MOSFET connected with the output terminal of the current mirror is cut off. If V_c goes down to zero, the output voltage of the CMOS inverter becomes equal to the input terminal voltage and V_b in SW-CCM and SW-LVCM, respectively, and it has the same operation as CCM and

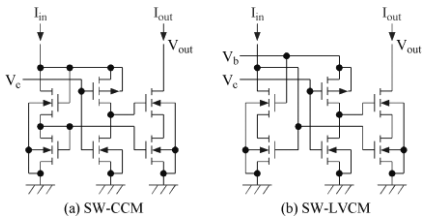

Fig. 6 Proposed switched current mirrors.

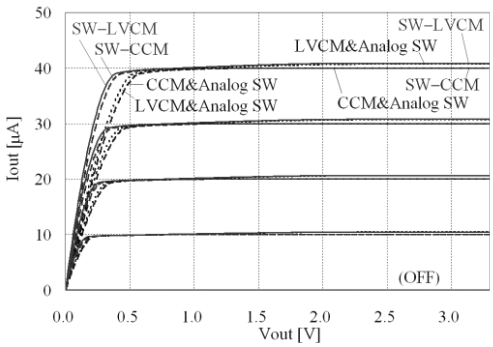

Fig. 7 V_{out}-I_{out} characteristic of the switched current mirrors operated under the strong-inversion region.

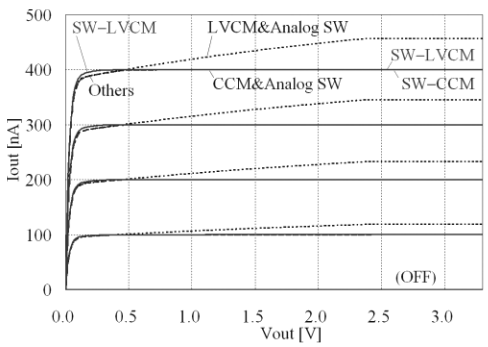

Fig. 8 V_{out}-I_{out} characteristic of the switched current mirrors operated under the weak-inversion region.

LVCM, respectively.

The characteristic of the proposed switched current mirrors is verified using HSPICE and is compared with that of an ordinary combination of a current mirror and an analog switch. The V_{out}-I_{out} characteristic of the proposed switched current mirrors operated under the strong-inversion region and the weak-inversion region are shown in Figs. 7 and 8, respectively. When V_c is equal to zero, SW-CCM and SW-LVCM realize almost the same characteristics as that of CCM and LVCM, respectively. The proposed circuits have lower V_{min} than the ordinary combinations of a current mirror and an analog switch in both operation regions. And, I_{out} is cut off when V_c is turned to the supply voltage.

4.4 Binary-to-MVD Converter

A converter from a 4-bit binary number to the 7-digit MVD-ORNS number can be composed of SW-LVCMs as

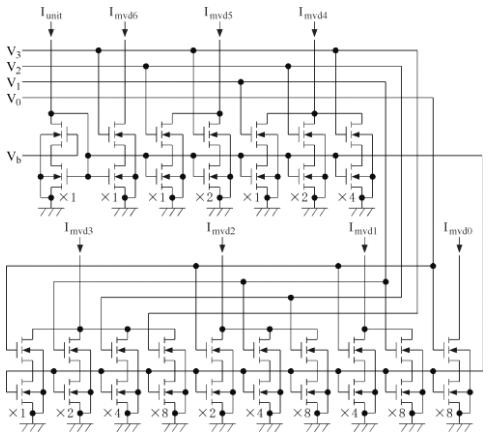

Fig. 9 4-bit binary to 7-digit MVD converter with SW-LVCMs.

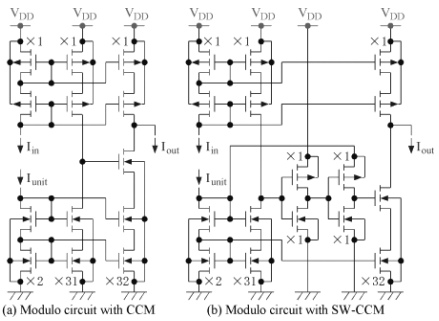

Fig. 10 Modulo circuits for the modulo operation ($X = 16$).

shown in Fig. 9. I_{unit} is the unit current, and the output currents (I_{mvd0}–I_{mvd6}) are given by the weighted sum of I_{unit} according to the input voltages (V_0–V_3). A CMOS inverter in the SW-LVCM cannot be omitted when the input voltage is inconsistent with the bias voltage for the current mirror. Power dissipation of the converter is estimated as the power supply voltage multiplied by the sum of the unit current and all output currents.

4.5 Modulo Circuit

The modulo operation makes a comparison between the input and the cardinal number (X), and it subtracts X from the input when the input is equal to X or higher. In order to distinguish the digit value clearly, it is better to set the threshold for comparison in 0.5 lower than X. Figure 10 (a) shows the modulo circuit with CCMs and an analog switch. In the other way, the analog switch in Fig. 10 (a) can be replaced with SW-CCM and an additional CMOS inverter as shown in Fig. 10 (b). Of course, it is possible to use LVCM and SW-LVCM instead of CCM and SW-CCM, respectively.

Figures 11 and 12 show HSPICE simulation results of the modulo circuit operated under the strong-inversion region and the weak-inversion region, respectively, and the unit currents are equal to 1 microampere and 10 nanoamperes, respectively. The output current (I_{out}) is following

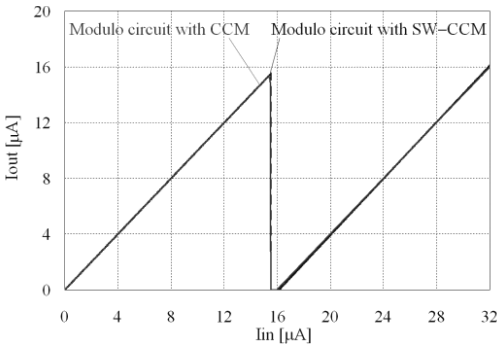

Fig. 11 I_{in}-I_{out} characteristic of Modulo circuits operared under the strong-inversion region.

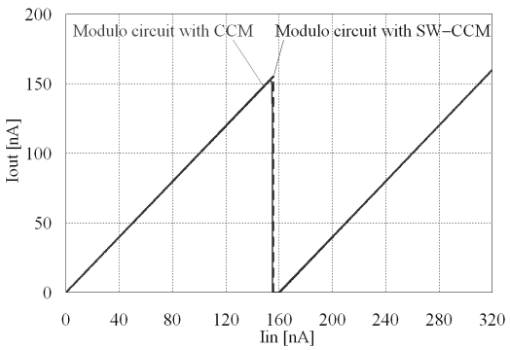

Fig. 12 I_{in}-I_{out} characteristic of Modulo circuits operared under the weak-inversion region.

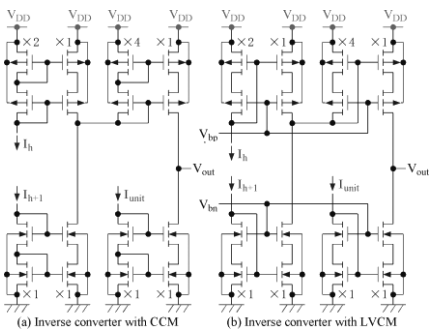

Fig. 13 Inverse converters.

the input current (I_{in}) or the current subtracted from I_{in}. The maximum power dissipation of the modulo circuit with CCM runs up to 262 microwatts and 1.43 microwatts in the strong-inversion region and in the weak-inversion region, respectively.

4.6 Inverse Converter

The inverse converters are composed of CCMs and LVCMs as shown in Figs. 13 (a) and (b), respectively. And, HSPICE simulation results of the inverse converter with CCMs operated under the strong-inversion region and the weak-inversion region are shown in Figs. 14 and 15, respectively. The output voltage is made by the balance of current signals

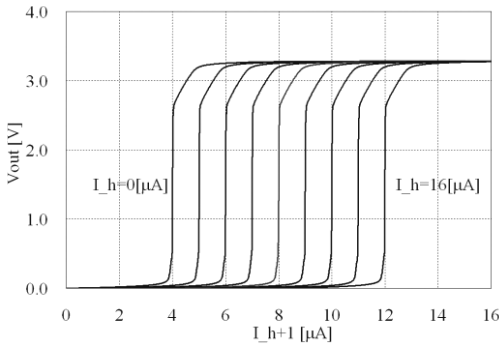

Fig. 14 Output voltage of the inverse converter operated under the strong-inversion region.

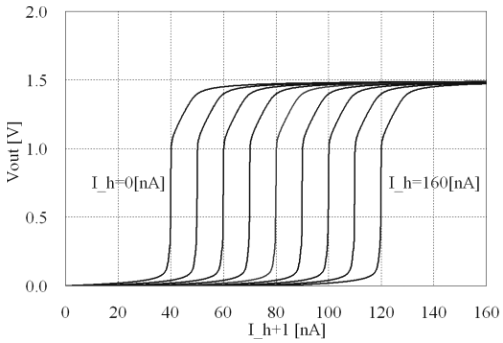

Fig. 15 Output voltage of the inverse converter operated under the weak-inversion region.

on the adjoining lower digit (I_h) and higher digit (I_{h+1}).

5. Conclusion and Discussion

In this paper, the 4-bit addition and multiplication algorithms employing MVD-ORNS (Multiple-Valued Digit ORNS) have been optimized thought the logic-level analyses, and the current-mode circuit components have been reconsidered and verified using HSPICE with CMOS 0.35 micrometer device parameters.

In the optimization of algorithms, the maximum digit value and the number of modulo operations in series have been successfully reduced from 49 to 29 and from 3 to 2, respectively, by the arrangement of addition lines in the 4-bit multiplier. And, the correct calculation results have been brought without any ripple carry propagation.

In the reconsideration of the circuit components, three types of current mirrors have been compared with each other, and the switched current mirrors have been proposed. The characteristic of the current mirrors, the proposed switched current mirrors, the modulo circuit, the binary-to-MVD converter and the inverse converter has been verified using HSPICE. In particular, the proposed SW-LVCM has coped with both the lower minimum operation voltage and the smaller difference between the input current and the output current. And, the operation of the weak-inversion region has been very effective to reduce the minimum operation voltage and power dissipation although the time response

hasn't reached that of the strong-inversion region. In addition, it is necessary to pay attention to the device parameter mismatch in case of the weak-inversion region. Since there are both the important parts and unimportant parts in the current-mode MVD-ORNS arithmetic circuit, it is better to give priority to the important parts in the transistor-level layout of VLSI chips.

If the signal delay on wires is assumed to be zero, the delay time in the binary-to-MVD converter, the inverse converter and the digit-by-digit addition is seldom related to a bit length of the input. Therefore, the calculation speed of the current-mode MVD-ORNS arithmetic circuit is mainly limited by the number of the modulo circuits in series. On the other hand, the ripple carry propagation time and the maximum power dissipation of an ordinary 1-bit full adder are equal to 10.3 nanoseconds and 2.3 microwatts, respectively, in the same device parameters. Accordingly, there is some possibility that the current-mode MVD-ORNS adder makes the addition earlier than an ordinary full adder with the 11-bit input or higher in the strong-inversion region. An ordinary 4-bit full adder is composed of 168 MOSFETs, and it is about one-fourth of the current-mode MVD-ORNS adder. Unfortunately, it is kept at almost the same ratio even if a bit length of the input gets longer.

It is said that the current-mode MVD-ORNS arithmetic circuit has some potentials to realize the high-speed full-parallel calculation, the operation under the low supply voltage and lower power dissipation for long-life battery-driven applications according to the operation region of current mirrors. Since there are various combinations of the circuit components, the optimization of algorithms and the verification of circuit components using HSPICE in this paper will be helpful to bring the advantage of MVD-ORNS into full play.

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