LETTER

Single-Event-Upset Tolerant RS Flip-Flop with Small Area

Kazuteru NAMBA[†a)], ***Member***, **Kengo NAKASHIMA**[†*], ***Nonmember***, ***and*** **Hideo ITO**[†], ***Fellow***

SUMMARY This paper presents a construction of a single-event-upset (SEU) tolerant reset-set (RS) flip-flop (FF). The proposed RS-FF consists of four identical parts which form an interlocking feedback loop just like DICE. The area and average power consumption of the proposed RS-FFs are 1.10 ∼ 1.48 and 1.20 ∼ 1.63 times smaller than those of the conventional SEU tolerant RS-FFs, respectively.

key words: *soft error, single-event-upset (SEU) tolerance, reset-set flip-flop (RS-FF), interlocking feedback loop*

1. Introduction

In recent high-density and low-power VLSIs, soft errors frequently occur for several reasons, such as neutrons from cosmic rays, and they become a substantial problem. In logic circuits, single-event-upsets (SEUs), which are a class of soft errors, have become a particularly serious problem [1], [2]. Particle strikes in logic circuits induce transient current pulses, which cause voltage pulses referred to as single-event-transients (SETs). On storage elements such as flip-flops (FFs), SETs may upset the elements' stored-values. These upsets are the SEUs. To prevent SEUs from occurring, various SEU tolerant storage elements have been proposed [3]. For example, the dual interlocked storage cell (DICE) [4] is one of the most popular SEU tolerant latches, and it consists of four identical parts forming an interlocking feedback loop.

A reset-set (RS) flip-flop (FF) is one of basic storage elements. Some SEU tolerant RS-FFs have been proposed [5], [6]. These SEU tolerant RS-FFs have four identical parts making a loop just like DICE. However, they require large area overhead.

This paper presents a construction of an SEU tolerant RS-FF. The proposed RS-FF has four identical parts like the conventional FFs, and its area is smaller than the conventional ones.

2. Proposed Soft Error Tolerant RS Flip-Flop

Figure 1 shows the construction of the proposed SEU tolerant RS-FF. The FF has two inputs R and S, two output lines Q and QB, and two local lines Q2 and Q2B. If no SET occurs, the values of Q, Q2 and the inverted values of QB, Q2B are the same as each other. When (R,S) = (1,0) and (0,1), the output value at Q is reset to 0 and set to 1, respectively. If (R,S) = (0,0), the FF keeps its previous value. The input (1,1) is forbidden. Just like DICE [4] and the conventional SEU tolerant RS-FFs [5], [6], the proposed FF can be divided into four parts with identical structure, e.g. the part consisting of P1, P2, N1 and N2, and the four form an interlocking feedback loop.

The proposed RS-FF is capable of tolerating an SEU caused by an SET occurring on Q, QB, Q2 or Q2B. Next, the SEU tolerant capability is demonstrated. When (R,S) = (1,0) or (0,1), no upsets occur because even if SETs occur, the stored-values are immediately reset or set. Table 1 summarizes the changes of the values of the output and local lines, and the states of the transistors in the case where an SET occurs on Q for (R,S) = (0,0). The first rows of Table 1 (i) and (ii) show the correct values and states before the SET occurrences. The second rows show the values and states immediately after the occurrences, and the subsequent rows show the changed ones in order of time. The dotted vertical lines in columns express the same values and states as in the last row.

Table 1 (i) shows the changes in the case where an SET occurs on Q with the value of 0. The value of Q incorrectly changes into 1 as shown in the second row. The SET turns on N2 and turns off P6 as shown in the third row. The node Q2B is cut off from V_{DD} owing to turning off of P6. It comes to be in a high impedance state and keeps storing the previous values using the parasitic capacitance. Since P1, P2 and N2 are in on-states, the value of QB comes to be an intermediate one and neither 1 nor 0 as shown in the fourth row. This weakly turns on P4 and weakly turns off N8 as shown in the fifth row. The node Q is connected to the ground through N4 while it is weakly connected to V_{DD} through P3, P4, and then the value of Q returns to 0 soon as shown in the sixth row. This return turns all changed values and states back to the correct ones as shown in the seventh row and after. In summary, even if an SET $0 \rightarrow 1$ occurs on Q, all erroneous values and states in the FF return to be correct after a short time, and no SEUs occur. Similarly, an SET $1 \rightarrow 0$ on Q does not bring about SEUs as shown in Table 1 (ii). Since the proposed FF has repeated structure, even if SETs occur on the other nodes, QB, Q2, and Q2B, they are tolerated in the same way.

It is noted that SETs occurring in the FF cause transient pulses on the output Q as shown in the second-fifth rows

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[†]The authors are with the Graduate School of Advanced Integration Science, Chiba University, Chiba-shi, 263–8522 Japan.
[*]Presently, with NTT Data Corporation.
a) E-mail: namba@ieee.org
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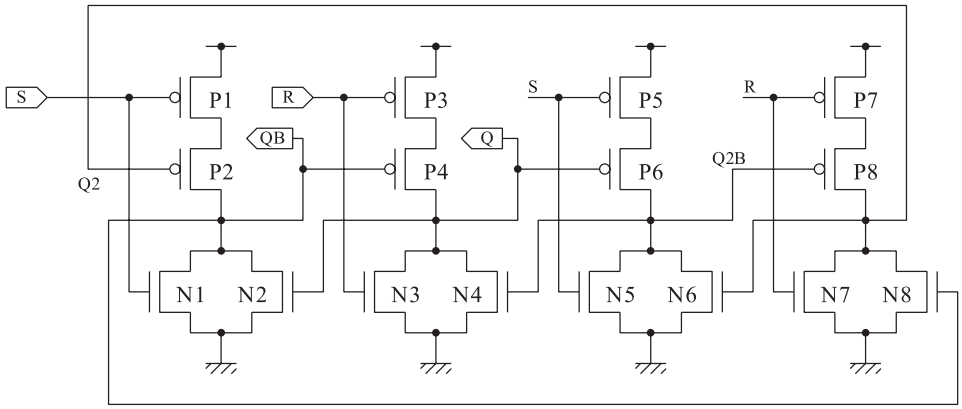

Fig. 1 Construction of proposed SEU tolerant RS-FF.

Table 1 Changes of values of lines and states of transistors on proposed RS-FF with an SET occurring on Q for (R,S) = (0,0).

(i) SET on Q with 0

P1	P2	N1	N2	QB	P3	P4	N3	N4	Q	P5	P6	N5	N6	Q2B	P7	P8	N7	N8	Q2	
on	on	off	off	1	on	off	off	on	0	on	on	off	off	1	on	off	off	on	0	correct state
		on		x		x			1		off							x		SET occurrence on Q
		off		1		off			0		on							on		return of value on Q correct state

(ii) SET on Q with 1

P1	P2	N1	N2	QB	P3	P4	N3	N4	Q	P5	P6	N5	N6	Q2B	P7	P8	N7	N8	Q2	
on	off	off	on	0	on	on	off	off	1	on	off	off	on	0	on	on	off	off	1	correct state
		off						x	0		on			x		x				SET occurrence on Q
		on						off	1		off			0		on				return of value on Q correct state

in Table 1 (i), (ii). In addition, the proposed FF does not tolerate SETs occurring on or propagated to the inputs R and S just like the conventional SEU tolerant RS-FFs. They should be tolerated by use of an SET tolerant method such as [7], [8] besides the proposed design.

3. Evaluation

Figure 2 and Table 2 show comparison results between the proposed RS-FF and three conventional RS-FFs, namely a normal RS-FF, and two conventional SEU tolerant RS-FFs proposed in [5], [6]. The evaluated FFs are designed on a 45 nm predictive technology model [9]–[12] and simulated by HSPICE. The V_{DD} supply voltage is set to 1.0 V. In the simulation, soft errors are generated using the soft error occurrence model shown in [13], [14], namely, the double exponential model.

Figure 2 shows relations between charge of striking particles and recovery time, i.e. time after an SET inverts the output value of an RS-FF before the erroneous value is corrected. If a particle strike does not flip the output value even for a moment, the recovery time is regarded as 0. If an SEU occurs, i.e. an inverted output value is not corrected even after a long time, the recovery time is regarded as infinity. If the recovery time for a FF is short, we can regard that the FF has high SEU tolerant capability. For any particle charges including those of around 0.15 pC, which neutron strikes generate [15], recovery time for the proposed RS-FF is almost equal to or shorter than those for the other three conventional RS-FFs. Thus, we can conclude that the proposed RS-FF has high SEU tolerant capability.

The "area ratio" column in Table 2 shows the area ratio of the evaluated RS-FFs to the normal RS-FFs. The area of the proposed RS-FF is 1.10 $\sim$ 1.48 times smaller than that of the conventional SEU tolerant RS-FFs. The "power" column shows the average power consumption. In the simulation, the input values change every 0.5 ns and a sequence (R,S) = (1,0), (0,0), (0,1), (0,0) is repeatedly supplied. The

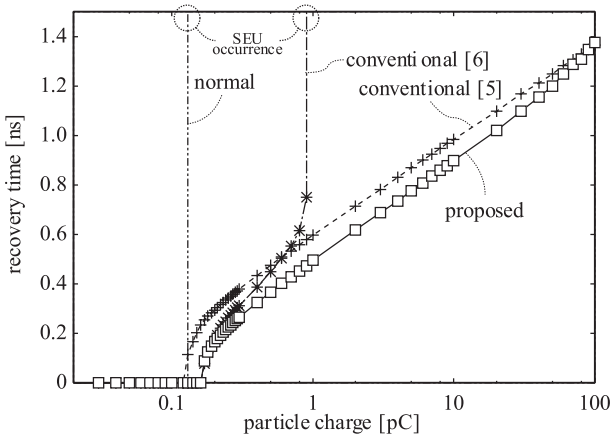

Fig. 2 Particle charge vs recovery time.

Table 2 Comparison results.

	area ratio	power (μW)	delay (ns)
normal RS-FF	1.00	16.2	0.037
conventional RS-FF [5]	2.88	43.9	0.027
conventional RS-FF [6]	2.13	32.2	0.025
proposed RS-FF	1.94	26.9	0.037

consumption of the proposed RS-FF is 1.20 ∼ 1.63 times lower than that of the conventional ones. The "delay" column shows the delay time from an input R or S to an output Q or QB. The proposed RS-FF has the longest delay time. However, the difference is small. In fact, the difference between those of the proposed RS-FF and the conventional RS-FF with the shortest delay time [6] is about twice as small as the gate delay time of an inverter.

4. Conclusion

This paper presented a construction of an SEU tolerant RS-FF. Just like DICE, the proposed FF has a repeated structure in which four identical parts form an interlocking feedback loop. Simulation results show that the proposed RS-FF has high SEU tolerant capability. The area and average power consumption of the proposed RS-FFs are 1.10 ∼ 1.48 and 1.20 ∼ 1.63 times smaller than those of the conventional SEU tolerant RS-FFs, respectively.

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