PAPER

Construction of BILBO FF with Soft-Error-Tolerant Capability*

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SUMMARY In this paper, a soft-error-tolerant BILBO (Built-In Logic Block Observer) FF (flip-flop) is presented. The proposed FF works as a soft-error-tolerant FF in system operations and as a BILBO FF in manufacturing testing. The construction of the proposed FF is based on that of an existing soft-error-tolerant FF, namely a BISER (Built-In Soft Error Resilience) FF. The proposed FF contains a reconfigurable C-element with XNOR calculation capability, which works as a C-element for soft-error-tolerance during system operations and as an XNOR gate employed in linear feedback shift registers (LFSRs) during manufacturing testing. The evaluation results shown in this paper indicate that the area of the proposed FF is 8.5% smaller than that of a simple combination of the existing BISER and BILBO FFs. In addition, the sum of CLK-Q delay and D-CLK setup times on system operations for the proposed FF is 19.7% shorter than that for the combination.

key words: *soft-error-tolerance, DFT (design for test), BISER (built-in soft-error resilience), BILBO (built-in logic block observer), reconfigurable C-element*

1. Introduction

In modern high-density and low-power VLSIs, striking of charged particles such as alpha and cosmic ones frequently induces soft-errors for several reasons [1], [2]. One-time, only soft-errors on memory systems seriously affected operations of VLSI systems. However, in modern VLSI systems, soft-errors occurring on logic circuits have also come to be a substantial problem [1], [2]. To resolve this issue, various soft-error-tolerant flip-flops (FFs) were proposed [3]. The built-in soft-error resilience (BISER) FF is a class of soft-error-tolerant FFs and contains C-elements [4]. The BISER FF is capable of correcting soft-errors occurring on the FF as well as those on combinational parts in logic circuits.

To facilitate manufacturing testing, designs for test (DFTs) are widely used. Some researchers have proposed DFTs with soft error tolerant capability [2], [5]–[9]. Although the area overheads of those designs are high for DFT, they are low enough to be used as soft error tolerant designs. These works target scan design, a class of DFTs that use scan FFs. These designs utilize reconfigurable scan FFs which act as soft-error-tolerant FFs during system operations while acting as scan FFs in manufacturing testing. In testing, these FFs cannot tolerate soft-errors. Despite this, we can use them to perform reliable testing. This is because, in general, test application times are much shorter than system operating times, and thus the probability of a particle strike during manufacturing testing is much lower than that during system operations. In [2], [5]–[7], full-hold scan FFs with soft-error-tolerant capability were proposed. The full-hold scan FFs are a class of scan FFs, and they make controllability and observability much better [10]. The FFs proposed in [2], [5] detect and correct soft-errors occurring on the FFs. Using the FF proposed in [6], soft-errors occurring on combinational parts are mitigated. The FF proposed in [7] tolerates soft-errors on combinational parts as well as those on the FF. In [8], [9], soft-error-tolerant enhanced scan FFs were proposed. The enhanced scan FFs facilitate delay fault testing using extra latches [11]. The FFs proposed in [8] detect and/or correct soft-errors on the FFs by comparing values stored in original and extra latches. The FFs proposed in [9] is a class of master-slave FFs and every slave latch with soft-error-tolerant capability transforms into two latches used as slave and extra latches on manufacturing testing.

Besides scan designs, there is another well-known class of DFT, namely built-in self-test (BIST) technique [12], which uses built-in test pattern generators (TPGs) and/or output response analyzers (ORAs). The BIST has several advantages, e.g. at-speed testing and reduced need for automatic test equipment (ATE), though it requires large area overhead. We can expect to obtain a BIST architecture with low area overhead by combining with soft-error-tolerant design just like the above scan designs. However, no existing works provided such BIST architecture.

This paper presents a construction of a built-in logic block observer (BILBO) architecture with soft-error-tolerant capability. The BILBO is a class of BIST, and uses BILBO FFs [13]. The BILBO FFs can form linear feedback shift registers (LFSRs), which are used as built-in TPGs and/or ORAs. The proposed FF is based on the BISER FFs [4] and uses a reconfigurable C-element with XNOR calculation capability in place of an ordinary C-element.

This paper is organized as follows: Section 2 gives preliminary considerations and introduces two existing FFs, namely BISER and BILBO FFs. Section 3 describes the proposed FF. Sections 4 and 5 present the evaluation and conclusion, respectively.

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2. Preliminary

2.1 BISER

The proposed FF is based on an existing soft-error-tolerant FF, namely a BISER FF [4], the construction of which is shown in Fig. 1. The BISER FF is a class of master-slave FFs and consists of two master latches M1, M2, two slave latches S1, S2 and two C-elements C1, C2. The construction and truth table of the C-elements are illustrated in Fig. 2. If the same values d are input to the two inputs IN1 and IN2, the C-element outputs the inverted value $\overline{d}$. If not, the C-element keeps its previous output value which is stored in the weak keeper, and thus the output value is not changed.

The BISER FF is capable of correcting soft-errors occurring in the FF as follows: Unless a soft-error occurs, the master latches M1 and M2 store the same values as well as S1 and S2 store the same ones. Even if a soft-error occurs on M1, M2, S1 or S2 and one of the two input values of a C-element C1 or C2 becomes incorrect, the C-element keeps outputting previous correct values.

As illustrated in Fig. 1, we can insert a delay element to the input of M2. By inserting the delay element, we can correct soft-error pulses which occur on the combinational logic and are propagated to the input D with preventing the pulses from being input to M1 and M2 at the same time.

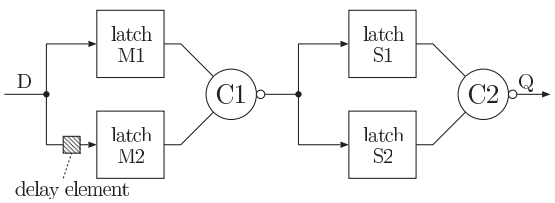
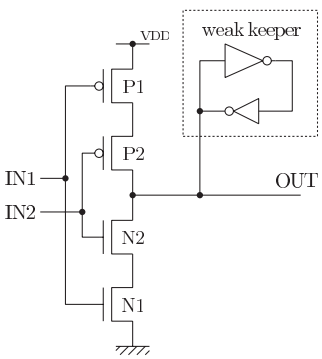


Fig. 1 Built-in soft-error resilience (BISER) FF [4].



(a) construction.

IN1	IN2	OUT
0	0	1
0	1	not change
1	0	not change
1	1	0

(b) truth table.

Fig. 2 C-element.

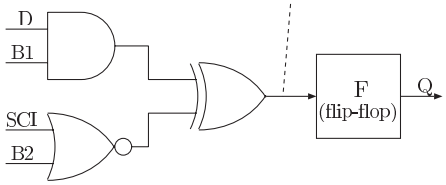
2.2 BILBO

The BILBO is a class of BIST techniques [13]. The BILBO uses BILBO FFs, the construction of which is illustrated in Fig. 3 (a). A BILBO FF consists of some gates and a normal FF F. This has a scan input SCI and two control inputs B1, B2 as well as a normal input D. Just like scan FFs, BILBO FFs are used in place of normal FFs and connected to each other in a daisy chain fashion through the scan input SCI as shown in Fig. 3 (b). It is noted that values input from SCI are always inverted as shown in Fig. 3 (a), and thus values from the previous FF to SCI are inverted. Each FF is controlled by the control inputs B1, B2. In addition, the selector at the input of the chain is controlled by another control input B3.

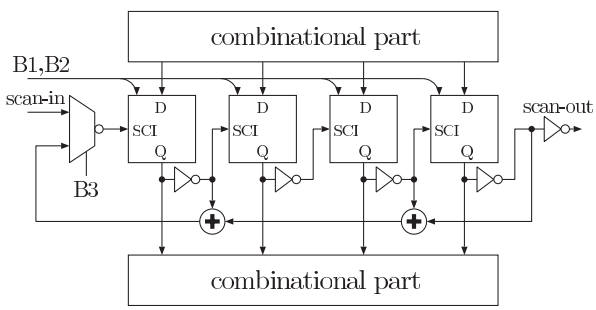
The connected BILBO FFs can work as not only ordinary scan chains but also LFSRs such as single and multiple input signature registers (SISR and MISR), which can be used as TPGs and/or ORAs. Specifically, by changing the values of the control inputs B1, B2 and B3, we can change the function of BILBO FFs as follows:

- If B1=B2=0, the inverted value of SCI is input to F and so BILBO FFs work as a scan chain or a SISR. According to the value of B3, it is decided whether they work as a scan chain or a SISR.
- If B1=0 and B2=1, logic zero is used as the input of F and thus BILBO FFs are initialized as logic zero.
- If B1=1 and B2=0, the input value of F becomes $D \oplus \overline{SCI}$. The BILBO FFs can work as a MISR.
- If B1=B2=1, D is selected as the input of F and thus

B1	B2	input to F
0	0	$\overline{SCI}$
0	1	0
1	0	$D \oplus \overline{SCI}$
1	1	D



(a) construction of BILBO FF.



(b) example of implementation.

Fig. 3 Built-in logic block observer (BILBO) architecture [13].

the BILBO FFs work as normal FFs.

3. Proposed Soft-Error-Tolerant BILBO FF

This section presents the proposed soft-error-tolerant BILBO FF, which uses a reconfigurable C-element with XNOR calculation capability. In 3.1, the reconfigurable C-element is illustrated. In 3.2, the proposed FF is explained.

3.1 Reconfigurable C-Element

Figure 4 shows the construction of the reconfigurable C-element, which differs from that of the ordinary one from the following points:

- The reconfigurable C-element has a control input B2.
- In the pass transistors N1 and N2, PMOS transistors as well as NMOS transistors are used.
- The pass transistor N1 is connected to $\overline{B2}$ and not the ground.
- A weak NMOS transistor N3 is added.

The operations of the reconfigurable C-elements are summarized in Table 1. If B2=1, then a reconfigurable C-element works as an ordinary C-element because N1 is connected to $\overline{B2}$ with logic zero and N3 is closed, and thus the reconfigurable C-element comes to be equivalent to the original C-elements. Meanwhile, if B2=0, it works as an XNOR gate from the following reason: The weak transistor N3 is opened and works as a pull-down register. If IN1=IN2=0, then P1 and P2 are opened and OUT is connected to V_{DD}. If IN1=IN2=1, then N1 and N2 are opened and OUT is connected to $\overline{B2}$, the value of which is logic one. From these, if IN1=IN2, the value of OUT becomes logic one. If IN1≠IN2, OUT is not connected to either V_{DD} or $\overline{B2}$, but connected to the ground through N3, and thus its value becomes logic zero.

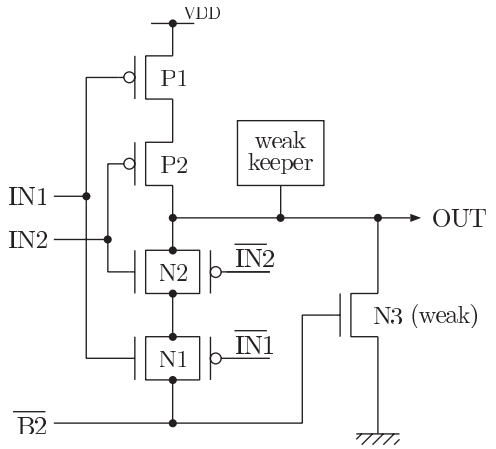


Fig. 4 Construction of reconfigurable C-element with XNOR calculation capability.

Table 1 Truth table of reconfigurable C-element with XNOR calculation capability.

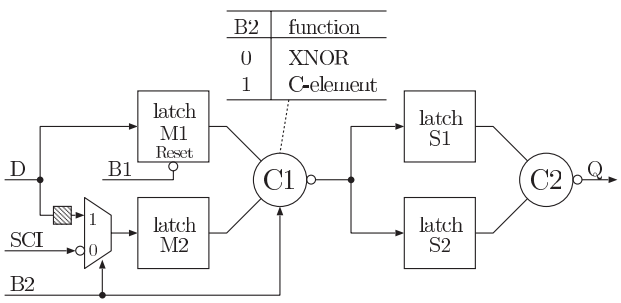
IN1	IN2	B2	OUT	function
0	0	0	1	XNOR
0	1		0	
1	0		0	
1	1		1	
0	0	1	i	C-element
0	1		not change	
1	0		not change	
1	1		0	

3.2 Construction and Operation of Proposed FF

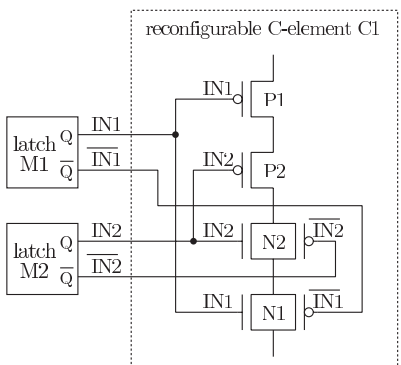
Figure 5 (a) shows the construction of the proposed soft-error-tolerant BILBO FF, which is similar to that of the BISER FFs. The difference of the proposed FF from the BISER FF is as follows:

- The proposed FF has two control inputs B1, B2 and a scan input SCI like the original BILBO FFs.
- The master latch M1 has a reset input that B1 is applied to.
- A selector is inserted at the input of M2.
- The reconfigurable C-element shown in 3.1 is used as C1.

Clock signals, which are omitted in this figure, are applied in the same way as the original BISER FFs. The proposed FFs are connected to each other in a daisy chain fashion just like the original BILBO FFs as shown in Fig. 3 (b). As shown in Fig. 4, the reconfigurable C-element requires not only input values IN1 and IN2 but also the inverted input values $\overline{IN1}$

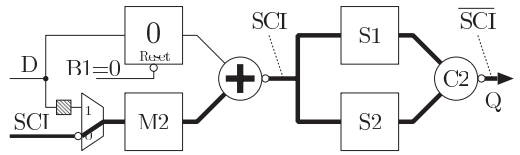


(a) construction.

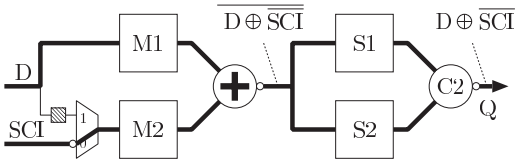


(b) connection between master latches M1, M2 and C-element C1.

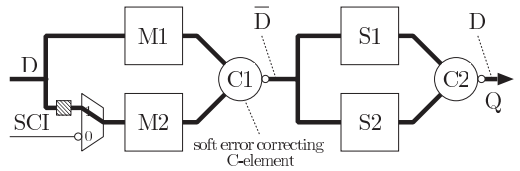
Fig. 5 Proposed soft-error-tolerant BILBO FF.



(a) B1=0, B2=0 (to work as scan chain or SISR).



(b) B1=1, B2=0 (to work as MISR).



(c) B1=1, B2=1 (to work as BISER).

Fig. 6 Operation of proposed FF.

and $\overline{\text{IN2}}$. The inputs of C1 are supplied from the master latches, and thus, as illustrated in Fig. 5 (b), we can obtain the inverted values from $\overline{\text{Q}}$ of M1 and M2 without additional inverters.

Next, the operations of the proposed FF are explained. The operations are similar to those of the BILBO FF and are summarized in Fig. 6. It is noted that the output values of C1 are finally output from the FFs after inverted by C2.

- If B1=B2=0, the proposed FFs work as a scan chain or a SISR because C1 outputs the value input from SCI for the following reason: The master latch M1 outputs logic zero because of the reset input. The inverted value of SCI is selected as the input of M2. In addition, C1 works as an XNOR gate. From these, C1 outputs $0 \oplus \overline{\text{SCI}} = \text{SCI}$ and thus the FF finally outputs $\overline{\text{SCI}}$.
- If B1=1 and B2=0, the proposed FFs work as a MISR because C1 outputs the value $\overline{\text{D} \oplus \overline{\text{SCI}}}$ from the following reason: The master latch M1 outputs the value input from D. The inverted value of SCI is selected as the input of M2. Furthermore, C1 works as an XNOR gate.
- If B1=B2=1, the proposed FFs work as BISER FFs because the input value from D is supplied to both master latches M1 and M2, and C1 works as a C-element just like the original BISER FFs. (More precisely, the value of D is supplied to M2 after delayed by the delay element.) Even if a soft-error occurs on M1 or M2, or if a soft-error pulse is input from D, it is corrected in the same way as the BISER FFs. In addition, the FFs can tolerate soft-errors on the additional lines B1, B2 as described later.
- If B1=0 and B2=1, the proposed FFs make a meaningless operation unlike the original BILBO FFs, which are reset for initialization.

This paragraph explains the reason why the proposed FFs working as BISER FFs can tolerate soft-errors on B1, B2. If the clock signal is 0, master latches are transparent and any errors are not latched into the master latches. In contrast, slave latches are closed and thus their values can incorrectly change. However, the slave latches are not connected to B1, B2, and thus their values are not changed by errors on B1, B2. If the clock signal is 1, only the master latches are closed and thus only their values can change. If an error occurs on B1, the error can change the value of M1. In contrast, it does not affect M2 and C1. Thus, it is tolerated just like errors occurring on M1. An error occurring on B2 affects both the input of M2 and the reconfigurable C-element C1 at a time. Even if the error changes the input value of M2, it does not change the value of M2, because M2 is closed. The error reconfigures C1 as an XNOR gate, which can change the output value of C1. However, after a short time, B2 returns to correct, and then C1 returns to a C-element. Both M1 and M2 keep their correct values and thus the output value of C1 returns to correct. In sum, the proposed FF tolerates soft-errors on B1 and B2.

While we can reset the original BILBO FFs by setting B1=0 and B2=1, we cannot reset the proposed FFs in this way. Instead, we can reset the proposed FFs by the following steps:

1) Set B1=B2=1 and the clock signal to 0. (The master latches M1 and M2 are transparent and their values become the same ones input from D.)
2) Rise the clock signal. (The master latches M1 and M2 are closed.)
3) Set B2=0. (The reconfigurable C-element C1 works as an XNOR gate. Since the values of M1 and M2 are the same, C1 outputs logic one. The logic one is stored in both S1 and S2. Finally, the FFs output logic zero.)

4. Evaluation

Table 2 shows a comparison between the proposed FF and four conventional FFs, namely a normal FF, a BISER FF [4], a BILBO FF [13], and a combination of BISER and BILBO FFs, which we can obtain by using a BISER FF as F in the BILBO FF shown in Fig. 3 (a). The comparison between the BISER FFs and other soft-error-tolerant FFs were demonstrated in [14] and thus not shown in this paper. The evaluated FFs are designed on a 45 nm predictive technology model [15]–[18] and simulated by HSPICE. The V_{DD} supply voltage and temperature are set to 1.0 V and 27°C, respectively. The rise and fall times of all input signals including the clock signals are set to 10 ps. Similarly to in [3], all outputs are connected with a fan-out of four inverter loads. In the simulation, soft-errors are generated with the soft-error occurrence model shown in [19], [20], namely, the double exponential model. For the three soft-error-tolerant FFs, namely the proposed FF, the BISER FF and the combination of BISER and BILBO FFs; in the simulation, delay elements shown in Figs. 1 and 5 are not placed. Use of

Table 2 Comparison with conventional FFs from the viewpoint of BILBO testability, maximal charge of tolerable particles (fC), area (ratio to one inverter), power consumption (mW) and AC characteristics (ns).

FF	BILBO testability	charge of tolerable particles	area	power consumption		AC characteristic			
						CLK-Q	D-CLK time		CLK-Q
				max	avg	delay	setup	hold	+setup
proposed FF	√	> 10,000	21.5	1.22	0.10	0.091	0.031	−0.002	0.122
BILBO [13] + BISER [4]	√	> 10,000	23.5	1.22	0.12	0.092	0.061	−0.035	0.152
BILBO [13]	√	82.6	13.5	0.78	0.06	0.050	0.059	−0.038	0.109
BISER [4]		> 10,000	17.0	1.22	0.10	0.089	0.014	0.005	0.104
normal FF		82.6	7.0	0.89	0.04	0.048	0.015	−0.001	0.064

the delay elements brings in soft-error-tolerant capability for input soft-error pulses but brings about penalties of several parameters such as area, power consumption and AC characteristics of almost the same amount among the three FFs. The evaluation for use of delay elements on the BISER FFs were already presented in [4].

The "BILBO testability" column shows whether each FF has BILBO testability. Soft-errors are generally induced by charged particles and the "charge of tolerable particles" column shows the maximal charge of tolerable particles. The evaluated FFs have several internal nodes, and a charged particle is struck at every internal node in this evaluation. This column gives the minimal result of the maximal charges for any internal nodes. If the maximal charge for a FF is high, we can regard that the FF has high soft-error-tolerant capability. The maximal charge for the proposed FF, BISER FF and the combination of BISER and BILBO FFs are higher than 10 pC. Neutron strikes generate charges up to around 150 fC [21], and thus we can conclude that the three FFs have enough high soft-error-tolerant capability for practical use. From the two columns, the only FFs with both soft-error-tolerant capability and BILBO testability are the proposed FF and the combination of BISER and BILBO FFs. The "area" column shows the area of each FF, to be precise, the area ratio of each to an inverter. While the area of the proposed FF is larger than those of BISER and BILBO FFs, it is smaller than that of their combination. The "power consumption" column gives the maximal and average power consumptions on system operations. In the simulation, a data sequence $0101\cdots$ is sent to each FF as input data at the clock frequency of 1 GHz. The values stored in the FFs change every clock cycle. The power consumption of the proposed FF is almost equal to those of the BISER FF and the combination of BISER and BILBO FFs. The "AC characteristic" column shows the AC characteristics of the evaluated FFs, namely CLK-Q delay, D-CLK setup and D-CLK hold times on system operations. Besides it shows the sum of CLK-Q delay and D-CLK setup times. In general, FFs with a short sum of CLK-Q delay and D-CLK setup times bring in high clock frequency because clock periods must be larger than the sum of the two times and the maximal path delay time on combinational parts. The sum for the proposed FF is shorter than that for the combination of BISER and BILBO FFs. On the combination of BISER and BILBO FFs, there are an AND gate, an XOR gate and a C-element C1 in addition to a master latch M1 or M2, a slave latch S1 or S2 and a C-element C2 between the input D and the output Q. On the other hand, there is only a reconfigurable C-element C1 but not an AND or XOR gate on the proposed FF. This provides the proposed FF the shorter sum compared to the combination.

5. Conclusion

This paper has proposed a construction of a FF with the following characteristics:

- The proposed FF is capable of correcting soft-errors during system operations.
- The proposed FF can work as a BILBO FF on manufacturing testing.
- The construction of the proposed FF is based on the BISER FFs, and uses a reconfigurable C-element with XNOR calculation capability.
- The area ratio of the proposed FF to an inverter is 21.5 while that of the combination of BISER and BILBO FFs is 23.5.
- The sum of CLK-Q delay and D-CLK setup times on system operations for the proposed FF is 122 ps while that of the combination of BISER and BILBO FFs is 152 ps under a 45 nm technology.

Acknowledgments

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