LETTER

Improving Test Coverage by Measuring Path Delay Time Including Transmission Time of FF

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SUMMARY As technology scales to 45 nm and below, the reliability of VLSI declines due to small delay defects, which are hard to detect by functional clock frequency. To detect small delay defects, a method which measures the delay time of path in circuit under test (CUT) was proposed. However, because a large number of FFs exist in recent VLSI, the probability that the resistive defect occurs in the FFs is increased. A test method measuring path delay time including the transmission time of FFs is necessary. However, the path measured by the conventional on-chip path delay time measurement method does not include a part of a master latch. Thus, testing using the conventional measurement method cannot detect defects occurring on the part. This paper proposes an improved on-chip path delay time measurement method. Test coverage is improved by measuring the path delay time including transmission time of a master latch. The proposed method uses a duty-cycle-modified clock signal. Evaluation results show that, the proposed method improves test coverage 5.25∼11.28% with the same area overhead as the conventional method.

key words: *small delay faults, test coverage, flip-flop, clock pulse*

1. Introduction

With the increasing speed of integrated circuits, violations of the performance specifications are becoming a major factor affecting the product-quality level [1]. Delay defects that degrade performance and cause timing related failures are emerging as a major problem in nanometer technologies [2]. Several delay fault models and delay test methods have been proposed. Transition fault and path delay fault are two prevalent fault models.

A small-delay defect is a delay defect with defect size not large enough to cause a timing failure under the system clock cycle. Usually, it is caused by resistive short, resistive open, or resistive via. Since they might escape detection during traditional Pass-Fail delay fault testing with functional clock, small-delay defects become significant problems. Moreover, small-delay defects defects can become a reliability issue because the defect might be magnified during subsequent aging in the field and cause a timing failure of the chips. Hence, it is important to detect such defects during manufacturing test [3]. Recently, small-delay defect screening with criteria based on statistical analysis was proposed [4]. However, the cost of testing and debugging for delay defects in modern high-performance chips by using external high-speed automatic test equipment (ATE) is very expensive. Moreover, it is inherently limited by the accuracy of the provided test clock frequency with the external ATE, which can be affected by factors such as parasitic capacitance, resistance of probe and tester skew, etc. [5]. On-chip path delay time measurement is one of the best alternatives to solve these problems. By measuring delay time of the path under measurement (PUM), not only the gross and small-delay faults can be detected but also the amount of timing violation in the failing paths can be obtained under certain environment conditions [6], [7].

To detect small-delay faults, some on-chip path delay time measurement methods using embedded delay measurement were proposed. Datta et al. proposed a modified vernier delay line (VDL) technique for path delay measurement [8]. High-resolution delay measurement capability can be achieved by using this method. Tsai et al. proposed a built-in delay measurement (BIDM) circuit consisting of coarse and fine blocks, which is an extension of the modified VDL technique. A built-in-self delay testing methodology based on BIDM and self-calibration methods can be developed [9]. Pei et al. also proposed an area-efficient version of the modified VDL [10]. The feature of this method is the delay range of each stage which increases by a factor of two gradually from the last to the first delay stages of VDL. Therefore, without decreasing delay measurement resolution, this method can expand delay measurement range much easier with significantly less hardware overhead. The authors' group proposed a measurement system which is different from the VDL method to improve the accuracy of the measured value [11]. This method measures two paths, a path which includes the PUM and the other path whose length is almost equal to the redundant line of the path which is measured previously. The measured delay time of the former path minus that of the latter path gives the delay time of the PUM. This method is able to give a precise measurement. In addition, a method with smaller execution time and circuit area has been proposed [12]. However, the path measured by the conventional on-chip path delay measurement method does not include a part of the master latch. Thus, testing using the conventional measurement method cannot detect defects occurring on the part. To improve the test coverage of conventional on-chip path delay measurement method, this paper proposes an improved on-chip path delay measurement method. Test coverage is improved by measuring the path delay time including transmission time of the master latch. The proposed method uses a duty-cycle-modified clock signal.

The rest of the paper is organized as follows. Sec-

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tion 2 describes the conventional on-chip path delay measurement method and explains the disadvantage of low test coverage. Section 3 illustrates the proposed method and the duty-cycle-modified clock signal for the proposed method. Section 4 evaluates the proposed method. Finally, Sect. 5 concludes this paper.

2. Conventional Small-Delay Test Method

This section introduces the conventional on-chip path delay measurement method and the small-delay defect screening with criteria based on statistical analysis. The disadvantage of low test coverage also will be explained.

2.1 Conventional Small-Delay Test Method

Figure 1 shows the architecture of the on-chip path delay measurement method of [12]. This method measures the path delay time by embedded measurement circuit. The on-chip path delay measurement system consists of delay value measurement circuit (DVMC), and circuit under measurement (CUM). The input $START$ is used to trigger the measurement system. The embedded delay measurement circuit DVMC has two input lines, *start* line and *stop* line. DVMC is used to measure the time difference between the transition signals sent to *start* line and *stop* line. The input line *clk* is the clock signal of CUM. The line clk_i is the clock line of FF_i. The lines ssg_{in} and ssg_{out} are connected to stop signal generator (SSG). The SSG is embedded in CUM. It sends the transition, which propagating to the output of an arbitrary PUM, to the *out* line of SSG. The measurement system measures the delay time of each path (each path including one PUM) whose input and output are *start* and *stop*, respectively. Therefore, the system measures the path including one clock line clk_i, a path under measurement p, and some redundant lines ssg_{in} and ssg_{out}. For example, by the measurement of the path $p' = clk_i\text{-}p\text{-}ssg_{in}\text{-}ssg_{out}$, the small-delay defects on clk_i and p can be detected.

Before the measurement, a test pattern which sensitizes p is assigned to the primary inputs and FFs of CUM. SSG is controlled to send the transition, which propagating to the output of p, to *out*. Then, we start the measurement by launching a positive transition to $START$. The transition propagates to both *start* of DVMC and *clk*. At the moment the clock rising edge reaches FF_i, a transition is launched to p. The transition reaches *stop* of DVMC through p, ssg_{in} and ssg_{out}. Then, DVMC stops the measurement. The measured delay time of p' contains the delay of redundant lines ssg_{in} and ssg_{out}. However, by using the new criterion which proposed in [4], we can detect small-delay defects occurring on path p and the segments of clock trees.

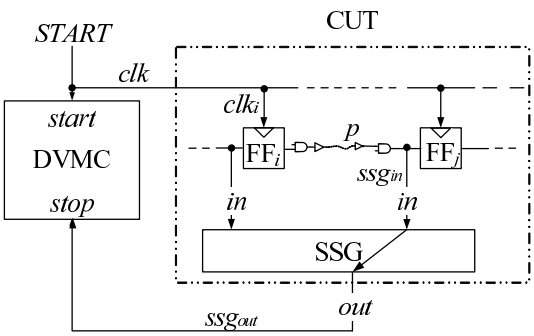

Fig. 1 Architecture of on-chip path delay measurement system.

2.2 The Disadvantage of the Conventional Method

When we measure the path delay time by using the conventional method, the master latch is not be tested. The architecture and operation of master-slave FF are shown in Fig. 2. As shown in Fig. 2 (a) master-slave FF consists of two latches, which called master latch and slave latch, connected together. Every latch consists of two inverters (INV) and two transmission gates (TG). When the clock is low, the D input is stored in the master latch, and the slave latch does not change state. When the clock is high, the output of the master latch is stored in the slave latch, and the master latch does not change state. The output of master-slave FF changes state only when the clock makes a transition from low to high.

When we measure the delay time of the path p from FF_i to FF_j by using the conventional method, the $START$ signal triggers the measurement of DVMC. At the same time, the data which stored in the master latch of FF_i is propagated to the combination circuit through the slave latch (ST1 and SI1) of FF_i. When the transition reaches the *stop* of DVMC through SSG, DVMC stops the measurement. The measured path delay time includes the delay time of the slave latch (ST1 and SI1) of FF_i, does not include the delay time of the master of FF_j. Thus, when we measure path delaydelay time by using the conventional method, the master latch is not be tested. The resistive open (short/via) defects on the master latch cannot be detected.

3. Proposed Method

This section presents a new path delay measurement method

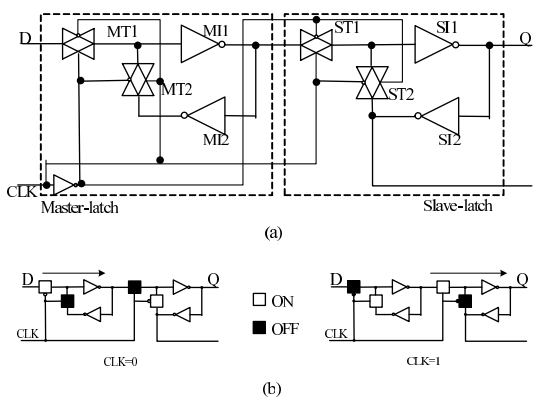

Fig. 2 (a) Architecture and (b) operation of Master-Slave FF.

to improve test coverage of the conventional delay measurement method. The proposed method changes the connection point to SSG, and uses a duty-cycle-modified clock signal.

Figure 3 illustrates the architecture of the proposed method. The path from FF_i to FF_j is PUM. The point O in the master latch of FF_j is connected to the SSG in the proposed method, while the input of FF_j is connected to the SSG in the conventional method. The proposed method measures the path delay time including the master latch of FF_j (the transmission gates MT1 and the inverters MI1 and MI2, specifically) unlike the conventional method. As a result, testing using the proposed measurement can detect resistive open (short/via) defects occurring on master latchs. Therefore the proposed method improves the test coverage compared to the conventional method.

The proposed method uses a duty-cycle-modified clock signal (illustrated in Fig. 4 (b)), because there are some paths with clock signal with the duty cycle of 50% (shown in Fig. 4 (a)). The duty-cycle-modified clock is generated outside CUT by using an arbitrary waveform generator like [13]. Imagine a path the delay time of which is shorter than 0.5×clock cycle. The state of the TG gate MT1 is OFF when the transition reaches the input D of FF_j. The transition does not appear at O until MT1 comes to be ON. Thus, we cannot measure the delay time correctly observing at O. To measure the delay time, the state of MT1 has to be set to ON before the transition reaches the input D of FF_j. We can archive it shorting the duty cycle of the clock signal such that the width of clock signal is shorter than the sum of CLK-Q delay time of a FF (T_{C-Q}) and the delay time of the shortest path (T_{Pmin}) in one circuit. In this, the state of the clock signal is low whenever a transition reaches the D input. FFs have a minimum clock width as its AC characteristic in general. If the clock width is narrower than the minimum clock width, the FF cannot work correctly. This can be a problem for the proposed method. However, it is no problem as discussed in Sect. 4.

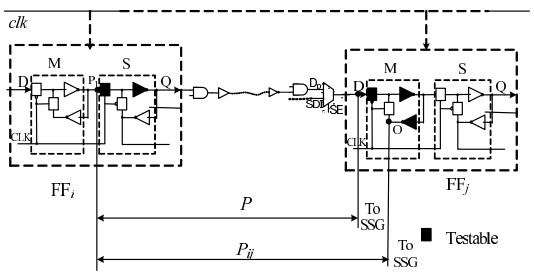

Fig. 3 Architecture of the proposed method.

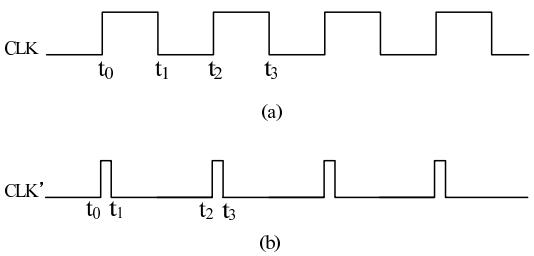

Fig. 4 (a) Conventional clock (b) duty-cycle-modified clock.

4. Evaluation

In this section, we study the test coverage improvement effect of the proposed method. Then we discuss whether the proposed method can be executed correctly. The hardware overhead also will be evaluated.

4.1 Improvement of Test Coverage

Table 1 shows the test coverage of ISCAS89 benchmark circuits by using the conventional method [12] and the proposed method. Here, test coverage is defined as the percentage of gate input and output lines included in the PUMs. Note that, we assume all the paths in one circuit can be sensitized. In Table 1, the column circuit shows the circuit name. The columns N_{gate} and N_{FF} show the number of gates and FFs in one circuit. The column *Cov* (%) reports the test coverage. The columns *CNV* and *PRO* give the results of the conventional method and the proposed method [12], respectively. The column C_{over} *(%)* shows the effect of test coverage improvement by using the proposed method. The proposed method improves test coverage 5.25∼11.28%.

4.2 Performability of Proposed Method

Table 2 shows the AC characteristics of the FFs of the conventional architecture [12] and proposed architecture, for each manufacturing process (180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm, 22 nm, using the corresponding Predictive Technology Model (PTM) [14]). In the table, *Process* and $V_{DD}(V)$ show the process technology and the supply voltage of each process, respectively. The column P_{min}

Table 1 Test coverage effect of the proposed method.

Circuit	N_{gate}	N_{FF}	*Cov(%)*		C_{over}*(%)*
			CNV	*PRO*	
S5378	2779	179	84.64	92.32	7.68
S9234	5597	228	89.49	94.75	5.25
S13207	7951	669	81.11	90.56	9.44
S35934	16065	1728	77.44	88.72	11.28
S38417	22179	1636	82.91	91.46	8.54
S38584	19253	1452	82.62	91.31	8.69
Ave			83.04	91.52	8.48

Table 2 AC characteristics of FFs.

Process	$V_{DD}(V)$	*Conventional*			*Proposed*		
		P_{min} (ps)	T_{D-O} (ps)	T_{C-Q} (ps)	P_{min} (ps)	T_{D-O} (ps)	T_{C-Q} (ps)
180 nm	1.8	100	200	240	100	240	240
130 nm	1.5	34	45	65	34	65	65
90 nm	1.4	25	32	50	25	50	50
65 nm	1.3	20	28	40	20	40	40
45 nm	1.0	18	22	30	18	30	30
32 nm	0.9	14	20	26	14	25	26
22 nm	0.8	12	18	24	12	24	24

reports the minimum width of the clock signal which can guarantee the correct work of the FF. The column T_{D-O} reports the delay time from the input D of the FF to O of the master latch. The column T_{C-Q} reports the $C-Q$ time of the FF.

As discussed in Sect. 3, to measure path delay times by using the proposed method, the width of clock signal is shorter than the delay time of the shortest path (T_{Pmin}) in one circuit. In other words, we need to meet condition of (1):

$$T_{C_1} < T_{C-Q} + T_{Pmin}, \quad (1)$$

where T_{C_1} is the width clock signal. In addition, to guarantee the correct work of FF, we need to meet condition of (2):

$$P_{min} \leq T_{C_1}. \quad (2)$$

As the evaluation results of Table 3, in each process (3) is ture:

$$P_{min} < T_{C-Q}. \quad (3)$$

Then, by setting $P_{min} = T_{C_1}$, we can meet the conditions of (1) and (2). In other words, the clock signal that satisfies the conditions of (1) and (2) is always present for every circuit. Therefore, the proposed method can measure all sensitizable paths. We do not need to set $P_{min} = T_{C_1}$ while we need to decide T_{C_1} such that T_{C_1} satisfies (1) and (2). Considering process variations and the complexity of width controlling of clock signal, we should set T_{C_1} satisfying the two by a wide margin. However, even if T_{C_1} does not meet the two, it does not bring about fault escape in manufacturing testing. If T_{C_1} does not satisfy (1), the measured delay time comes to longer than the actual one. As a result, some paths not delayed may be regarded as delayed paths, which lead to a yield loss. However, any delayed paths are detected. If T_{C_1} does not satisfy (2), the FF at the input of a path under measurement misses capturing transition, and then no transition is observed at the output of the path. Eventually, manufacturing testing fails detecting this fact.

4.3 Area Overhead

We evaluate the areas of ISCAS89 benchmark circuits, by using Design Compiler with Rohm 0.18 μm standard cells. The results are shown in Table 3. $Area_{non\_scan}$ shows the area of non-scan circuit. The column STD shows the result of the standard scan design. The columns CNV and PRO show the results of the conventional method and the proposed method, respectively. The sub column $Area$ (mm^2) shows the area, and AO (%) shows the area overhead. As the evaluation results, the area overhead of the proposed method is almost same as the conventional method.

Table 3 Area overhead.

Circuit	Area $_{non\_scan}$	STD		CNV		PRO	
		Area (mm^2)	AO (%)	Area (mm^2)	AO (%)	Area (mm^2)	AO (%)
S5378	0.059	0.064	7.74	0.075	26.78	0.075	26.78
S9234	0.102	0.108	5.80	0.116	13.24	0.116	13.24
S13207	0.187	0.205	9.24	0.220	17.49	0.220	17.49
S35934	0.458	0.503	9.73	0.537	17.18	0.537	17.18
S38417	0.500	0.543	8.46	0.566	13.16	0.566	13.16
S38584	0.482	0.520	7.80	0.541	12.14	0.541	12.14

5. Conclusion

This paper has proposed an improved on-chip path delay measurement method. Test coverage is improved by measuring the path delay time including transmission time of the master latch. A duty-cycle-modified clock signal is also used. The proposed method improves test coverage 5.25~11.28% with the same area overhead of the conventional method.

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