All switched-capacitor realized piezoresistive pressure sensor interface chip for automotive TPMS

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Abstract: An all switched-capacitor structure realized piezoresistive pressure sensor interface chip for automotive tire pressure monitoring system is presented. The propose integrated circuit consists of high resolution incremental ADC, low noise switched-capacitor amplifier, high accuracy bangdap reference and low-power relaxation oscillator and other related blocks. Proposed structure was implemented in standard $0.35\,\mu m$ CMOS process with an area of $6.1\,mm^2$. The experimental results show that the signal conditioning method provides high accuracy of 1% of the full scale output with a battery voltage from $3.6\,V$ to $2.1\,V$ over the full military temperature range. The charge consumption results into $25\,mAh$ in 10 years, including sleep mode and junction leakage current.

Keywords: pressure sensor, switched-capacitor, CDS, low power, TPMS

Classification: Integrated circuits

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1   Introduction

Nowadays, the increasing accident rate related to incorrect air pressure in vehicle has attracted public more awareness and a draft bill requiring the fitting of a tire pressure monitoring system (TPMS) in all vehicles from 2006 in USA [1]. Compared with indirect methods of measuring tire pressure, the direct way mounted inside the tire can provide a more accurate and trustworthy results. In order to achieve the required performance of operation life, at least 10 years, many low power techniques have been proposed to eliminate the power consumption, such as power manager unit, Timing optimization. For realization of ultra-low power and high accuracy sensor interface, all switched-capacitor (SC) topology is proposed, not only the incremental Analog-Digital-Convert (ADC), but also low power amplifier (LNA) and high accurate band-gap voltage reference. Moreover, due to correlated double sampling (CDS) techniques adopted in band-gap voltage reference and LNA, op-amp do not require a high output driver and lead to area and power consumption reducing and simplifying op-amp frequency compensation. Finally, experiment results are provided to verify the effectiveness of the topology.

2   The proposed all switched-capacitor topology

Fig. 1 illustrates the proposed all switched-capacitor piezoresistive pressure sensor signal interface structure. It consists of a low-power differential switched-capacitor amplifier, a high accuracy band-gap voltage reference, a high accurate incremental ADC with embedded digital filter, relaxation Oscillator and digital control unit.

Piezoresistive pressure sensor connected as a Wheatstone bridge is fabricated by Micro-Electro-Mechanical technology. In order to eliminate power consumption of pressure sensor, the bridge is switched on only during the pressure measure cycle. The sensor interface features high gain accuracy LNA to boost the pressure sensor signal prior to digitization by means of a 13 bits ADC for 1% accuracy of full scale output (FSO) of pressure sensor [2]. The ADC employs two-state single-order incremental $\Sigma\Delta$ADC structure and works at one-shot mode [5]. After power-up, the modulator and the decimation filter are reset to a well-define stage. Then, the modulator produces 13 bits binary output. Finally, the incremental $\Sigma\Delta$ADC is powered down again to save power. Since the output of piezoresistive pressure sensor is seriously dependent on absolute temperature, a temperature sensor is also realized in system with a inaccuracy of $\pm1°C$ over $-55°C$ to $125°C$ range. The temperature sensor and pressure sensor share the same LNA for small
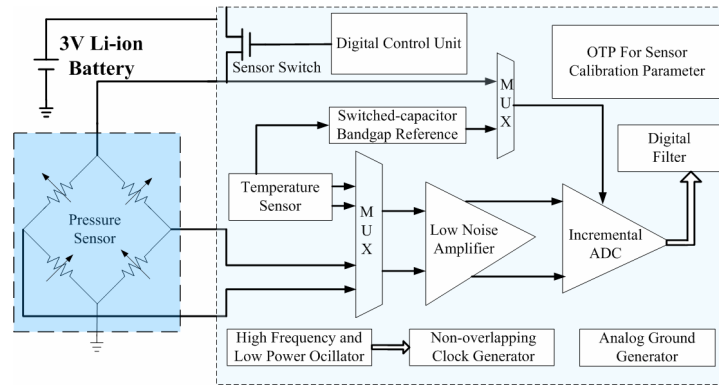
**Fig. 1.** Block diagram of the proposed sensor interface circuit

signal boost for saving area and power, but the reference voltage of incremental $\Sigma\Delta$ADC is different for their distinct ratio metric character. The temperature sensor uses a band-gap voltage and the pressure sensor adopts the Wheatstone bridge excitation voltage directly. Multiplexers are designed to select the input of LNA and reference voltage of incremental $\Sigma\Delta$ADC. A 9 bits battery voltage sensor with an accuracy $\pm100\,\text{mV}$ is also included to remind user about the low battery voltage risk.

2.1 SC CDS Band-gap voltage reference

Compared with conventional SC bandgap voltage reference [4], the proposed circuit adopts CDS technique to reduce op-amp offset voltage and finite gain effects. As shown in Fig. 2 (a), the improved structure consists of a temperature-dependent core, a SC CDS amplifier and some process calibration blocks [3]. The proportional to absolute temperature (PTAT) voltage is directly connected to the differential input of the SC CDS amplifier and the port VBE is linked to one plate of C3, as illustrate in Fig. 2 (b). The classical feedback reset switch is replaced by the elementary sample-and-hold branched consisting of capacitor C3 and their associated switches. During the sample phase (F1), capacitor C1 sample the difference emitter-base voltage of the two BJTs while C3 acts as feedback capacitor, which causes the op-amp output to change only by the op-amp input offset voltage. This is a much smaller value than the structure [4]. Since the output dynamic range is reduced, the requirement of slew-rate of op-amp is greatly relaxed and attractive to low power design. The SC amplifier's gain factor sets to be K, compensating the temperature coefficient of base-emitter voltage of the BJT Q3 to obtain a temperature-independent voltage. The VREF voltage can be written as equation (1):

$$\text{V}_{\text{REF}} = \text{K} \times \Delta\text{V}_{\text{BE}} + \text{V}_{\text{BE}}' = \text{K} \times \Delta\text{V}_{\text{BE}} + \text{V}_{\text{BE}} + 1\,\text{uA} \times \text{R}_{\text{ARRAY}} \qquad (1)$$

Since the slope of the base-emitter voltage depends on process parameters, the absolute value of the collector current and stress effect introduced by packaging, the calibration after packaging is demanded to meet high accuracy requirement. In our design, two level trimming is applied. The 5 bits fine trimming resistance array is used to obtain a trimming resolution of 31 nA and the total range of 2 uA-7 uA is sufficient to compensate for the practical process spread and variation of absolute value of biased current.
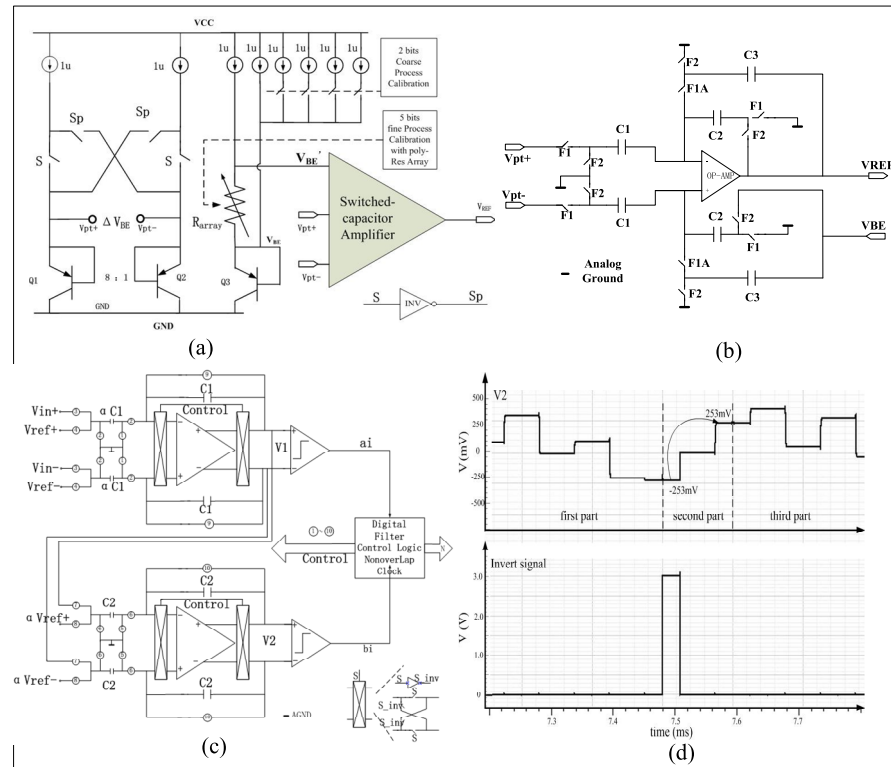
Fig. 2. (a) Proposed SC BGR, (b) SC amplifier for SC BGR, (c) Proposed incremental $\Sigma\Delta$ADC topology, (d) Integration cycle and offset cancellation

2.2 Incremental $\Sigma\Delta$ADC topology

The incremental $\Sigma\Delta$ADC includes a $\Sigma\Delta$ modulator and a digital filter, as shown in Fig. 2 (c). The modulator adopts two-stage single-order structure with a clock frequency of 20 kHz. Compared with single stage and simple counter structure demanding 2^{13} periods, only 64 periods are required to achieve a resolution of 13 bits with a conversion time of 12.8 ms. A fully differential switched-capacitor implementation is used to suppress common disturb and improve SNR. In order to avoid saturation of first stage, the gain factor of the first stage is set to 1/4. Meanwhile, the reference voltage of the second stage is also required to have the same gain factor. To guarantee negligible errors due to finite op-amp gain, a gain-boost folded cascade implementation with a DC gain of 95 dB is used. The digital filter filters out the high frequency noise and generates the 13 bits binary output from the bit-stream of two modulators. For the reason that the input offset voltage of op-amp in the modulator directly added to the ADC input and drifts along with temperature and technology process, we have to design a special timing to eliminate its effects. As shown in Fig. 2 (d), the entire integration cycle is divided into three parts: first, the modulator works normally in the first part for 64 periods; After the integration of the first part, the V2 can be shown as equation (2):

$$V_2 = (i+1) * \mathrm{i} * Vin - \sum_{j=1}^{i} a_j(i+1-j) * Vref$$
$$- \sum_{j=2}^{i+1} b_j * Vref + \mathrm{i} * (i+1) * V_{\varepsilon 1} + 2 * \mathrm{i} * V_{\varepsilon 2} \qquad (2)$$

Where $V_{\varepsilon 1}$ and $V_{\varepsilon 2}$ are corresponding op-amp offset voltage in the first and second stage modulators, and i is 64 here. Compared with traditional chopping technique [6], the proposed technique requires not only reverse of the polarity of input and output ports of both two op-amps, but also some charge transfer. The charge stored in integration capacitor of the second stage reverse and the integration capacitor of first stage is reset to zero; at the third part, the modulator operates under the same timing as the first part. The op-amp offset voltages are integrated in the same way as first integration part, but the residual offset introduced in the first part has been inversed in the second part, so at the end of third part, the effect of offset voltage has been eliminated and the effective integration voltage has been doubled. The Voltage V2 at the end of third part is:

$$V_2 = 2 * \left\{ (i+1) * \mathrm{i} * Vin - \sum_{j=1}^{i} a_j (i+1-j) * Vref - \sum_{j=2}^{i+1} b_j * Vref \right\} \quad (3)$$

The error caused by offset voltage is eliminated and the effectiveness of method is dependent on the correlation of offset voltage during the entire integration cycle and charge-injection mismatch obviously. The residual offset voltage is below $30\,\mu\mathrm{V}$, meeting the system inaccuracy requirement.

2.3 Switched capacitor low noise amplifier

A fully differential switched capacitor structure is realized in LNA with 13 bits linearity [2]. Since the sensitivity of piezoresistive pressure sensor is unique between different sensors, the LNA should have function of programmable gain. By switching the number of sampling capacitor unit, the ratio of sampling and charging capacitor is programmed and realizes a gain of 16, 20 and 24. And the error caused by op-amp finite gain is proportional to A^{-2} rather than A^{-1}, allowing using low-gain single-stage op-amp without causing large gain error [2], bringing low power benefit and simple frequency compensation. In order to satisfy the noise floor requirement limited to 1/2 LSB with 13 bit resolution, the sampling capacitor is choose to $16*1.4\,\mathrm{pF}$ at the worse condition.

3 Experiment results

The sensor interface circuit was fabricated in a standard $0.35\,\mu\mathrm{m}$ CMOS process. A chip microphotograph is shown in Fig. 3 (a). The chip area is $6.1\,\mathrm{mm}^2$
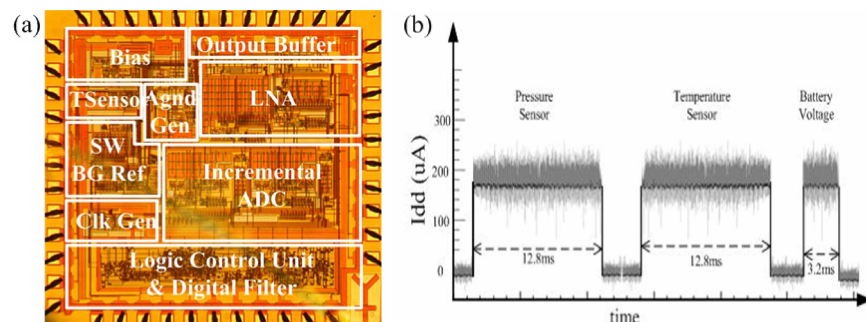
Fig. 3. (a) Chip Micrograph of sensor interface, (b) Typical charge consumption of chip at different mode

Table I. PERFORMANCE COMPARISON

Reference	Ref [9]	SP30 [7]	MPXY8300 [8]	This work
Pressure range	100 ~500 kPa	100 ~ 900 kPa	100 ~ 800 kPa	100~ 1000kPa
Temperature range	-40℃~125℃	-40℃~125℃	-40℃~125℃	-55℃ ~ 125℃
Power Supply	2.1~3.6	2.1~3.6	2.3 ~ 3.6	2.1~3.6
Sensor Type	Capacitive Sensor	Pizeoresistive Sensor	Capacitive Sensor	Pizeoresistive Sensor
Structure Comparison	without LNA SAR ADC (10bits)	——	SC LNA SAR ADC (10bits)	SC bandgap SC LNA + SC IDC (13bit)
Temperature Accuracy	——	-3 ℃~ 7℃	1℃ (Sensitivity)	±1℃
Pressure Accuracy	±5 kPa	±35 kPa	——	±(5-10) kPa
Voltage Accuracy	100mV	100mV	100mV	100mV
Pressure Consumption	——	12 μA-sec	6.28 μA-sec	2.2 μA-sec
Temperature Consumption	——	2.5 μA-sec	1.17 μA-sec	2.2 μA-sec

and temperature compensation was implemented off-chip with FPGA for testing flexibility. Fig. 3 (b) shows measured current consumptions for the different measurement mode (@ Vdd = 3 V). Since Pressure and temperature measurement share the same structure and same ADC inaccuracy, they both last 12.8 ms for a complete conversion cycle with a current of about 175 μA. For battery voltage sensor, only 3.2 ms is needed for its low accuracy requirement. The combined three measurement mode consumes total 5.04 μA-sec. Assume that the cars is running at about a quarter of their time and the TPMS measurement the data once every 5 seconds averagely, the overall charge consumption of the pure measurement is about 22.1 mAh in 10 years. Considering the measured 28 nA for low power relaxation oscillator and junction leakage current, this topology leaves a total of 90% of charge available for RF-transmission, piezoresisitive sensor an battery self-discharge with a battery capacity of 250 mAh.

Table I compares the achieved performance with previous works [9]. Since most work in this field is done in industry, the performances of related specifications of two commercial TPMS sensor have also been included in the table [7, 8]. From the table, it can be seen that the topology we realized has lower power consumption and higher temperature and pressure accuracy with a larger pressure range.

4 Conclusions

A CMOS piezoresistive sensor with all switched-capacitor structure realized has been present. The proposed topology produces an accuracy of 1% FSO over the military temperature range. CDS technique, offset-cancellation technique, high accuracy gain control and low power optimization were adopted effectively with the benefit of switched-capacitor structure. Experimental results show that the chip is capable of operating with a battery capacity of 250 mAh for 10 years, only consuming less 10% charge available.

Acknowledgments