

An ultra-low power BPSK demodulator with dual band filtering for implantable biomedical devices

Benjamin P. Wilkerson, Joon-Hyup Seo, Jin-Cheol Seo,
and Jin-Ku Kang^{a)}

Dept. of Electronics Engineering, Inha University,
100 Inha-ro, Nam-gu, Incheon 402–751, Republic of Korea

a) jkang@inha.ac.kr

Abstract: In this letter, a low-power non-coherent BPSK demodulator which is applicable to implantable biomedical devices is described. The proposed demodulator adopts the dual band filtering for recovering the timing and data in non-coherent way. The circuit has been fabricated with a 0.18 μm CMOS technology and the power consumption of the proposed demodulator is measured at 82 μW with a 2 MHz carrier frequency achieving 1 Mbps data rate.

Keywords: non-coherent BPSK (Binary Phase Shift Keying), dual band filtering, demodulator, CMOS, biomedical application

Classification: Integrated circuits

References

- [1] Y. Hu and M. A. Sawan, “A Fully Integrated Low-Power BPSK Demodulator for Implantable Medical Devices,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2552–2562, 2005.
- [2] M. Zhou, M. R. Yuce, and W. Liu, “A Non-Coherent DPSK Data Receiver with Interference Cancellation for Dual-Band Transcutaneous Telemetries,” *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2003–2012, 2008.
- [3] C.-S. A. Gong, M.-T. Shiue, K.-W. Yao, and T.-Y. Chen, “Low-power and area-efficient PSK demodulator for wirelessly powered implantable command receivers,” *Electron. Lett.*, vol. 44, no. 14, pp. 841–842, 2008.
- [4] F. Asgarian and A. M. Sodagar, “A High-Data-Rate Low-Power BPSK Demodulator and Clock Recovery Circuit for Implantable Biomedical Devices,” *IEEE EMBS Conf.*, pp. 407–410, 2009.

1 Introduction

Implantable biomedical devices are commonly used to stimulate neurons directly inside the human body. Recently, various implantable biomedical circuits that need a self-powered data communication on wireless inductive links have been developed [1, 2, 3, 4]. In a wireless data transceiver system

design for implantable biomedical devices, the power consumption of the circuit should be as low as possible with a reasonable data rate. Thus the modulation/demodulation scheme should be chosen under these design constraints. For data modulation, a PSK (Phase Shift Keying) demodulator is usually used in a coherent way. But the coherent PSK demodulator usually requires a power hungry phase-locked loop (PLL) block. For implantable biomedical devices, non-coherent methodology has an advantage in terms of power consumption and circuit complexity. In reference [2], a switched capacitor circuit with an analog integrator is used in a non-coherent DPSK (differential phase shift keying) receiver. The approach does not have a PLL circuit, but it still has an internal clock generator circuits and an analog integrator, resulting in increased power consumption and a complicated circuitry.

This letter describes a BPSK demodulator circuit with the dual band filtering and a digital deglitching circuit in a non-coherent way. The proposed circuit consumes very small power, which is applicable to implantable medical devices.

2 Proposed architecture

The proposed non-coherent BPSK demodulating scheme adopts the dual band filtering with additional timing generator to find the symbol with ultra-low power consumption. In proposed scheme, the BPSK modulated signal is first processed by marching through the LSB (Lower Side Band) and the USB (Upper Side Band) paths. The higher frequency portion of the signal exists near the phase changing boundary. The outputs from the LSB and USB comparators are used for further processing to find the recovered clock. The corner frequency is set at 2 MHz on both filters. While processing with two filters, the LPPF and the HPPF causes the phase shift on the output. The phase difference between two paths is about 90 degrees with a small variation on a targeted frequency. By processing two outputs from the LSB and USB with additional digital circuits, the data boundaries can be derived with edge pulses. By combining the LSB output with the intermediate data the carrier signal is generated. Then the clock and the demodulated data could be derived with very low power consumption.

Fig. 1 shows the proposed BPSK demodulator that consists of five major blocks: (1) a block filtering with a LSB using a comparator with a first order LPPF (Low-Pass Pre-Filter), (2) a block filtering with a USB using a comparator with a first order HPPF (High-Pass Pre-Filter) and a delay circuit for delay matching with the LSB path, (3) an EXOR circuit for generating the symbol timing pulse by detecting each phase changing edge from the LSB output and the delayed output of the USB, (4) a digital

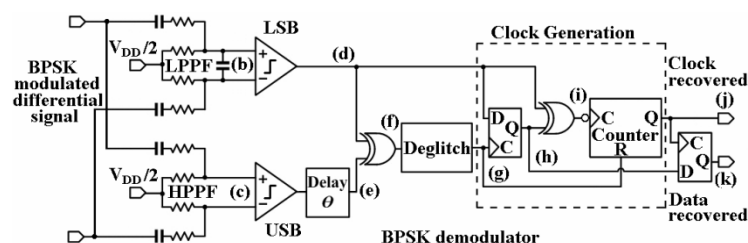


Fig. 1. The proposed BPSK demodulator

deglitching circuit for eliminating unwanted glitches caused by the misaligned timing between the output of the LSB and the USB, and (5) a clock generation and a data recovery block.

The timing diagram of the proposed BPSK demodulator is shown in Fig. 2. The LPPF works on the low frequency and the HPPF works on the high frequency portion of the signal (shown in (b) and (c)). The comparators in the LSB and USB paths digitalize the signals from the filters (shown in (d) and (e)). For recovering a symbol edge pulse, a 90 degree phase delay is added on the USB signal to find the data boundary. The delay (θ) circuit used in the USB path consists of a current mirror and a current controlled delay for generating precision controllable delay. The delay time is 125 ns for 90 degree phase shift. After adding a 90 degree phase delay from the output of USB, the phase difference between the LSB output and the delayed output of the USB becomes 180 degree. Therefore, taking the EXOR operation between the LSB output and 90 degree delayed USB output gives the symbol edge pulse with some glitches as shown in (f). These glitches come from the phase variation through the filters and inductive links. The glitch-free symbol edge timing pulse can be generated through a digital deglitching circuit. The recovered symbol edge pulse generates an intermediate data from the LSB output by the symbol edge timing pulse in (h). The signal in (i) gives the carrier pulse and the recovered clock is generated with a digital counter which could be reset by the symbol edge. The final demodulated data shown in (k) is obtained through the D F/F.

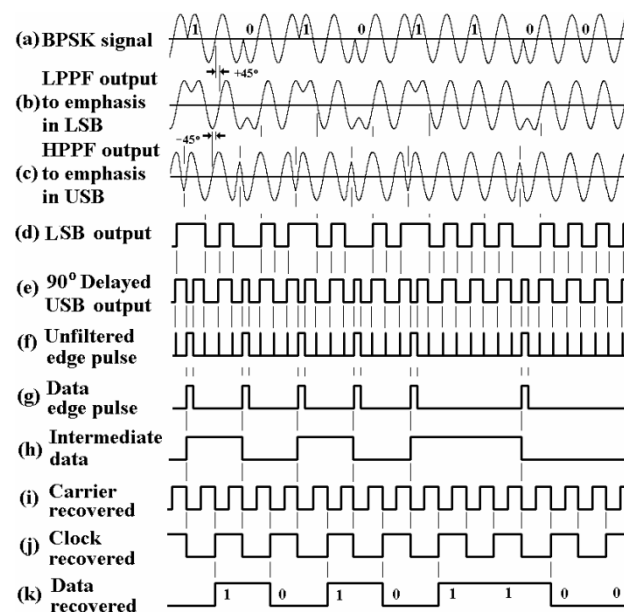
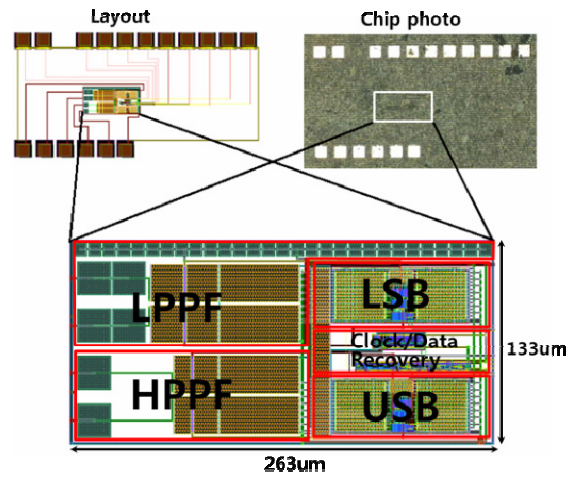


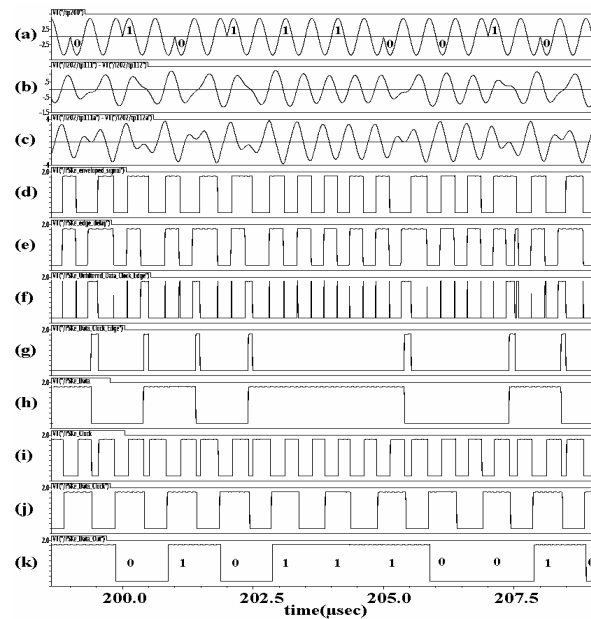
Fig. 2. Timing diagram of the proposed BPSK demodulator

3 Measurement results

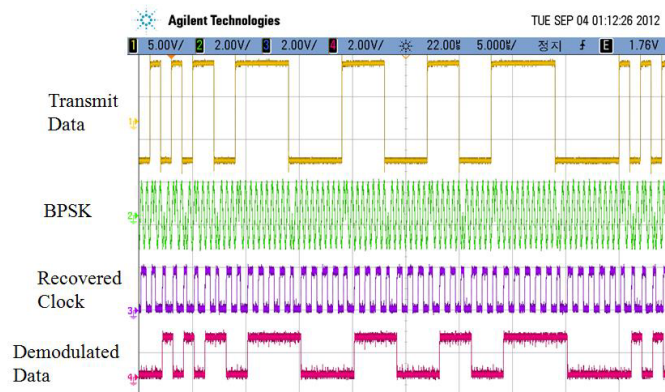
The proposed circuit has been designed with a 0.18 μm standard CMOS technology. The layout and chip microphotograph of proposed BPSK demodulators are shown in Fig. 3(a), respectively. Most areas are occupied by the RC filters and comparators with capacitors for the USB and LSB



(a)



(b)



(c)

Fig. 3. (a) Layout and chip photo, (b) simulation waveforms, and (c) measured waveforms

paths. The total chip area is $133 \times 263 \mu\text{m}^2$. The filter circuits can be improved to reduce the chip area. The carrier frequency is 2 MHz and the data rate is set at 1 Mbps. The simulation results of the proposed BPSK

receiver are shown in Fig. 3(b). The nodes shown in the Fig. 3(b) are the same as the nodes in Fig. 1. The inductive coupling factor k is set 0.5 on the inductive link for sending and receiving data on BPSK system. Therefore the signals on the filters are more degraded. The differential signals to the comparator in the LSB path have the larger signal strength at 1.5 MHz, while the differential signals of the comparator in the USB path have the larger signal strength at 2.5 MHz. The simulation also shows that the glitches on the unfiltered edge pulses are removed through the digital glitch-cancelling circuit. In the test environment the BPSK signal was generated and forwarded to the receiver. The binary input signal is transformed to BPSK signal and transmitted wirelessly. The inductive link was implemented externally. The proposed demodulator chip was mounted on the board with a chip-on-board (COB). Fig. 3(c) shows the measured results on random BPSK signals and it demonstrates the BPSK signals are demodulated correctly. The proposed BPSK demodulator consumes $82\ \mu\text{W}$ with a 1.8 V power supply. The summary of performance comparison of BPSK demodulators is shown in Table I. Compared to other works, our work shows the lowest power consumption with relatively higher data rate and lower carrier frequency. The better device for bio-implantable device transfers a higher rate data with lower carrier frequency and lower power consumption. A figure of merit (FoM) can be derived as the data rate divided by the power consumption and the carrier frequency. The last column in Table I shows the value of FoM. Compared to previous published works, the proposed circuit shows the best FoM performance.

Table I. Performance comparison with prior work

Ref. #	Carrier	Modulation	Data rate	Voltage	Power	FOM* 10^3
1	13MHz	BPSK	1.51Mbps	1.8V	$652\ \mu\text{W}$	0.18
2	20MHz	DPSK	2Mbps	5V	$6200\ \mu\text{W}$	0.02
3	4MHz	BPSK	0.2Mbps	1.8V	$59\ \mu\text{W}$	0.84
4	20MHz	BPSK	20Mbps	1.8V	$310\ \mu\text{W}$	3.22
Our Work	2MHz	BPSK	1Mbps	1.8V	$82\ \mu\text{W}$	6.09

*FOM= data rate(Mbps)/(carrier Freq. (MHz) $\times$ power(μW))

4 Conclusion

This letter presents a low-power non-coherent BPSK demodulator for implantable biomedical devices. The proposed demodulator adopts the dual band filtering and digital deglitching for demodulating data. The proposed BPSK demodulator shows power consumptions only $82\ \mu\text{W}$ using $0.18\ \mu\text{m}$ CMOS.

Acknowledgments

This work was supported by Key Research Institute Program through the NRF (2012-0005858) and by the MKE under the ITRC support program through NIPA (NIPA-2012-H0301-12-1010). CAD tools are supported by IDEC.