ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.2, 1–6

A low-power high-speed true single phase clock divide-by-2/3 prescaler

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Abstract: A novel low power high-speed true single-phase clock-based (TSPC) divide-by-2/3 prescaler is presented. By modifying the precharge branch in the TSPC flip-flop instead of the AND gate in conventional topologies, the inverter between the two flip-flops of the conventional divide-by-2/3 prescaler is eliminated, and the number of switching stages is reduced to 6. The prescaler is designed in SMIC 0.18 μm CMOS process, the simulating results show that the maximum operating frequency of the prescaler in divide-by-3 mode reaches 10 GHz with 1.836 mW power consumption, and is 50% faster than the conventional divide-by-3 circuit. The maximum operating frequency of the prescaler in divide-by-2 mode reaches 8 GHz with 1.34 mW power consumption.

Keywords: prescaler, TSPC, high-speed, low-power, CMOS

Classification: Integrated circuits

References

[1] S. Pellerano, et al., "A 13.5-mW 5-GHz frequency synthesizer with dynamic logic frequency divider," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 378–383, 2004.

[2] W. H. Chen and B. Jung, "High-speed low-power true single-phase clock dual-modulus prescalers," *IEEE Trans. Circuits Syst.II, Exp. Briefs*, vol. 58, no. 3, pp. 144–148, 2011.

[3] X. P. Yu, et al., "Design and optimization of the extended true single-phase clock-based prescaler," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 11, pp. 3828–3835, 2006.

[4] Z. Deng and A. M. Niknejad, "The speed-power trade-off in the design of CMOS true-single-phase-clock dividers," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2457–2465, 2010.

[5] M. V. Krishna, et al., "Design and analysis of ultra low power true single phase clock CMOS 2/3 prescaler," *IEEE Trans. Circuits Syst.I, Reg. Papers*, vol. 57, no. 1, pp. 72–82, 2010.

DOI: 10.1587/elex.10.20120913
Received December 03, 2012
Accepted January 07, 2013
Published January 29, 2013

1 Introduction

The prescaler is a critical building block in the frequency synthesizer, which operates at the highest frequency and consumes more power than other building blocks. Several topologies are available for prescaler in the GHz range, including current-mode logic (CML), true single-phase clocked (TSPC) logic and extended TSPC (E-TSPC) logic [1]. Without the static power dissipation, the TSPC prescaler consumes lowest power among the three topologies [2]. With the scaling down of CMOS processes, the speed improvement of the transistors makes it possible to replace the CML logic in less than 10-GHz band applications. Various TSPC prescaler are proposed to improve the speed of TSPC prescaler with less power penalty, mainly focusing on reducing the critical path delay [2], minimizing the logic gates [3] and reducing the number of transistors stacking [4]. But there is a tradeoff between the power consumption and the speed in the conventional ones. In this letter, we present a novel control logic that improves the speed of TSPC prescaler without the power penalty. The divide-by-3 operation is obtained by delaying the precharge phase of the second stage of a TSPC flip-flop by one clock cycle. During the divide-by-2 operation, one of the D flip-flops (DFF) can be shut off to save power.

2 Architecture

The conventional divide-by-2/3 dual-modulus TSPC prescaler is shown in Fig. 1 a. Though the AND gate and OR gate can be absorbed by the first stage of DFF2 in stacked logic to reduce the logic depth, the speed of the prescaler is still limited by the propagation delay of the stacked AND gate in the input stage of DFF2, thus the prescaler in the divide-by-3 mode is generally much slower than a single TSPC D flip-flop.

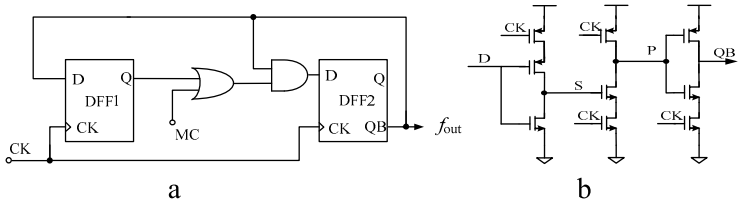

Fig. 1. Conventional TSPC divide-by-2/3 prescaler and DFF. a Conventional TSPC divide-by-2/3 prescaler, b Schematic of the TSPC DFF

There are three stages in a typical TSPC D flip-flop shown in Fig. 1 b. When CK=0, the first inverter samples the input data D, the second inverter precharges the node P to high, and the third inverter holds the output. When CK turns from low to high, the first inverter holds the input data, the second stage evaluates the data where the node P is discharged if the input QB is low, and the third stage is the output stage that passes the evaluated data to the output [2]. The divide-by-2 is obtained by connecting the output QB

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to the input D of a single TSPC DFF. The divide-by-2 operation is finished by periodically discharging, charging and holding at the node P according to QB every two clock cycles. If the charging operation at node P is delayed by an additional clock cycle, the divide-by-3 operation is obtained, therefore a new TSPC divide-by-2/3 prescaler is proposed as shown in Fig. 2 a.

When the modulus control signal MC is low, the proposed prescaler is set to be in the divide-by-3 mode. The divide-by-3 operation in this TSPC divider can be explained by the timing diagram in Fig. 2 b. During the positive cycle of CK from the timing t0 to t1, the DFF1 output Q1B is low, the added transistors M17 does not affect the behavior of DFF2. At timing t1, when CK turns from high to low, the first stage of DFF2 samples the input data and charges the node S2.

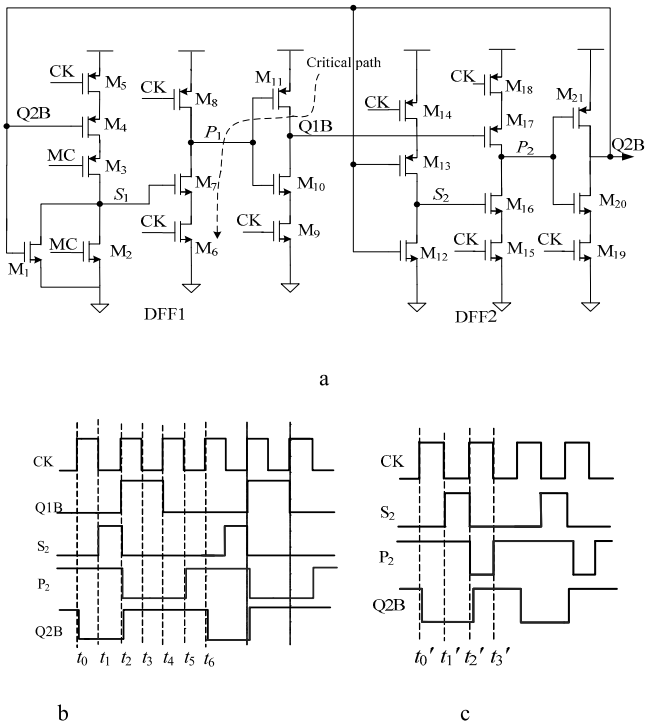

Fig. 2. The proposed TSPC divide-by-2/3 prescaler and timing. a Proposed TSPC divide-by-2/3 prescaler, b Timing diagram in the divide-by-3 operation, c Timing diagram in the divide-by-2 operation

When the clock CK turns high at timing t2, the node P2 evaluates the data, the voltage at node P2 is discharged through the transistors M15 and M16, then the output Q2B of the DFF2 toggles from low to high, and the DFF1 output Q1B also turns from low to high.

At timing t3, when the negative cycle of the clock arrives, the node P2 should be charged to high through transistors M18 and M17 if in the divide-by-2 mode as shown in Fig. 2 c. While the output Q1B of the flip-flop DFF1 is high at this time, the transistor M17 is turned off by Q1B, and the precharge

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operation of the second stage of DFF2 is stopped, the voltage at node P2 keeps low until the next falling edge of the clock.

At timing t4, the voltage at node Q1B turns low after the rising edge of the clock CK, thus the node of P2 is charged to high again at timing t5. When the next rising edge of the clock CK comes at timing t6, the output Q2B turns low, and a divide-by-3 operation is completed.

As described above, a clock cycle is swallowed by DFF2 when the output Q1B of DFF1 goes high, and the division ratio becomes three. The key points of the divide-by-3 operation is that the control signal Q1B should turn off the transistor M17 to prevent the node P2 being charged to high before the negative cycle of the clock signal. So the critical path in this divide-by-3 circuit is from P1 to M17, which is just as similar as the critical path in a divide-by-2 circuit, thus the operating speed of this prescaler in divide-by-3 mode is almost as fast as the divide-by-2 circuit composed of a single TSPC DFF.

The power consumption of the proposed prescaler is reduced in the divide-by-2 mode. In the flip-flop DFF1, the modulus control circuit is a NOR gate merged in the first stage. When the MC signal is "1", the divider is in the divide-by-2 mode, the nodes S1 and P1 of the DFF1 is set to "0" and "1" respectively, and the output Q1B is set to "0", the DFF1 is shut off and the switching activities of DFF1 is blocked.

The switching power in the divide-by-3 mode is also reduced, since there is a reduction of total number of stages in the prescaler as shown in Fig. 2 a. The inverter between the flip-flop DFF1 and DFF2 of the conventional TSPC 2/3 prescaler is eliminated, and the number of switching stages is reduced from 7 to 6 in the proposed prescaler. Furthermore, the control signal Q1B from DFF1 skips the input stage of the DFF2 and directly control M17 in the precharge stage, and the output of DFF1 only needs to drive a PMOS transistor M17, the load capacitance of DFF1 is essentially reduced compared with the conventional TSPC divide-by-3 circuit.

3 Simulation results

The proposed divide-by-2/3 is simulated in SMIC 0.18 μm CMOS process with 1.8 V supply voltage. The power consumption versus the input frequency of the divide-by-2 circuit consisting of a single TSPC DFF, the proposed prescaler and the conventional prescaler based on [2, 3, 4] are simulated respectively as shown in Figs.3 a and b. The simulation results show that the conventional 2/3 prescaler can operate up to a maximum frequency of 4.5 GHz. the divide-by-2 circuit by a single TSPC DFF can work up to a maximum frequency of 10 GHz, and the proposed TSPC prescaler in the divide-by-3 mode can operate up to 10 GHz. The proposed prescaler in divide-by-3 mode works almost as fast as the divide-by-2 circuit. The E-TSPC prescaler has the highest power consumption due to its short-circuit current. The maximum frequency of the proposed prescaler in the divide-by-2 mode is as fast as the prescaler based on Ref [2], but the power consumption

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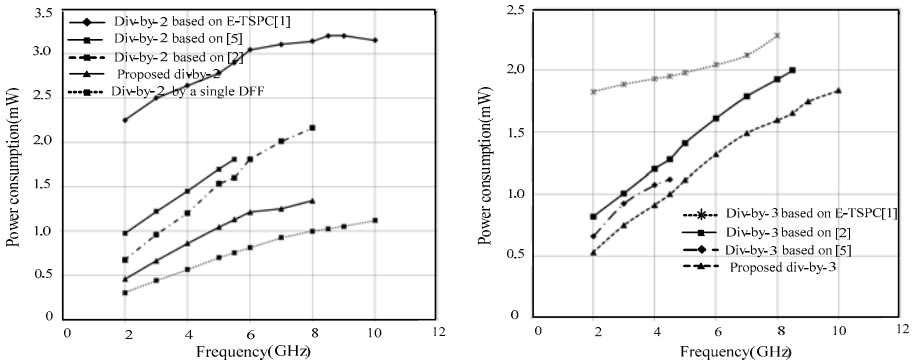
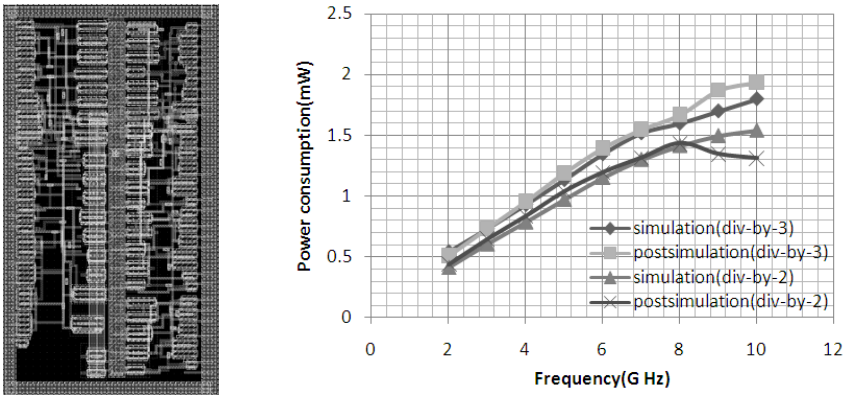


a b

Fig. 3. Performance of the proposed prescaler. a Performance comparison of the prescaler in the divide-by-2 mode, b Performance comparison of the prescaler in the divide-by-3 mode, * The prescaler in [5] has a limited input frequency no higher than 6 GHz



a b

Fig. 4. Layout and Comparison between simulation and postsimulation. a The layout of the proposed prescaler, b Performance comparison between simulation and postsimulation

is reduced by 30%. The proposed prescaler is about 20% faster than the prescaler based on Ref [2], and the power consumption is 15% less under the same operating frequency. The layout of the proposed prescaler is shown in Fig. 4 a and the core size is 55 um×30 um. Fig. 4 b shows the performance comparison between simulation and postsimulation. There is no obvious difference between two simulation conditions in both modes, which indicates the proposed prescaler has immunity against parasitic effect.

4 Conclusion

In this paper, a new high-speed and low-power divid-by-2/3 prescaler is presented. By modifying the precharge stage in the TSPC DFF, the precharge phase is delayed by a clock cycle to achieve the divide-by-3 operation. The

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inverter between the flip-flop DFF1 and DFF2 of the conventional TSPC 2/3 prescaler are eliminated, and the number of switching stages is reduced to 6 in the proposed prescaler. The simulation results demonstrate the high-speed and low-power properties of this proposed prescaler.

Acknowledgments

This work was financially supported by the National Natural Science Foundation of China No.61176031 and the National Natural Science Foundation of Jiangsu (No.BK2011334 & No.BK2011018).

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