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Examination of short calibration problem of Transmission Line Pulse

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Abstract: The degree of leaning of the Electro-Static Discharge (ESD) wave form (hereinafter referred as RON) of ESD protection parameters is closely related to the internal core circuit damage. Accurate measurement of RON requires stable short calibration with Transmission Line Pulse (TLP). In particular, for the high-precision ESD design of the thin gate oxide transistor in the most advanced technology, the high accuracy RON measurement of TLP is required. During short calibration, we found the contact resistance between the packaged sample and integrated circuit (IC) socket varied depending on the calibration current. Scanning Electron Microscope (SEM) analysis of contacts made it clear.

Keywords: Electro-Static Discharge, Transmission Line Pulse, calibration

Classification: Electron devices, circuits, and systems

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1 Introduction

For the efficient ESD design, it is important that the ESD protection circuits accept the ESD transient so that no excess current is applied to the other circuits protected against ESD. The ESD protection circuit should have enough current capability so that the voltage can be suppressed below the damage level of the protected circuit [1, 3, 4]. For this purpose, both I-V performance of the ESD protection circuit and withstand voltage of the protected circuits should be defined [1]. Recently, TLP Test system is available to analyze the electrical performance of the ESD protection circuit as well as the withstand voltage of the protected circuit, and the ESD design cannot be done without it [3, 5]. Jon Barth reported the contact resistance between needle and wafer pad during the short calibration required before the TLP measurement [3]. In many cases, TLP is measured using a wafer. However, when a failure is found in the packaged product, it is necessary to carry out TLP measurement using the packaged product. We conducted some experiments including SEM observations. In this paper, we clarified the problem of carrying out the package based short calibration using a packaged sample and IC socket.

2 ESD design window

Figure 1 is the ESD Design Window. The I-V curve in this figure is that of 65 nm technology node ESD protection circuit. Damage voltage and current are called as Vt2 and It2 respectively. The ESD protection circuit should work under the internal core circuit damage voltage and above VDD [1, 4]. The It2 should be designed to accept the requested ESD limit.

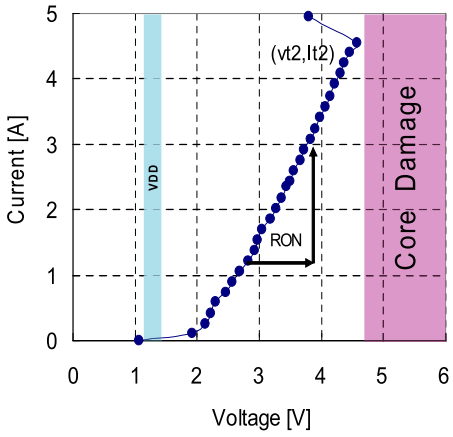

Fig. 1. I-V curve which indicated ESD design window. The damage in the internal core circuit occurs approximately more than 4.7 V area shown with red color. The appropriate ESD design window is between 1.3 V and 4.7 V.

3 RON and internal core circuit damage

Figure 2 shows three I-V curves with different RON. It also shows if the internal core circuit failed or not, assuming the internal core circuit damage voltage was 4 V or 5 V and the Human Body Model (HBM) criterion was

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2 kV (1.33 A). The curves that have"P"are the cases with no damage because the I-V curve and the damage voltage line of the internal core circuit cross above 1.33 A. On the other hand, the curves with "F" are the cases with damage because the I-V curve and the damage voltage line of the internal core circuit cross below 1.33 A. The RON of the I-V curves were approximately 1.4 Ω, 1.7 Ω and 2.5 Ω. At 1.4 Ω curve, damage did not occur with both 4 V and 5 V internal core circuit damage voltages. However, at the 1.7 Ω curve, although damage did not occur with 5 V internal damage voltage, damage did occur with 4 V internal damage voltage. The difference between 1.4 Ω and 1.7 Ω is only 0.3 Ω. This fact explains that 0.3 Ω calibration value gives big effect to ESD design in the advanced technology node. Short calibration of TLP is very important to measure the RON value accurately.

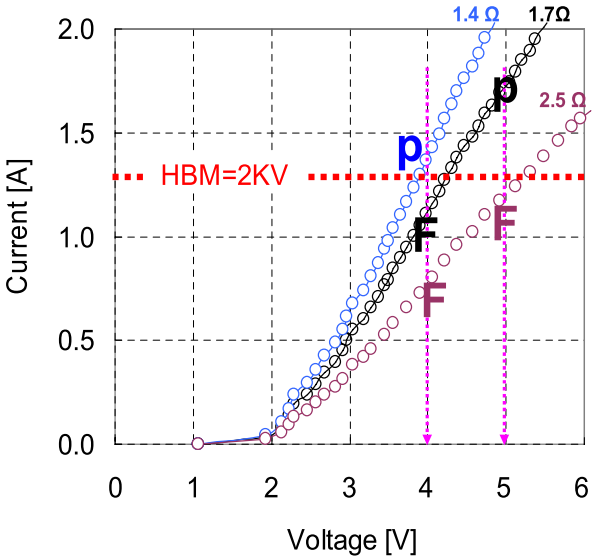

Fig. 2. Relation between RON and the internal core circuit damage voltage obtained from I-V measurements. RON is negligibly small compared to 1.5 kΩ HBM discharging resistor, HBM 2 kV current is given by 2 KV/1.5 KΩ=1.33 A.

4 Calibration and device under test

4.1 Layout pattern for calibration

For the short calibration, we made a short pattern between the adjacent pins of the device under test (DUT). The short pattern was made by connected pattern on every metal layer to get the lowest pattern resistance (nearly 0 Ω). When 0 Ω I-V line is measured from this layout pattern, I-V curve of the device itself can be measured, excluding the impedance from TLP test system to the ESD protection device, such as measurement system and bonding wire resistances. Figure 3 shows the image picture of the short layout pattern.

4.2 Device under test

A DUT of QFP208pin package was loaded in the socket, and then short calibration measurement was done by connecting IC clips from TLP test system to IC socket pins where the short pads in Fig. 3 were wired as Fig. 4.

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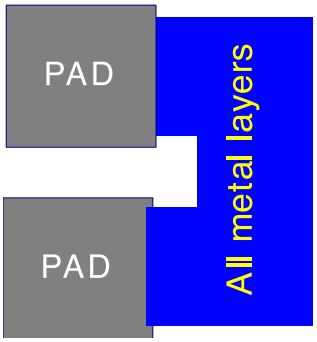

Fig. 3. Calibration layout pattern for short test. The pattern has all metal layers. Though via holes are not shown, as many as via holes located to decrease resistance.

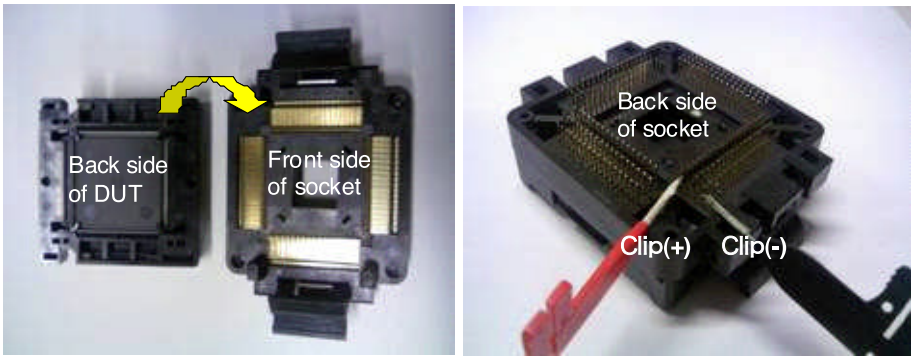

Fig. 4. Description of the procedures of calibration measurement connection.

5 Experiments

5.1 Number-of-times dependence of measurement

We applied 3 A, 5 A, 6 A, 8 A and 10 A, 2 times per each current to the short layout pattern (Fig. 3), and then measured the I-V curve using the Barth Model-4002 TLP tester without any data correction. Figure 5 are the results.

First, we applied current up to 3 A. The measured curve was very far from the ideal short calibration corresponding to 0 Ω. Next we applied current up to 3 A, one more time. Though no data correction was done, the resistance decreased a lot (second curve). Then we increased current up to 5 A. Up to 3 A point, the curve (third curve) was similar to the second curve. Up to 5 A current was applied again, and then 4th curve was derived. Resistance was decreased than third results. Similarly, by applying up to 6 A current, 5th curve was similar to 4th curve up to 5 A. But 6th curve gave lower resistance. 7th and 8th at 8 A current and 9th and 10th curve at 10 A current showed the similar variation. From the above experiment, following fact was found.

- Resistance decreases once current was applied.
- If applied current increased resistance decreased further.

At this point, it was expected that resistance at some location decreased. Furthermore, at 1 V, the difference of RON between the 1st measurement and the 10th measurement was 0.23 Ω without any data correction. This

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value is equivalent to the 0.3 Ω which was explained in Chapter 3. That is, the issue of unstable RON is a problem that affects the ESD design in the most advanced technology. To find at what location the resistance decreased, next experiment was conducted.

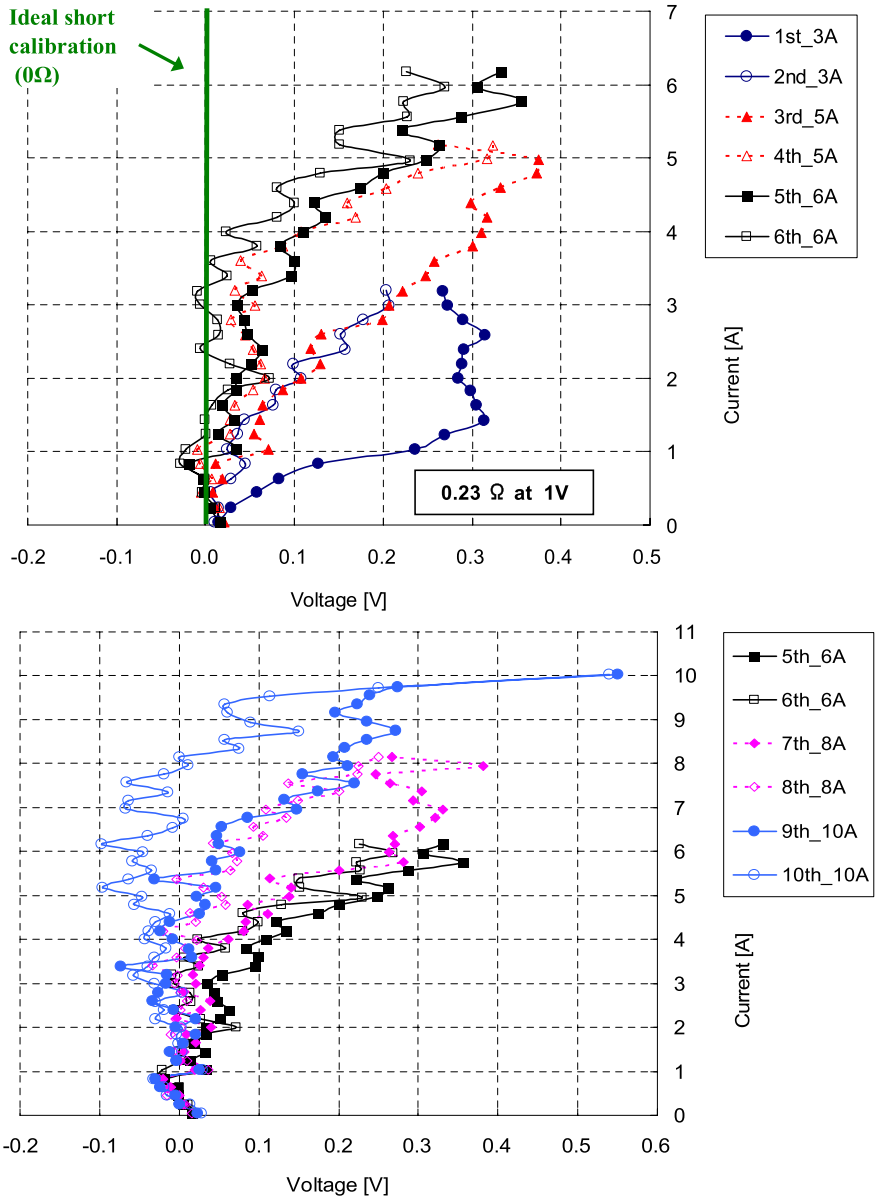

Fig. 5. The results of number-of-times dependence of measurement. I-V curve after 3 A, 5 A and 6 A (top) and I-V curve after (6 A), 8 A and 10 A (bottom).

5.2 Re-clip and re-load the DUT

Before the 11th measurement, IC clip was removed from IC socket, then re-clipped again and then measured up to 10 A. 12th measurement was done after the DUT was unloaded from the socket and reloaded again, up to 10 A. 13th measurement was the repetition of 12th measurement, up to 10 A. Figure 6 is the results. At 11th curve, no difference from curve 10th was

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observed, though IC clips were removed from IC socket leads. But, 12th curve after unloading/loading the DUT from/to IC socket gave higher resistance similar to the 1st curve in Fig. 5. 13th curve was a similar curve with 11th curve. From these experiments, it was determined that the cause of the resistance variation was the contact resistance between the sample package and IC socket. The difference of RON was 0.5 Ω at 1 V.

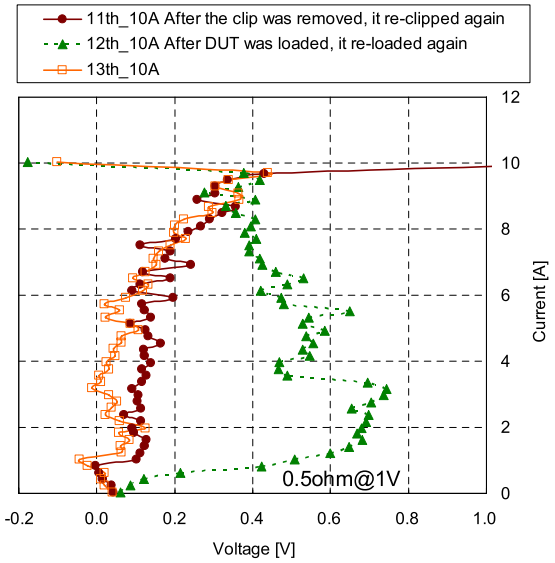

Fig. 6. I-V measurement results of re-clip and re-load the DUT.

5.3 Strong adhesion

Because contact between the DUT and socket was suspicious, we pushed the DUT in the socket, and then measured up to 3 A and 10 A twice each as Fig. 7. I-V curves were overlapped well and no resistance variation was found.

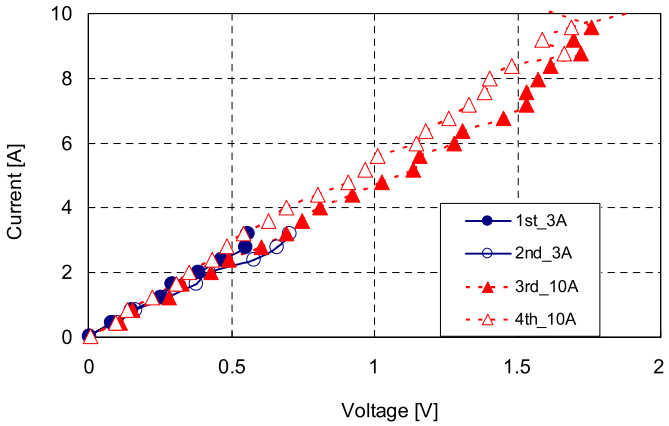

Fig. 7. I-V measurement results while pushing hard the DUT in the IC socket.

5.4 Direct clip of the pin of DUT

We tried to connect the IC clip to IC pins directly without using IC socket. Figure 8 gives the measurement results and the clip connection to DUT. The measurements were done in the same sequence as section 5-1, however no resistance variation was found. All curves were overlapped well and no

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resistance variation was detected. When clip was disconnected once and reconnected again, 11th curve was measured. The resistance difference between these (11th curve and other curves) was only 0.07 Ω that was one digit smaller than the experiments of section 5-1 and 5-2.

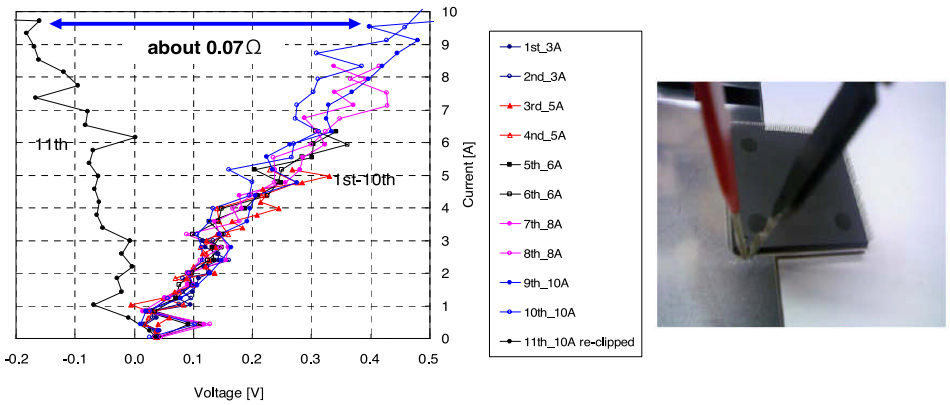

Fig. 8. I-V curve when DUT pin were direct clipped to the TLP tester (left), IC clip connection to DUT pins (right).

6 SEM observation and examination

The DUT pin (lead frame tip) is solder plated. The melting temperature is 200 degree C. Because it is not a very high temperature, it is expected that TLP high current cleans the contact, and reduces the contact resistance.

Calibration pins were pin 2 and 3 of the package. We observed SEM pictures of these 2 pins with pin 4 as the reference. Figure 9 was shown the melted solder on pin 2.

Figure 10 is the SEM picture of DUT pin surface after pressing the DUT hard to the IC socket. This informs that contact portion was scratched each

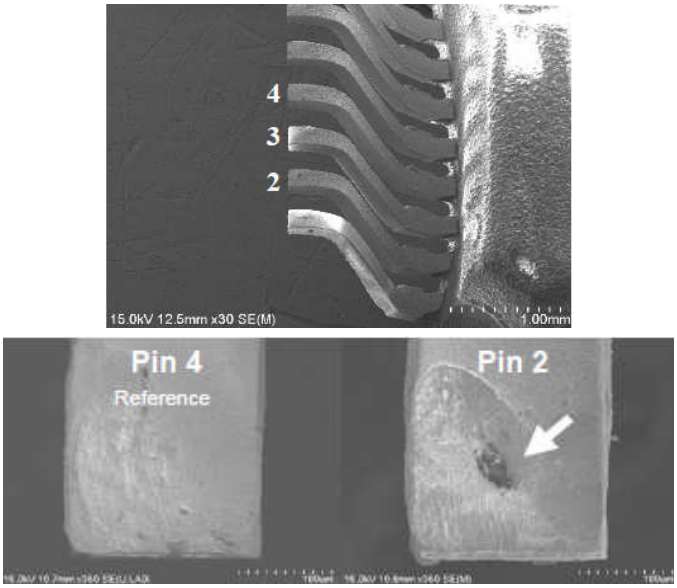

Fig. 9. SEM observation result is shown. Contact portion of the DUT to socket (top), and pin 2 after 10 A current (bottom right), and reference pin (pin 4, bottom left).

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other and contact surface was increased. Also, Fig. 11 is the SEM picture of the IC pin clipped by IC clip directly. The trace of IC clip on the IC pin easily explained that solder plate was cleaned out to assure the low contact resistance.

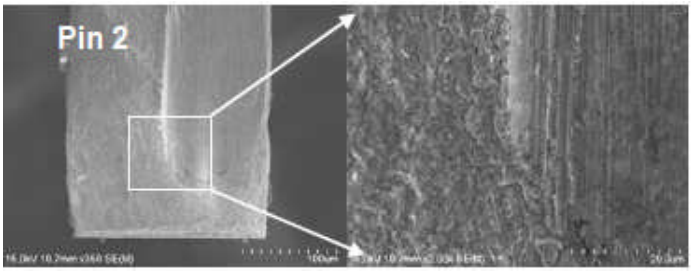

Fig. 10. SEM observation of Pin 2 after pressing the DUT hard to IC socket. Scratching extended contact surface.

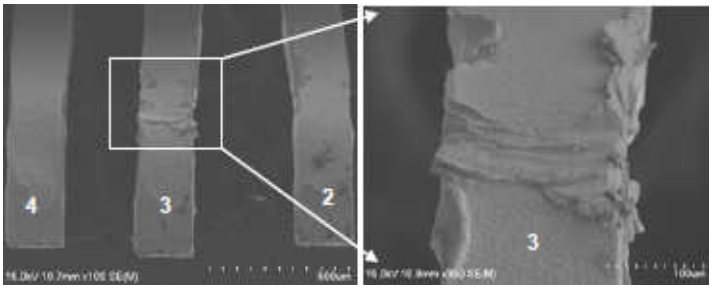

Fig. 11. SEM observation of IC pin after clipped directly. Trace of the contact between IC clip and IC pin are observed.

7 Conclusions

For the efficient ESD design of the thin gate oxide transistor in the most advanced technology, the high accuracy RON measurement is required. If packaged DUT is loaded in the socket and I-V curve is measured by TLP test system, it was found that the resistance of the I-V curve (ramp of the I-V curve) decreased by increasing measurement current. This was because of the contact resistance between DUT pin (solder plated lead frame tip) and gold plated IC socket contact. By the SEM picture analysis, trace of the solder melting by the TLP calibration current was found. The reasons why contact resistance decrease by pressing a DUT in the socket or DUT pin was direct clipped by IC clip were also found from the SEM pictures. There is package level TLP measurements requirement for the packaged product, some solutions to avoid the mismatch between short calibration and actual measurement should be provided, especially high accuracy low RON measurement is expected.

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