

Low power high-gain class-AB OTA with dynamic output current scaling

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Abstract: A high-performance operational transconductance amplifier (OTA) is proposed. In order to increase DC gain, gain bandwidth, and the slew rate under low standby quiescent current, the proposed OTA has the dynamic output current scaling and class AB operation. Under the condition of $250 \,\mu\text{A}$ quiescent current and a $30 \,\text{pF}$ load capacitance with a step voltage from 1.2 to 1.5 V at a rise time of 1 nsec in a unit gain configuration, HSPICE simulation results are presented to show a higher DC gain, gain bandwidth and slew rate than conventional OTAs.

Keywords: operational transconductance amplifier (OTA), slew rate, dynamic biasing, voltage regulators, low-dropout regulator (LDO)

Classification: Integrated circuits

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1 Introduction

The operational transconductance amplifiers (OTA) are widely used to drive large capacitive load in the LDO regulator and switched-capacitor



filter applications [1]. The OTAs have to meet several requirements such as accuracy and speed. For accuracy, high voltage gain is required, and for speed, wide bandwidth and high slew rate are needed. As shown Fig. 1(a), the current mirror OTA is conventional type, and the DC gain of the current mirror OTA is not large enough for an accurate target voltage. In addition, the large signal behavior is poor because of limited tail current.



Recently, many researchers have proposed various strategies to improve the performance of the OTA for meeting the needs of the applications specification. Typically, the conventional current mirror OTA is modified by class AB type to achieve a high DC gain [2, 3, 4, 5], and the constant tail current source is substituted by a dynamic biasing tail current for low power and a high slew rate [3, 4, 5]. However, applications still require more improved OTA performance to suit the demands of users.

In this letter, we proposed a new OTA that achieves a sufficiently high gain, gain bandwidth, and slew rate with a single-pole frequency characteristic.

2 Proposed OTA

2.1 OTA description

The alphabet under the NMOS transistors in Fig. 1 such as A, B, C and D represent their respective normalized size of the transistor. As shown Fig. 1(a), the transconductance and output resistance of the OTA [A] are shown below.





$$G_{\rm m} \text{ of OTA } [A] = g_{\rm m1,2} \times \frac{A}{B} = \frac{I_{\rm t}}{V_{\rm OD}} \times \frac{A}{B},$$
 (1)

$$R_{\text{out}} \text{ of OTA } [A] = (r_{\text{o6}} \| r_{\text{o8}}) = \left(\frac{1}{\lambda_6 \cdot I_{\text{O,Q}}} \left\| \frac{1}{\lambda_8 \cdot I_{\text{O,Q}}} \right) \\ = \frac{2}{(\lambda_6 + \lambda_8) \cdot I_{\text{t}}} \times \frac{A}{B}$$
(2)

where λ is the channel length modulation coefficient, V_{OD} is the overdrive voltage, which equals $V_{GS} - V_{TH}$ in the saturation region, I_t is the tail current, and $I_{O,Q}$ is the drain current of the output transistors. The DC gain of the current mirror OTA is

Gain of OTA [A] = G_m × R_{out} =
$$\frac{2}{V_{OD}} \times \frac{1}{\lambda_6 + \lambda_8}$$
. (3)

If the overdrive voltage remains constant, the controlling tail current does not affect the gain of the amplifier. A common practice for high gain is using a cascoded output stage; However, the cascoded output stage limits the output swing of an amplifier, so it cannot be a general solution [2]. In addition to the problem of a low DC gain, the current mirror OTA in Fig. 1(a) has a limited maximum output current ($I_{o,max}$), and as a result, a low slew rate (SR) as shown below.

SR of OTA [A] =
$$\frac{I_{o,max}}{C_{load}} = \frac{I_t \times \frac{A}{B}}{C_{load}},$$
 (4)

where C_{load} is the load capacitance. If the tail current, I_t , or the current mirror ratio, A/B, is increased for higher slew rate; however, it will also increase the quiescent current. Since the small handheld devices are gaining popularity, higher quiescent current cannot be tolerated in such portable systems.

So, we proposed a new OTA, which achieves sufficient high gain, bandwidth, and slew rate with small quiescent current and a single-pole frequency characteristic.

2.2 Proposed scheme description

In order to achieve a high DC gain, the output resistance must be increased. However, as mentioned earlier, cascoding limits the output voltage swing, so the use of cascoding is avoided. A solution to increase the output resistance is reducing the tail current as shown in (2); however, reducing the tail current in the OTA [A] proportionally reduces G_m such that the overall gain does not change. In addition, reducing the output current directly contradicts the requirement of a high slew rate.

As shown in Fig. 1(b), the OTA [B] is to increase the DC gain by adding an extra control circuit [3]. The OTA [B] has two voltage controlled current path. The transistors, M11, M12, M13, and M14 sense the input differential voltage, and control M9 and M10. The total transconductance of OTA [B] is as follows:

$$G_{\rm m} \text{ of OTA } [B] = (g_{\rm m1,2} + g_{\rm m11,12}) \times \frac{A}{B} \times \frac{B + 2C}{B + C + D}$$
 (5)





The quiescent output current can also be represented by Equation (6).

$$I_{O,Q} \text{ of OTA } [B] = \frac{I_t}{2} \times \frac{A}{B+C+D}$$
 (6)

As a result, the output resistance is increased as shown below.

$$R_{out} \text{ of OTA } [B] = \frac{2}{\lambda_6 + \lambda_8} \times \frac{B + C + D}{A}$$
(7)

Both transconductance and output resistance of the OTA [B] are increased, so the overall gain increase is significant. The important OTAs parameters are summarized in Table I. It is evident that the OTA [B] has advantages in terms of the transconductance, output resistance, and gain. Under the same quiescent currents, the OTA [B] has a significantly higher slew rate, but the slew rate is still limited by the tail current.

Table I. Comparison of the performances of the OTAs $(A = 2, B = 1, C = 4, D = 1, I_t = 250 \,\mu A, C_L = 30 \,pF, V_{DD} = 3 \,V).$

	OTA [B]		OTA [C]		OTA [new]	
	Eq.	Sim.	Eq.	Sim.	Eq.	Sim.
G _m	$(g_{m1,2}+g_{m11,12}) \times \frac{A}{B} \times \frac{B+2C}{B+C+D}$	0.88 mA/V	$2 \cdot \left(g_{m1,2} \times \frac{A}{B}\right)$	0.479 mA/V	$2 \cdot \left(\left(\underline{\textbf{g}}_{\texttt{m1,2+}} \underline{\textbf{g}}_{\texttt{m11,12}} \right) \times \frac{\textbf{A}}{\textbf{B}} \times \frac{\textbf{B+2C}}{\textbf{B+C+D}} \right)$	1.46 mA/V
R _{out}	$\frac{2}{(\lambda_{\delta}+\lambda_{\delta})\cdot I_{t}}\times \frac{B+C+D}{A}$	1.01 MΩ	$\frac{2}{(\lambda \delta + \lambda 8) \cdot I_{t_dynamic}} \times \frac{B}{A}$	0.965 MΩ	$\frac{2}{(\lambda_{\text{b}}+\lambda_{\text{B}})\cdot I_{t_\text{dynmaic}}} \!\!\times\!\!\frac{B\!+\!C\!+\!D}{A}$	1.1 MΩ
Gain	$\frac{2}{V_{\text{OD}}} \times \frac{1}{\lambda_{\text{S}} + \lambda_{\text{S}}} \times \frac{B + C}{B}$	59 dB	$\frac{4\times g_{m1,2}}{(\lambda_6+\lambda_8)\cdot I_{t_dynamic}}$	53.3 dB	$\left(\frac{4 \times \left(g_{m1,2} + g_{m11,12}\right)}{\left(\lambda_6 + \lambda_8\right) \cdot I_{t_dynamaie}}\right) \! \times \! \left(\frac{B + 2C}{B}\right)$	64.1 dB
Ι _{ο.Q}	$\frac{It}{2} \times \frac{A}{B+C+D}$	70.6 µA	$\frac{I_{t_dynamic}}{2} \times \frac{A}{B}$	53.1 µA	$\frac{I_{t_dynamic}}{2} \times \frac{A}{B+C+D}$	47.7 µ A
I _{O.Q T} otal	$I_t + 2 \times I_{\text{O},\text{Q}}$	250 µA	$I_{t_dynamic} + 2 \times I_{O,Q}$	250 µA	$I_{t_dynamic} \ + 2 \times I_{O.Q}$	250 µA
I _{O.max}	$I_t \!\times\! \frac{A}{B} \!\times\! \frac{B+C}{B+C+D}$	191 µ A	$I_{t_dynamic} \times \frac{A}{B}$	140 µA	$2 \cdot \left(I_{t_dynamic} \times \frac{A}{B} \times \frac{B+C}{B+C+D} \right)$	223 µA

X The performance of the OTA [A] is shown in the Ref. [2].

Therefore, another solution is a well known dynamic biasing scheme, the OTA [C] in Fig. 1(c) [3]. The OTA [C] features dynamic current sourcing capability depending on the differential input signal [5]. The OTA [C] consists of two matched transistors, M03' and M04' acting as DC level shifters. The M04' transistor senses the variation of the plus input voltage (V_P) and acts as a source follower amplifier. Then, M1 and M11 amplify the variation of V_P , acting as a common gate amplifier.

In order to achieve a more higher DC gain and slew rate, we proposed the OTA [new] shown in Fig. 1(d), which consists of a mixed topology of OTA [B] and OTA [C]. As shown in Fig. 1(d), by adding a extra signal path of (2), (3), and (4), the total transconductance of the OTA [new] is double that of OTA [B].





$$G_{m} \text{ of OTA [new]} = 2 \times (g_{m_OTA [B]})$$
$$= 2 \cdot \left(\left(g_{m1,2} + g_{m11,12} \right) \times \frac{A}{B} \times \frac{B + 2C}{B + C + D} \right) \quad (8)$$

Also, the quiescent output current can be expressed as

$$I_{O,Q} \text{ of OTA [new]} = \frac{I_{t_dynamic}}{2} \times \frac{A}{B+C+D}, \qquad (9)$$

where $I_{t_{dynamic}}$ is the dynamic tail current from the operation of OTA [new]. As a result, the output resistance is increased to

$$R_{OUT} \text{ of OTA [new]} = \frac{2}{(\lambda_6 + \lambda_8) \cdot I_{t_dynmaic}} \times \frac{B + C + D}{A}.$$
(10)

Since both transconductance and output resistance are increased, the overall gain increase in the proposed OTA [new]. One drawback of the OTA [new] is the creation of an extra non-dominant pole. The diode-connected transistors, M13 and M14 create an extra pole, so the overall frequency response should be carefully examined. However, the small-signal resistance at the drain of M13 and M14 is small, 1 of g_m , so the extra pole at that node is at the high frequency.

The important OTA parameters and the comparison of the OTAs [Anew] are summarized in Table I. We can see the OTA [new] has advantages in terms of the transconductance and output resistance. Under the same total quiescent current of the OTAs, the OTA [new] results in a significantly higher DC gain and slew rate than the conventional OTAs [A-C].

3 Simulation results

The OTA was simulated in a 180 nm CMOS technology. The normalized values, transistor size of A and B in the OTA [A] were 2 and 1, respectively, while the normalized values of A, B, C, and D in the OTA [B] were 2, 1, 4, and 1, respectively. The transistors all had the same length of 1 μ m and the widths were determined to have an overdrive voltage of about 200 mV with a supply voltage of 3 V. For fair comparison of the performances of the OTAs, the total quiescent current was set at 250 μ A.

Fig. 2 shows the AC simulation of the OTAs with a 30 pF load capacitor. The DC gain of the OTA [new] increased significantly. The DC gain of the OTAs [A-C] were 48.5 dB, 59 dB, and 53.3 dB while the OTA [new] demonstrated the DC gain of 64.1 dB. And the unity-gain frequency of the OTAs [A-C] were 1.5 MHz with 89.5°, 4.6 MHz with 86.3°, and 2.55 MHz with 86.2° phase margins, while the new OTA demonstrated a unity-gain frequency of 7.64 MHz with a 83° phase margin. The effect of non-dominant poles slightly decreased the phase margin of the OTA [new], but a sufficient phase margin was still achieved.

The step response of the OTA [new] is shown in Fig. 3 to confirm the stable operation, and the proposed OTA [new] has the best slew rate performance. The proposed OTA [new] has the fastest settling time of $0.08 \,\mu$ sec when the positive input voltage was varied from 1.2 to 1.5 V at a rise and fall time of 1 nsec.







Fig. 2. Results of the AC simulation



Fig. 3. Results of the step response simulation

4 Conclusion

A high-performance OTA architecture with single-pole characteristics was proposed in this letter. Instead of using a cascoded output stage, the proposed OTA [new] achieved a high DC gain. To achieve a high DC gain, the proposed OTA [new] is designed as a class-AB circuit. The output current increased dynamically by adaptive biasing which is the tail current boosting of the input differential stage.

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