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Effect of double-patterning and double-etching on the line-edge-roughness of multi-gate bulk MOSFETs

In Jun Park and Changhwan Shin[a)]

School of Electrical and Computer Engineering, University of Seoul, 90 Jeonnong-dong, Dongdaemu-gu, Seoul 130–743, Republic of Korea

a) *cshin@uos.ac.kr*

Abstract: Quasi-planar tri-gate (QPT) bulk metal-oxide-semiconductor field-effect transistors (MOSFETs) are fabricated by a low-power 28-nm complementary metal-oxide-semiconductor (CMOS) technology, in order to investigate the effect of double-patterning and double-etching (2P2E) on the line-edge-roughness (LER) as well as on the LER-induced threshold-voltage (V_{TH}) variation. We experimentally verified that the LER profile obtained by the 2P2E 193 nm immersion photolithography technique has a relatively lower spatial frequency (*i.e.*, longer correlation length) than that obtained by the conventional (*i.e.*, single-patterning and single-etching, or 1P1E) photolithography technique, although they have a comparable root-mean-square deviation and fractal dimension. Using Monte Carlo (MC) simulations to analyze the random V_{TH} variations in the QPT bulk MOSFETs, we confirmed that the 2P2E-LER-induced V_{TH} variation is much smaller than the total V_{TH} variation in the 28 nm QPT CMOS technology.

Keywords: CMOS, multi-gate, MOSFET

Classification: Electron devices, circuits, and systems

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1 Introduction

The transistor density in integrated circuits has almost doubled with each new generation of the complementary metal-oxide-semiconductor (CMOS) technology, primarily because of the steady miniaturization of the transistor size. To maintain scaling of the transistor size in sub-30 nm CMOS technology nodes, the double-patterning technique, which employs the 193-nm immersion photolithography, has been introduced in production because of the limited wavelength of the lithography system currently used. In addition, the scaled metal-oxide-semiconductor field-effect transistors (MOSFETs) at the sub-30-nm nodes suffer from a significant number of random variations such as line-edge-roughness (LER), random dopant fluctuation (RDF), and work function variation (WFV); therefore, non-conventional transistor architectures such as the ultra-thin-body and/or multi-gate MOSFET are being considered in the industry [1, 2]. In this study, the effect of the double-patterning and double-etching (2P2E) technique on the random variation (especially the LER) of multi-gate bulk MOSFETs is investigated.

2 Process flow of the multi-gate bulk MOSFETs

The front-end-of-line fabrication sequence is shown in Fig. 1 (a). A simple method (*i.e.*, timed etch in dilute hydrofluoric (DHF) acid to recess shallow trench isolation (STI) prior to gate stack formation) was used to achieve quasi-planar tri-gate (QPT) bulk MOSFETs using an otherwise conventional fabrication process [3]. Note that B with ~ 100 keV in the order of 10^{13} cm^{-2} and BF_2 with ~ 30 keV in 10^{13} cm^{-2} are implanted in the channel region, as the P-well and V_{TH}-adjustment ion-implantation. The halo ion implantation

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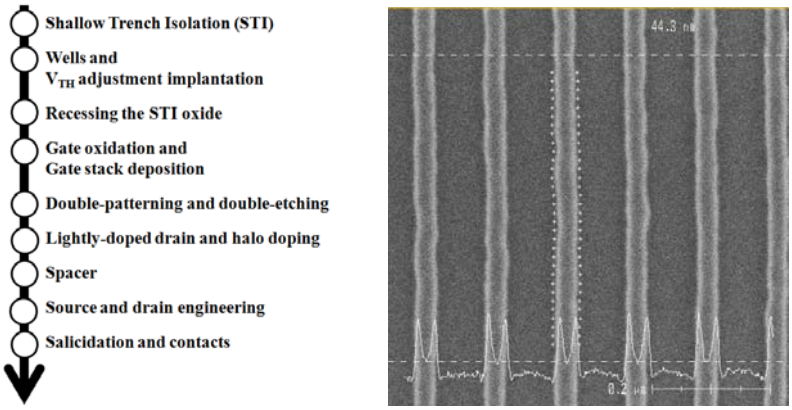

Fig. 1. (a) Sequence of the front-end-of-line CMOS fabrication process, (b) Plane view of the SEM image from a test structure that investigates the LER profile.

(*i.e.*, B with 30° tilted, 6.5 keV in 10^{13} cm^{-2}) is also performed in the channel region.

3 LER characterization

The 2P2E semiconductor fabrication process that employs the 193-nm immersion photolithography technique and advanced hard-mask etching techniques for the 28/22 nm CMOS technology node were used. Fig. 1 (b) shows the scanning electron microscopy (SEM) image of the test structure used in monitoring both the critical feature sizes and the LER. In order to quantitatively characterize the LER [4], three parameters were extracted out: (i) the root-mean-square deviation (σ), (ii) the correlation length (ξ), and (iii) the fractal dimension (D). σ represents the value of the fluctuating amplitude of the LER profile along the side line of the test structure, ξ represents the spatial frequency of the line-edge shape, and D represents the slope of the power spectrum plot of the line-edge shape. Table I summarizes these parameters in comparison with the conventional photolithography parameters (single-patterning/single-etching, or 1P1E).

Table I. Three parameters extracted from the 20 test structures across a 300 mm wafer.

Lithography	Root-mean-square (nm)	Correlation length (nm)	Fractal Dimension (unit-less)
2P2E	1 ~ 2	20 ~ 40	1.7 ~ 1.9
1P1E	1 ~ 2	< 15	1.6 ~ 1.9

From the statistical and experimental data (Table I), it was found that the 2P2E-based LER profile showed a slightly longer correlation length, (*i.e.*, lower spatial frequency) than the 1P1E-based LER profile. This result is primarily obtained when the feature is printed in two exposures (technically,

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the spaces between them are patterned, and not the features); the left and right edges of the features are patterned under different exposures. This minimizes the effect of the LER-induced V_{TH} variation mainly because of the smoothened LER profile in the channel width direction. Its Monte Carlo (MC) simulation is presented in the next section.

4 MC simulation of the 2P2E-LER-induced V_{TH} variation in QPT MOSFETs

The 2P2E-LER profile obtained from the experimental results (Fig. 1 (b)) is utilized in generating both sides of the gate electrode in the QPT bulk MOSFET. Fig. 2 shows the top view of a QPT MOSFET with a 2P2E-LER experimental profile. The LER profile on the left-hand side along the channel width is different from that on the right-hand side because the LER on one side is not correlated with the other side, unless the spacer lithography is used [5].

To accurately model the on-state current for the short channel lengths, the experimentally-calibrated hydrodynamic model (*i.e.*, the energy relaxation

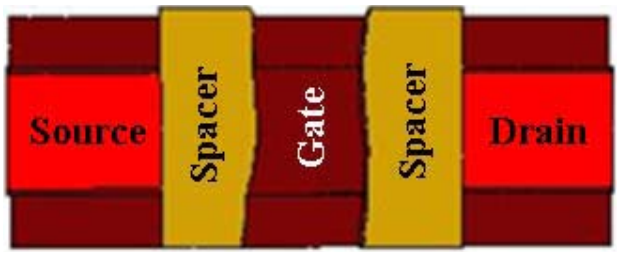

Fig. 2. Top view of the n-type QPT bulk MOSFET with a 2P2E-LER experimental profile. The gate electrode is not shown to clearly depict the LER profiles on both sides next to the spacer. In this study, $W_{eff}/L_{eff} = 60/36$ nm.

Table II. The MC simulation results that take into account the 2P2E-LER only (second column), the 2P2E-LER with RDF (third column), the 2P2E-LER with RDF and WFV (fourth column), and the experimental results that consider the systematic and random variations (last column). The ratio of LER/RDF/WFV with respect to the total variation of $V_{TH,Sat}$ and of VTH, Lin is 25.2/66.3/70.5% and 18.9/55.1/81.3%, respectively. The power supply voltage (V_{DD}) is 1.0 V; $V_{TH,Sat}$ and $V_{TH,Lin}$ are measured with V_{DS} = 1.0 V and 0.1 V, respectively.

V_{TH} variation (mV)	2P2E-LER only	2P2E-LER + RDF	2P2E-LER + RDF + WFV	Experiment
$\sigma(V_{TH,Sat})$ (mV)	12.2	34.3	48.6	49.1
$\sigma(V_{TH,Lin})$ (mV)	7.0	21.6	37.0	38.5

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time of the electrons and holes was adjusted to match the MC simulation results, so that it was changed to 0.14 ps) was used in the MC simulations. The simulations generated and simulated 200 different samples to estimate the V_{TH} variation caused by the 2P2E-LER only and by LER + RDF + WFV (compared with experimental results). Table II summarizes the MC simulation and experimental results. We confirmed the following: (i) the 2P2E-LER did not significantly contribute to the total random variation and (ii) RDF/WFV [6, 7] were the dominant variation sources in the QPT bulk MOSFET at the 28-nm node.

5 Conclusion

Multi-gate bulk MOSFETs have been fabricated by the low-power 28-nm CMOS technology using the 2P2E technique. Among the three parameters (*i.e.*, σ, ξ, and D) that characterized the LER, the correlation length only increased in the profile that used the 2P2E LER. The experimentally calibrated MC simulation results verified that the effect of the 2P2E LER-induced V_{TH} variation on the total V_{TH} variation was insignificant.

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