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A 5 MHz integrated digital DC-DC converter with a delay-line ADC and a Σ-Δ DPWM

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Abstract: An integrated digital buck DC-DC converter based on a 0.5 μm standard CMOS process is presented in this paper. Its switching frequency is 5 MHZ and no extra high frequency clock is needed. The delay-line ADC with a self-calibration loop utilized in the converter has low sensitivity to the process, voltage, temperature and loading (PVTL). The DPWM in the proposed DC-DC converter employs a first-order Σ-Δ modulator to achieve an equivalent resolution of 10-bit. The simulation results show that the proposed DC-DC converter can operate at the supply voltage range of 2.7 to 3.6 V with a transient response time of 30 μs. The peak efficiency reaches 94%.

Keywords: DC-DC converter, digital PID control, delay-line ADC, Σ-Δ modulator, DLL

Classification: Integrated circuits

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1 Introduction

With the development of the semiconductor process, the digital DC-DC converter becomes extremely attractive, because it has a lower cost, a shorter design period, more advanced controls, lower sensitivity to the parameter variations and less off-chip devices than the analog controlled DC-DC converter [1, 2, 3]. Besides that, many parameters in the digital DC-DC converter such as switching frequency and output voltage could be optimized according to the system where the converter is applied [4].

The block diagram of a conventional digital DC-DC converter is shown in Fig. 1. It is composed of a power stage and a feedback network. The power stage contains a switch M_P, a synchronous switch M_N and an output filter. The error between the feedback voltage V_{FB} and the reference voltage V_{ref} is quantized by an ADC. By a series of operation on the quantized error e[k], the digital PID Controller generates the duty cycle signal d[k+1].

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According to the duty cycle, the rectangular wave signal is attained through the DPWM to control the on-time and off-time of the power switches in each switching period. Thus, the output voltage is adjusted to a desired value. In order to obtain good performances, three function blocks i.e. the ADC, the PID controller and the DPWM should be well-designed.

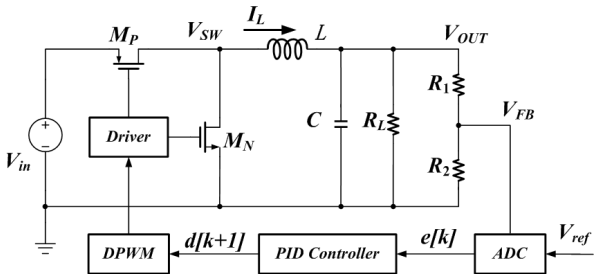

Fig. 1. Block diagram of the digital DC-DC converter

Obviously, the traditional ADC is not suitable for the digital DC-DC converter because of its large power consumption and die size. The ADC applied in the DC-DC converter could have a small dynamic range but a high resolution as only a small range around the reference voltage needs to be accurately quantized. Furthermore, the conversion time should be short, so that there would be enough time for the PID controller to finish its operations and the control loop delay can be minimized. Many structures of the ADC applied in the DC-DC converter have been proposed [5, 6, 7]. The ADC presented in [5] utilizes the feedback voltage to control the frequency of the oscillator, so that the feedback voltage could be detected by counting the number of the rising edges in one switching period. The main concern of this method is that the counter may give different results under the same inputs due to the randomness of the clock phase at the beginning of counting. The delay-line ADC [6, 7] is brought to the notice of the digital DC-DC designers owing to its low power consumption and small die size. However, the delay time of the delay-line is sensitive to the process, voltage, temperature and loading (PVTL).

As for the DPWM design, firstly the resolution of the DPWM should be finer than the resolution of the ADC to eliminate the limit cycles [8]. Generally, there are three kinds of DPWM implementations i.e. counter-comparator, ring-oscillator and hybrid DPWM. For a DC-DC converter with a switching frequency of $f_{SW} = 5\,\text{MHz}$, a 10-bit DPWM would require a $2^{10} f_{SW} = 5\,\text{GHz}$ system clock in a counter-comparator implementation or 2^{10} stages in a ring-oscillator implementation, which results in large dissipation and unacceptable die size. Thus, the hybrid DPWM is usually adopted in the digital DC-DC converters, which employs a ring-oscillator/counter structure [9, 10]. However, its system lock frequency is still much higher than the switching frequency, which limits the applications in the battery-powered devices such as mobile phones, PDAs and MP3 players.

In this paper, a 5 MHZ integrated digital DC-DC converter based on a

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0.5 μm standard CMOS process is presented. There is no extra high frequency clock needed in the converter. A self-calibration loop has been used in the delay-line ADC to reduce the sensitivity of the ADC to PVTL. A DPWM based on delay lock loop (DLL) employs a first-order Σ-Δ modulator to achieve an equivalent resolution of 10-bit.

The realization of the ADC, the DPWM and the PID controller will be presented in section 2 to section 4 respectively. The simulation results are addressed in section 5, and a conclusion is given in Section 6.

2 ADC design

The presented delay-line ADC with the self-calibration loop is shown in Fig. 2. When the ADC is working, there are two phases i.e. the calibrating phase and the normal phase.

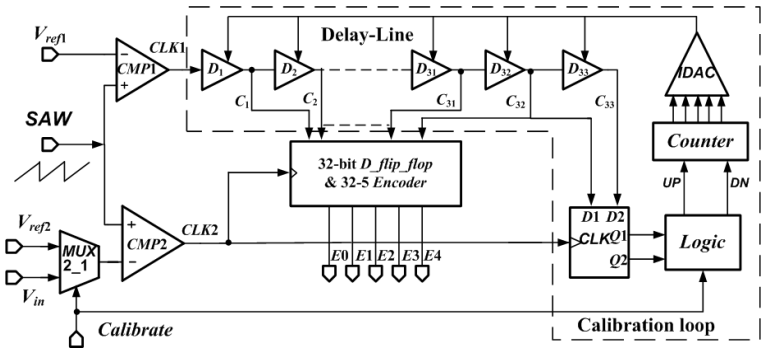

Fig. 2. Delay-line ADC with a self-calibration loop

During the calibrating phase, the reference voltage V_{ref2} is connected with the negative input of CMP2. SAW is compared with V_{ref1} and V_{ref2} as shown in Fig. 3. Assuming the slope of SAW is K_{SAW}, the delay time T_d between the rising edges of $CLK1$ and $CLK2$ is given by:

$$T_d = K_{SAW} \cdot (V_{ref2} - V_{ref1}) \tag{1}$$

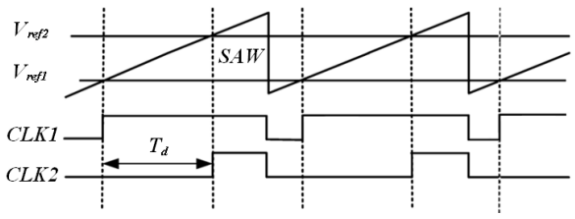

Fig. 3. Delay time of the delay-line

$D_1 \sim D_{33}$ are identical delay cells with adjustable delay time. The calibration loop is used to guarantee that the delay time of each delay cell is $T_d/32$. When the rising edge of $CLK2$ arrives, the states of C_{32} and C_{33} can indicate if the delay time is appropriate. As shown in Fig. 4, if both of

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C_{32} and C_{33} are high, it means that the delay time of each delay cell is too short. Thus, the counter counts down and the current offered to the delay cells would be decreased which leads to a longer delay time. Similarly, if C_{32} and C_{33} are low which means the delay time is too long, the calibration loop would increase the current to shorten the delay time. Only when C_{32} is high and C_{33} is low does the calibration be accomplished.

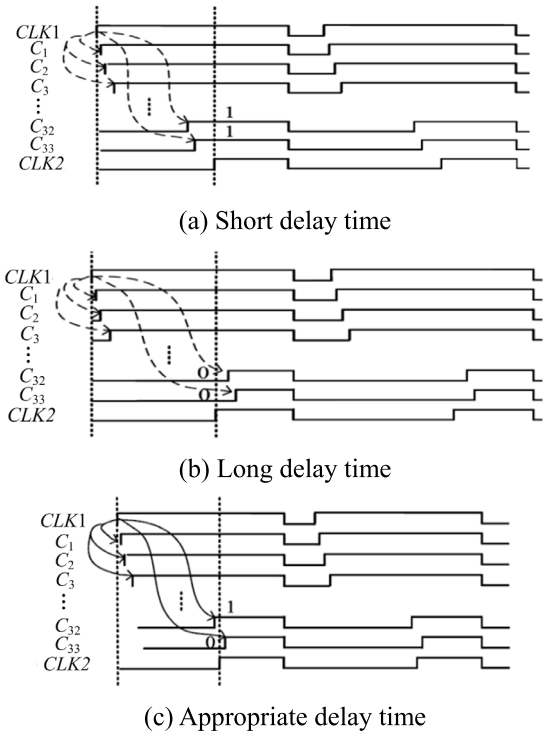

Fig. 4. Principle of the self-calibration loop

During the normal working phase of the ADC, V_{in} is connected to the negative input of CMP2. The calibration loop does not work and the delay time in each delay cell is constant. The states of $C_1 \sim C_{32}$ at the rising edge of $CLK2$ as shown in Fig. 5 can represent the error between V_{in} and V_{ref1}. By encoding $C_1 \sim C_{32}$ to binary code, the 5-bit digital code $E4 \sim E0$ is obtained.

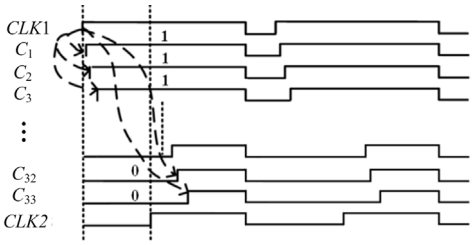

Fig. 5. Normal working phase

Based on the analysis of the presented delay-line ADC, it is seen that the dynamic range of the ADC is from V_{ref1} to V_{ref2} and the least significant bit

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(LSB) is given by:

$$LSB = \frac{V_{ref2} - V_{ref1}}{32} \tag{2}$$

According to Eq. (2), the LSB of the presented ADC is determined by V_{ref1} and V_{ref2} which could be design with low sensitivity to PVTL.

3 DPWM design

A high-resolution DPWM is presented in this section. It consists of a 5-bit core DPWM and a Σ-Δ modulator which improves the effective resolution of the core DPWM up to 10-bit. The block diagram of the first-order Σ-Δ modulator is illustrated in Fig. 6.

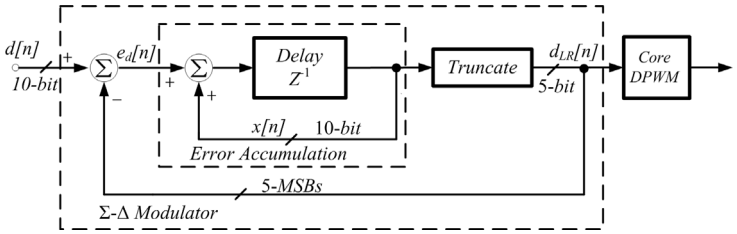

Fig. 6. Block diagram of the first-order Σ-Δ modulator

The essence of Σ-Δ modulator in DPWM is an error accumulation as Δ stands for the error and Σ represents the accumulation. According to the cumulative error, the core DPWM periodically changes its low-resolution output between two adjacent levels, so that the average value of the output slowly approaches the high resolution. For instance, to realize a duty cycle of 216/1024, the duty cycle of the core DPWM changes periodically as 6/32, 7/32, 7/32, 7/32, 6/32, 7/32, 7/32, 7/3, and the average value attains $216/1024 = 1/4 \cdot 6/32 + 3/4 \cdot 7/32$. The averaging is naturally performed with the filtering components of the power stage [11].

Fig. 7 shows the realization of the first-order Σ-Δ modulator. The error between the 10-bit high-resolution duty-cycle d[n] and the 5-bit low-resolution duty-cycle d_{LR}[n] is expressed as a 7-bit complementary code e[n]. At the beginning, the output of the modulator d_{LR}[4∼0] equals to d[9∼5], and the positive errors are accumulated in the 7-bit serial adder. When q[5] reahces one, the molator outputs d[9∼5]+1 so that the error turns to negative and the accumulation error begins to reduce. When the q[5] goes back to zero,

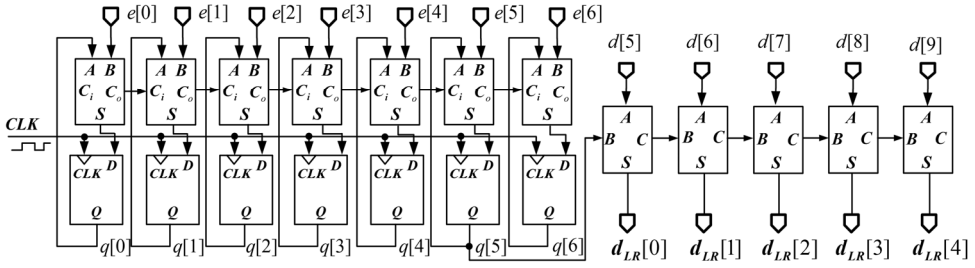

Fig. 7. Realization of the first order Σ-Δ modulator

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one cycle is finished. Thus, the low-resolution duty-cycle achieves a high equivalent resolution. In this application, the error accumulation q[n] is never less than zero i.e. the sign bit q[6] is always zero. To ensure the correct operation of the modulator under all circumstances, some extra logic circuits are essential.

Fig. 8 shows the core DPWM. The DLL in the core DPWM should be locked with a delay time from CLK_REF to C_{32} equaling to T, the period of CLK_REF. Thus, one of the signals C_1∼C_{32} would be chosen according to d_{LR}[n] to generate the rectangular wave. Comparing with the calibration loop in Fig. 2, the DLL in the core DPWM has demanding requirement for the delay-control. For the calibration loop in the ADC, there is no need to do some delay between the falling edges in each delay cell, because the desired delay time of the delay-line is much smaller than the switching period. The calibration loop can be locked correctly as long as the initial delay time is small than switching period. However, as for the DLL in the core DPWM, the falling edges in the delay-line can't be all settled at the end of the period without any delay, because the rising edge of C_{32} should be very close to the end of the switching period. The delay cell in the DPWM is shown in Fig. 9.

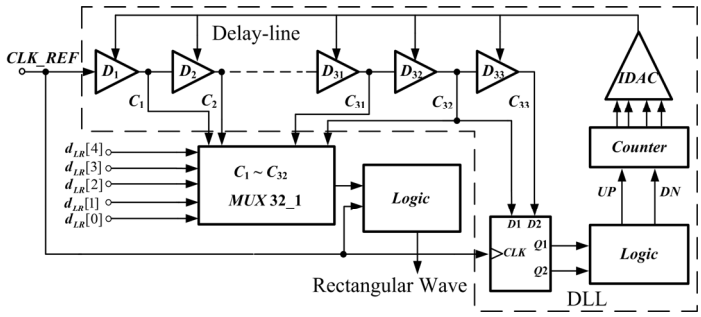

Fig. 8. Realization of the core PWM

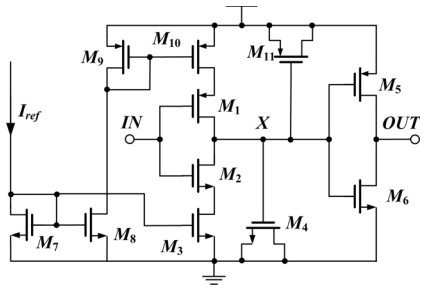

Fig. 9. Delay cell in the DPWM

Assuming the duty cycle of CLK_REF is 50%, the DLL may be incorrectly locked as shown in Fig. 10 (b). If the initial delay from CLK_REF to C_{32} is longer than the case A in Fig. 10 (c), the control loop finds C_{32} and C_{33} both high, deems the delay time still too short by mistake and locks with the delay time of $2T$. However, if the initial delay time is shorter than

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the case B, the loop would keep on shortening the delay time and never get locked. Thus, the allowable variable delay range of the DLL in the DPWM is from $T/2$ to $3T/2$. Thus, each delay cell should be designed carefully with a variable delay time from $T/64$ to $3T/64$.

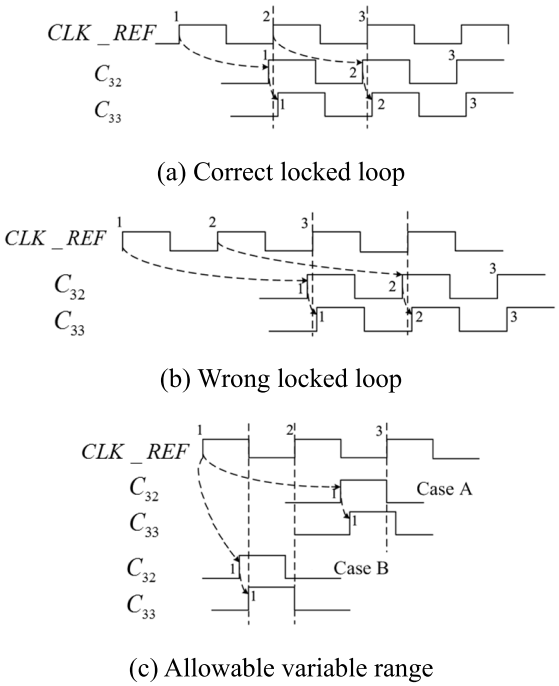

Fig. 10. Analysis of the locked delay time

However, if the current I_{ref} in Fig. 9 is constant, the delay time of each delay cell would vary with the supply voltage as the threshold of the inverter consisting of M_5 and M_6 is sensitive to the supply voltage. As a result, the DLL may be incorrectly locked. Thus, a current compensation circuit is designed to eliminate the influence of the supply voltage as shown in Fig. 11.

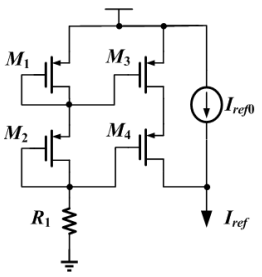

Fig. 11. Current compensation circuit

$M_1 \sim M_4$ constitute a current mirror with the ratio of 1:1. The I_{ref} can be given by:

$$I_{ref} = I_{ref0} + \frac{V_{dd} - V_{GS1} - V_{GS2}}{R_1} \tag{3}$$

Where I_{ref0} is adjustable and does not vary with the supply voltage. I_{ref} is used to charge and discharge the equivalent capacitor between X and

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ground C_X in Fig. 9. Thus, when the voltage of C_X arrives at the threshold of inverter V_H, the charge stored in C_X can be expressed as:

$$Q = I_{ref} \cdot t = \left(I_{ref0} - \frac{V_{GS1} + V_{GS2}}{R_1} + \frac{V_{dd}}{R_1} \right) \cdot t = \int_0^{V_H} C_X du \tag{4}$$

When the supply voltage changes ΔV_{dd}, V_H would change $\Delta V_{dd}/2$ if the M_5 and M_6 are well-matched. The variation of the V_{GS1} and V_{GS2} can be neglected if the aspect of the M_1 and M_2 is big enough. Thus, based on Eq. (4), we obtain

$$\frac{\Delta V_{dd}}{R_1} \cdot t = C_X \cdot \frac{\Delta V_{dd}}{2} \tag{5}$$

When the DLL is locked correctly, t = $T/32$. The R_1 is given by:

$$R_1 = \frac{T}{16 C_X} \tag{6}$$

4 Digital PID controller design

In this section, the bilinear transformation method has been applied to convert the transfer function of the PID controller from the discrete z domain to the continuous s domain, which facilitates using the bode diagram to analyze the stability of the digital DC-DC converter.

The digital PID compensation consists of a proportion term, an integration term and a differentiation term. The output of the PID controller in Fig. 1 can be given as

$$d[k+1] = K_p \cdot e[k] + K_d \cdot (e[k] - e[k-1]) + K_i \cdot di[k] \tag{7}$$

where

$$di[k] = di[k-1] + e[k] \tag{8}$$

$d[k]$, $e[k]$, $di[k]$ are the duty cycle, the error and the error accumulation at the k^{th} cycle respectively. K_p, K_d, K_i are the proportion coefficient, the differentiation coefficient and the integration coefficient respectively. Based on Eq. (7), $d[k]$ can be obtained as

$$d[k] = K_p \cdot e[k-1] + K_d \cdot (e[k-1] - e[k-2]) + K_i \cdot di[k-1] \tag{9}$$

Subtracting Eq. (9) from Eq. (7) leads to

$$\begin{aligned} d[k+1] = d[k] &+ K_p \cdot (e[k] - e[k-1]) \\ &+ K_i \cdot e[k] + K_d \cdot (e[k] + e[k-2] - 2e[k-1]) \end{aligned} \tag{10}$$

The block diagram of the PID controller is presented as shown in Fig. 12. K_p, K_d and K_i are all chosen to be 2^n, where n is a positive integer value, so that the multiplication in Eq. (10) can be performed simply by a shift operation.

According to Eq. (10), the transfer function of the PID controller can be derived as

$$G(z) = Z\left(\frac{d[k+1]}{e[k]} \right) = \frac{(K_p + K_d + K_i) - (K_p + 2K_d) z^{-1} + K_d z^{-2}}{1 - z^{-1}} \tag{11}$$

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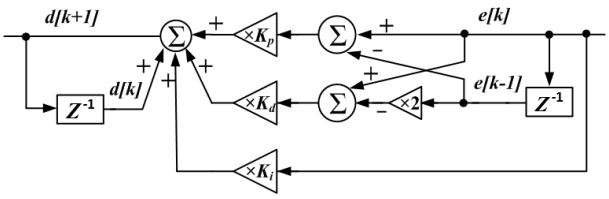

Fig. 12. PID controller based on shift operation

The bilinear transformation relation is expressed as Eq. (12) where T is the clock period of the discrete time.

$$z = \frac{1 + Ts/2}{1 - Ts/2} \tag{12}$$

Thus, the s-domain transfer function of the digital PID controller can be given by:

$$G(s) = \frac{2K_p + 4K_d + K_i}{2} \cdot \frac{\left(s^2 + \dfrac{4f_{SW}(K_p + K_i)}{2K_p + 4K_d + K_i}s + \dfrac{2f_{SW}^2 K_i}{2K_p + 4K_d + K_i}\right)}{s^2 + \dfrac{2}{T}s} \tag{13}$$

Based on Eq. (13), we can utilize the bode diagram to analyze and design the stability of the digital DC-DC.

5 Simulation results

The simulation results including the function blocks' simulation results and the whole chip simulation results would be represented in this section.

From the simulation result of the delay-line ADC shown in Fig. 13, the output $E4{\sim}E0$ step from 11111 down to 0001 responding to the input varying from 800 to 920 mV. The dynamic range of the delay-line ADC is from V_{ref1} to V_{ref2} i.e. 800 to 920 mV and the LSB of the delay-line ADC is $(920 - 800)/30 = 4$ mV. As the reference voltages V_{ref1} and V_{ref2} can be designed with low sensitivity to PVTL, the dynamic range and the LSB which are determined by V_{ref1} and V_{ref2} would also have low sensitivity to PVTL

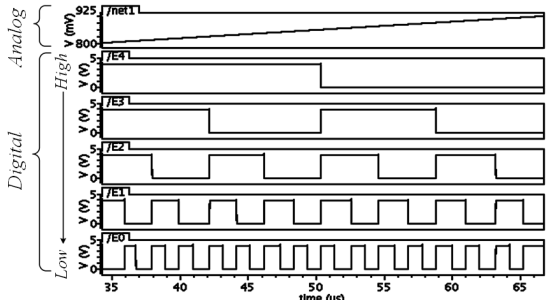

Fig. 13. Simulation result of the delay-line ADC

Fig. 14 represents the simulation result of the core DPWM and the first-order Σ-Δ Modulator. When the input duty cycle signal $d[9{\sim}0]$ from the PID

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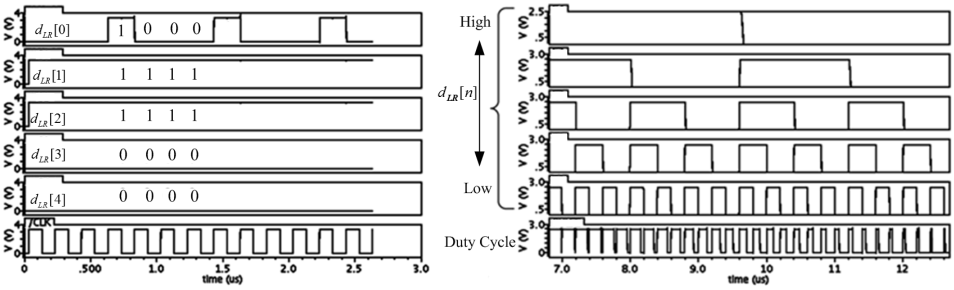
controller is 10'b0011001000, the 5-bit $d_{LR}[4\sim0]$ changes periodically between 5'b00111 and 5'b00110 to achieve the average duty cycle of 10'b0011001000 as shown in Fig. 14 (a). Fig. 14 (b) shows that the output of the core DPWM changes from full duty cycle to zero duty cycle when $d_{LR}[4\sim0]$ varies from 5'b11111 to 5'b00000.



(a) first-order Σ-Δ modulator (b) Core DPWM

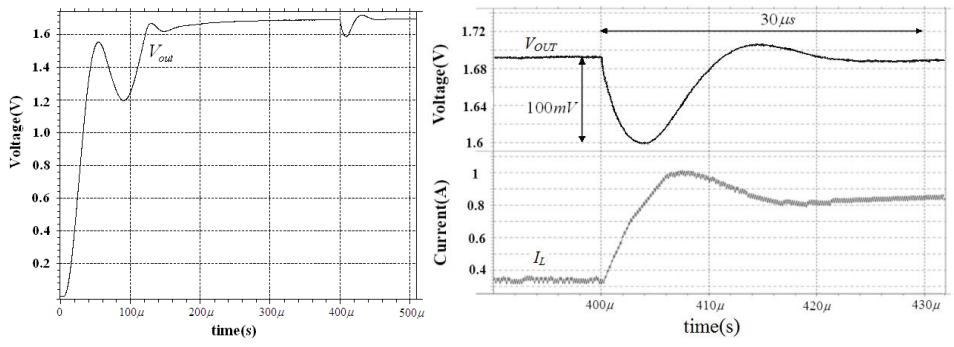
Fig. 14. Simulation result of the DPWM

A comparison of the DPWM performance with other previously published works is summarized in Table I. It is seen that the presented DPWM achieves a high resolution of 10-bit with low cost. Owing to the high resolution, the limitation of the LSB in the ADC caused the limit cycles [8] can be minimized. Thus, the line and load regulations which never exceed the LSB can be also minimized.

Table I. DPWM Performance comparison

	[12]	[13]	this work
Resolution	8-bit	8-bit	10-bit
Number of delay cells	32	16	32
Multiplexer	Two 16:1 Mux	Two 16:1 Mux	One 32:1 Mux

The whole chip simulation results are illustrated in Fig. 15, the performances of the presented converter is summarized in Table II and the efficiency curve is given in Fig. 16. The DC-DC converter can operate at the supply



(a) Start-up (b) Transient response

Fig. 15. Whole chip simulation results

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Table II. Performance summary

Technology	0.5μm CMOS	Inductor	4.7μH
Input voltage range	2.7~3.6V	capacitor	10μF
Output voltage range	1.7V	Output ripple	1.2mV
Current load Range	200~850mA	Line regulation	0.3%/V
Switching frequency	5MHz	Load regulation	0.4%/A
Transient response	30μs @500mA Load Step	Peak efficiency	94%

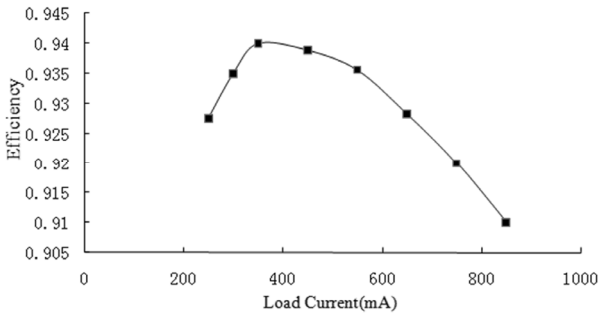

Fig. 16. Efficiency versus loading

voltage range of 2.7 to 3.6 V, start up within 250 μs and recover within 30 μs when the current load changes from 350 to 850 mA rapidly. The maximum efficiency is 94% under 350 mA loading. Table III shows the comparison table with prior arts. Our design features higher switching frequency and less transient response time.

Table III. Performance comparison

	[6]	[14]	[15]	[16]	this work
Technology	0.5μm CMOS	0.6μm CMOS	0.35μm CMOS	0.18μm CMOS	0.5μm CMOS
Input voltage range	5V	3.3V	3.6V	2.7~3.6V	2.7~3.6V
Output voltage range	2.7V	0.2~3V	1.8V	1.8V	1.7V
Max. loading	1A	N/A	N/A	400mA	850mA
Switching frequency	1MHz	500KHz	10MHz	1.65MHz	5MHz
Transient response time @ ΔI_{Load}	100μs @500mA	50μs @100mA	N/A	190μs @400mA	30μs @500mA
Peak efficiency	N/A	92%	85%	95.2%	94%

6 Conclusion

In this paper, a 5 MHZ integrated digital buck DC-DC converter with a delay-line ADC and a high-resolution DPWM is addressed, including the analysis, circuit implementation and simulation results. It is based on a 0.5 μm standard CMOS process. A self-calibration loop is utilized in the delay-line ADC to reduce the sensitivity to PVTL. The DPWM employs a first-order Σ-Δ modulator to achieve an equivalent resolution of 10-bit. Simulation results show that the digital DC-DC can operate at the supply voltage range of 2.7 to 3.6 V. The transient response time is less than 30 μs when the current load changes between 350 and 850 mA rapidly. The peak efficiency of the converter reaches 94%.

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