ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.5, 1–9

Area-efficient analog peripheral circuit techniques for Solid State Drive with NAND flash memories

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Abstract: This letter proposes area-efficient peripheral circuit techniques for 3D Solid State Drive (SSD) with NAND flash memories. We reduced charge pump stage using external high voltage of 12 V and 5 V, and improve target voltage accuracy using a cascode error amplifier of high voltage linear regulator. Also, we proposed fast transient response active mode VDC using NMOS pass element with external high voltage of 5 V.

Keywords: Solid State Drive (SSD), NAND flash memory, charge pump, boost converter, VDC

Classification: Integrated circuits

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DOI: 10.1587/elex.10.20130127
Received February 19, 2013
Accepted February 20, 2013
Published March 14, 2013

1 Introduction

Area-efficient technology for electronic devices has attracted much attention in recent years. An enterprise SSD for a data center is a future promising market of NAND flash memories [1]. The SSD based NAND flash memory has a speed, low-power operation, and size advantage over HDD. The typical SSD consists of more than sixteen NAND flash memories, DRAMs and a NAND controller. As the reduction of planar NAND feature cell size is almost limited, so TSV packaging, 3D NAND technology is upcoming key topic.

Also, a good strategy to decrease the power is lowering the external supply voltage, VCCE, from 3.3 to 1.8 V. Therefore, the charge-pump area more than doubles, which increases the NAND chip area by 5 to 10%. To overcome these problems, recently, many researchers have proposed various strategies to improve the area-efficient and power-efficient peripheral circuit of high voltage generator for 3D-SSD. Two main approaches have been proposed: Modifying the charge pump to improve the area-efficient and power-efficient [1, 2] and using the boost converter for area-efficient, power-efficient, and fast rising time performance [3, 4, 5].

We proposed the new scheme of the high voltage generator using external high voltage of 12 V and 5 V, and additionally we proposed fast transient response active mode VDC using NMOS pass element and external high voltage of 5 V.

2 Proposed scheme using external high voltage of 12 V and 5 V

2.1 Charge pump type high voltage generator using 12 V and 5 V

In the NAND flash memory, for each program, read, and erase operation, separated high voltage generators should be used. The conventional high voltage generators are a charge pump type.

Fig. 1 shows the proposed high-voltage generator circuit. It consists of a stage-controlled charge pump, a stage control circuit, an R/S latch type oscillator, switching regulator, and linear regulator. The output of high-voltage generator drives a selected wordline through a high voltage switch circuit during the program operation in NAND flash memory. The charge pump with a number of pump stages elevates a supplied voltage to a higher voltage, where the unit stage is composed of a stage capacitor and switching elements [1]. The R/S latch type oscillator generates periodic clock and drives stage capacitors in the charge pump. The switching regulators limit the pump output voltage to a required target voltage. The output from a

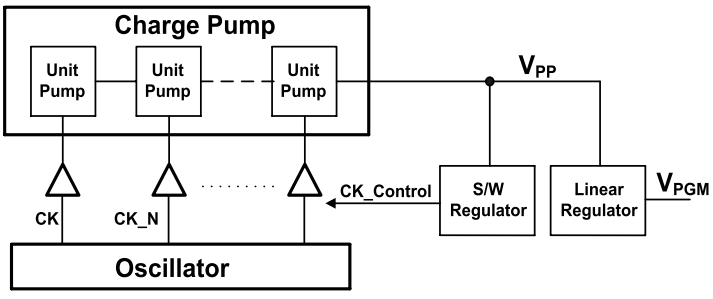

Fig. 1. Block diagram of a conventional high-voltage generation circuit.

DOI: 10.1587/elex.10.20130127
Received February 19, 2013
Accepted February 20, 2013
Published March 14, 2013

switching regulator becomes the input of a linear regulator. A switching regulator is composed of a resistive divider and a comparator, where the comparator detects whether the divided voltage is higher or not than a reference level and acts as on/off switch. Since the switching regulator switches the driving clock of the charge pump, the output ripple voltage is hard to avoid and it affects on a programmed cell distribution to be widen. So, to reduce the output ripple voltage high voltage linear regulator is used.

During the program operation, NAND flash memory requires highest maximum voltage of 30 V. Typically, the output voltage of the charge pump [1] can be expressed by

$$V_{PP} = (N+1) \times V_{G,MAX} - \frac{N \times I_{OUT,MAX}}{f \times (C_{PUMP} + C_S)} \quad (1)$$

where N is the number of stages, $V_{G,MAX}$ is maximum gain per unit pump stage, $I_{OUT,MAX}$ is output load current, f is clock frequency, C_{PUMP} is the stage pumping capacitance, and C_S is the parasitic capacitance in the pump stage.

A high-voltage generator can be modeled as shown in Fig. 2. The output voltage of charge pump can be expressed by a voltage source V_O, an equivalent resistance R_{PP}, and output load current I_{OUT}. Also, the output voltage of regulator can be expressed by $V_{PGM} = V_{PP} - I_{OUT} \cdot R_{REG}$ (2) where R_{REG} is the equivalent resistance of regulator.

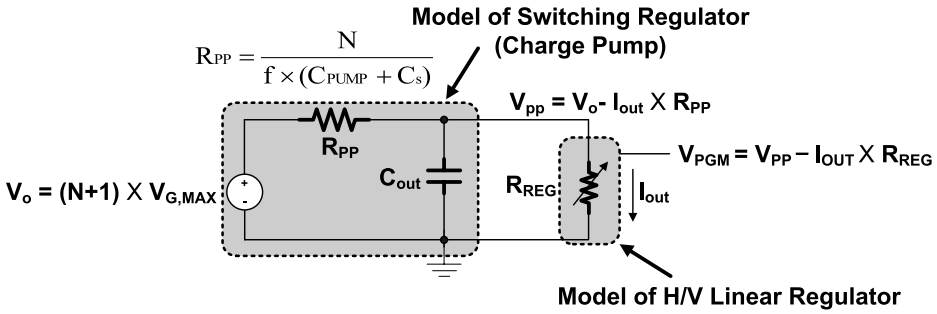

Fig. 2. Equivalent circuit model.

The output voltage of the program/erase charge pump has the highest maximum voltage, and the widest voltage ranges from 20 V to almost 30 V for program and erase operation. Conventionally, a pass charge pump (VPASS_PUMP) stage and program/erase charge pump (PE_PUMP) stage is connected in series, and the target output level of VPASS_PUMP is 12 V, and PE_PUMP pumping from the output of VPASS_PUMP [7].

We proposed a new charge pump scheme to reduce charge pump stage using external high voltage of 12 V and 5 V. Already 12 V and 5 V voltage level generated from the power supply as shown in Fig. 3. And the voltage level of 12 V is standard voltage that the main board need in the PC. From the power supply through the SATA power cable as shown in Fig. 3. Also, the single input multi-output (SIMO) boost converter [6] can be source of the external high voltage of 12 V and 5 V for the portable device. We can use external high voltage of 12 V instead of VPASS_PUMP to reduce the charge pump stage as shown in Fig. 3. The pumping clock voltage increases from VCCE of 3.3 V to external voltage of 5 V to improve the pumping voltage per one pumping cycle. Using an external voltage of 12 V and 5 V

DOI: 10.1587/elex.10.20130127
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< Power Supply 500 W > < SATA Power Cable >

AC INPUT	200~240 V~, 8A, 50/60Hz						
DC OUTPUT	+3.3V	+5V	+12 V1	+12 V2	+12 V3	-12V	+5Vsb
	20A	20A	19A	19A	19A	0.3A	2.5A
TOTAL POWER	110W		415W			3.6W	12.5W
	500W						

Fig. 3. Power Supply 500 W and SATA Power Cable.

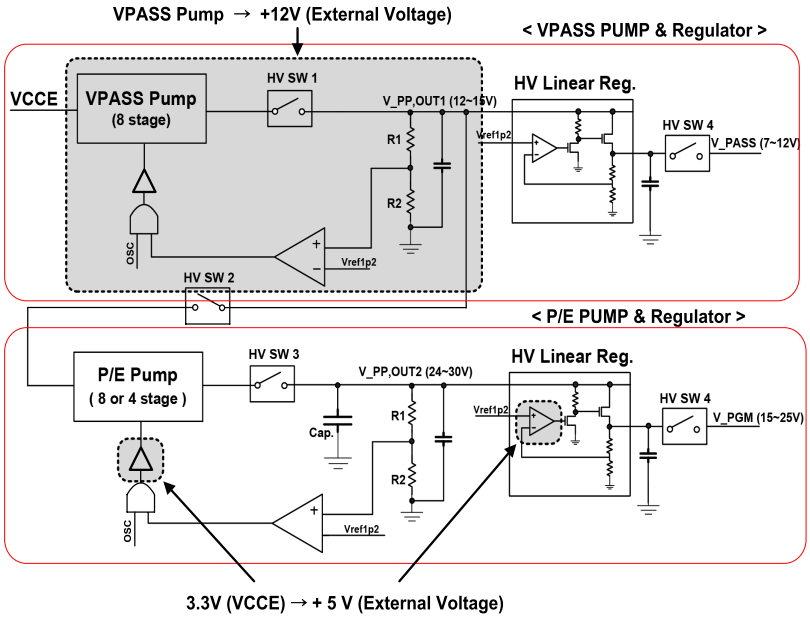

Fig. 4. Proposed high-voltage generation circuit.

improve the rising time to reach the target voltage of 30 V and reduce the peripheral chip size of the high voltage generator.

The simulation condition of clock period is 40 nsec (25 MHz), C_{PUMP} is 18 pF the maximum load current is 500 μA, and the output capacitor is 400 pF. As shown in Fig. 5 the pumping voltage increase from 31 mV to 102 mV per one pumping cycle. Using eq. (1), we activated number of 8 stage for generating 30 V with external voltage of 12 V and VCCE of 3.3 V. And we activated number of 5 stage for generating 30 V with external voltage of 12 V, 5 V and VCCE of 3.3 V. The number of stage is enough number of stage to generate the target voltage of 30 V considering PVT (Process, Voltage and Temperature) variation [1].

The comparison of the peripheral circuit performance are summarized in Table I. The number of stage in the Table I the activated number of stage could be controlled by the stage-controlled charge pump scheme [1, 2]. The external high voltage of 12 V is not available for the clock drivers due to the issue of breakdown voltage in the transfer transistor of charge pump, but clock voltage of 5 V is acceptable.

2.2 High linear regulator using external high voltage of 5 V

A high voltage linear regulator consists of a resistive divider, an error

DOI: 10.1587/elex.10.20130127
Received February 19, 2013
Accepted February 20, 2013
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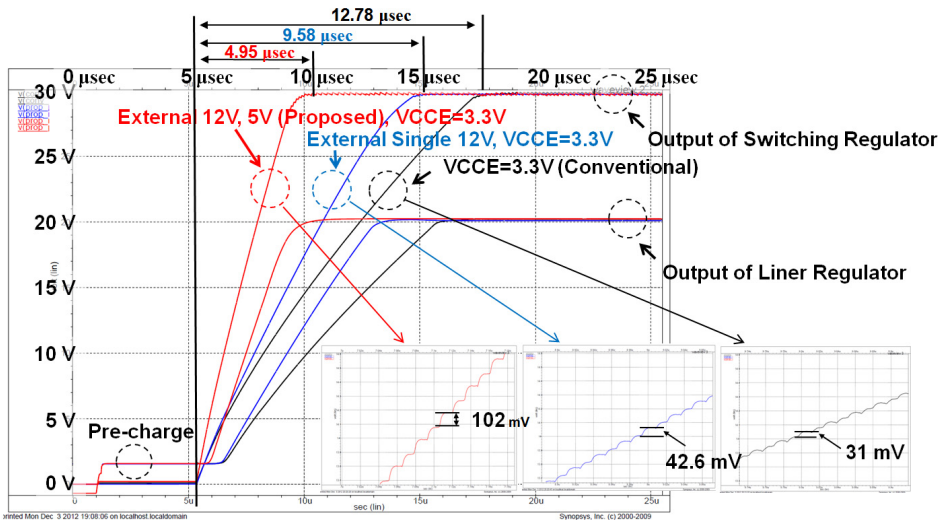
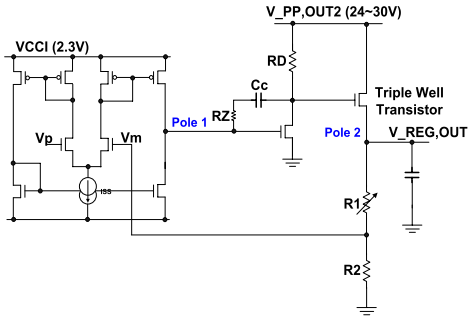


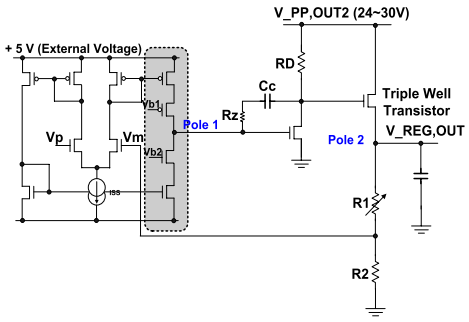
Fig. 5. Simulation result.

amplifier and a pass element as a NMOS or PMOS transistor. A PMOS transistor can easily achieve low drop output voltage, but NMOS has a better slew rate and load response characteristics. The circuit shown in Fig. 6 can be improved in terms of maximum output voltage by using triple well transistors in order to eliminate the body effect on the follower and low-V_{TH} transistors in order to reduce the voltage drop between gate and source due to the threshold voltage of the follower [7].

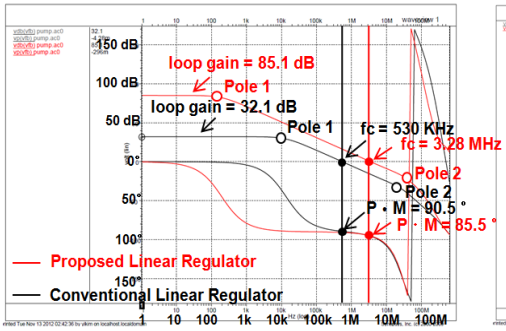
A voltage reference is used with the error amplifier to generate a regulated voltage, V_{REG}. If the voltage reference is stable, the fact that the V_{REG} is a function of a ratio of resistors, and the variation in the open loop gain of error amplifier is desensitized using feedback make the regulated



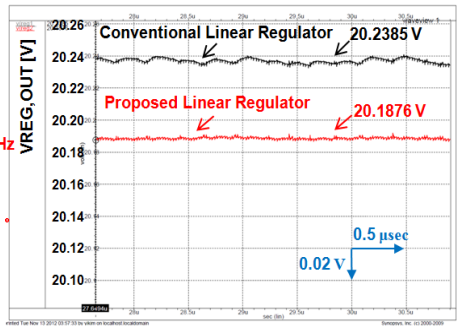
(a) Conventional H/V linear regulator



(b) Proposed H/V linear regulator



(c) AC simulation results



(d) Transient simulation results

Fig. 6. Proposed high voltage linear regulator and simulation results.

DOI: 10.1587/elex.10.20130127
Received February 19, 2013
Accepted February 20, 2013
Published March 14, 2013

voltage stable with process and temperature changes. The open-loop gain of error amplifier is finite, then we can write

$$V_{REG,OUT} = A_{OL} \times (V_p - V_m) \tag{3}$$

and

$$V_m = V_{REG,OUT} \times \frac{R_2}{R_1 + R_2} \text{ and } V_p = V_{REF} \tag{4}$$

Solving for the actual regulated voltage, gives

$$V_{REG,OUT} = V_{REF} \times \frac{1}{\frac{1}{A_{OL}} + \frac{R_2}{R_1+R_2}} \tag{5}$$

where A_{OL} is the open loop gain, V_p is the pulse input voltage, and V_m is the minus input voltage. The $V_{REG,OUT}$ of high voltage linear regulator can be calculated using equation (5), So the larger open loop gain can achieve a more accurate target voltage. To increase the loop gain, we proposed the cascode type operational amplifier using external high voltage of 5 V as supply voltage of operational amplifier. The simulated linear regulator condition of internal on-chip output capacitor is 14.4 pF, Rz is 4 KΩ, Cc is 5 pF, and a maximum output current of 500 μA. These results are loop gain of 53 dB and bandwidth of 2.7 MHz better than the results obtained without cascode stage under enough phase margin as shown in Fig. 6 (c).

2.3 Active mode VDC using external high voltage of 5 V

A PMOS common source stage has been used as a pass element in VDC regulators for its high voltage headroom. However, there are several disadvantages of using a PMOS pass element in an integrated regulator. First, the output pole is located at a relatively low frequency that leads to a complicated compensation scheme requiring a large external capacitor. Second, as a result of the low frequency dominant pole, the bandwidth of the system is reduced and the load regulation response tends to be slow. A third drawback of using PMOS transistor is that they have a smaller current driving capability than NMOS transistor resulting in a comparatively larger silicon area. On the other hand the use of an NMOS transistor as the pass element solves most of these problems. The NMOS transistor operates as source follower, thus the output pole is now located at higher frequency. This eliminates the need of an external capacitor and improves the load regulation. Additionally, the NMOS transistor requires a smaller silicon area to deliver the same amount of current. However, for an NMOS output stage to work, the output voltage needs to be lower than the gate voltage by a V_{GS} drop. As the technology scale down, the supply voltage levels are reduced, but the threshold voltage is not scaled at the same rate, thus leaving a low voltage headroom for this approach. A possible solution to this problem is to raise the gate voltage of the NMOS pass element above the supply voltage.

In previously proposed scheme we already use an external high voltage of 5 V for pumping clock signal, so we just use a external high voltage of 5 V as a supply voltage of operational amplifier to take a margin of V_{TH} for driving NMOS pass element.

The simulated active mode VDCs condition of internal on-chip output

DOI: 10.1587/elex.10.20130127
Received February 19, 2013
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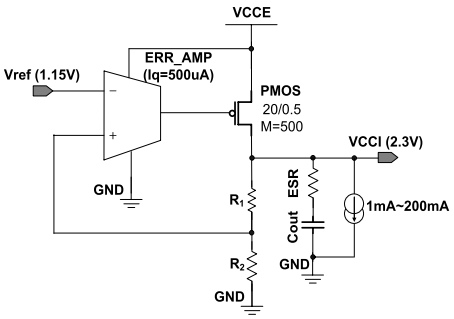
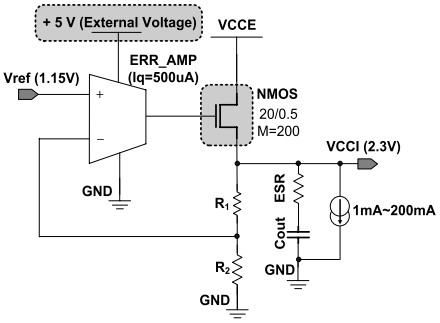
Published March 14, 2013

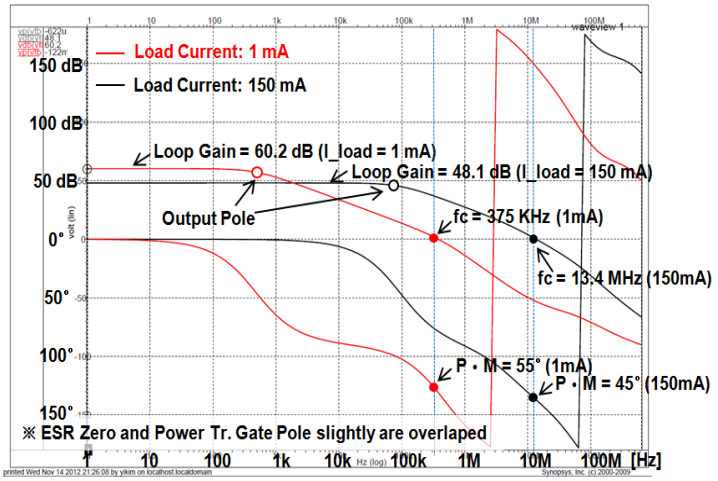
capacitor is 3.5 nF and the equivalent serial resistance (ESR) is 2.7 Ω, and a maximum output current of 150 mA. The proposed VDC operates with a VCCE ranging from 1.8 V to 3.8 V, external high voltage of 5 V. And the quiescent current of error amplifier is 500 μA. The VDC stability and its specifications are ensured for all of the process corners and over a temperature range of −30℃ to 100℃. The simulated open loop gain of proposed VDC is from 25.2 dB to 22.9 dB, the unit gain frequency is 6.8 MHz, to 27.9 MHz and the phase margin is from 55° to 62° for a load current variation from 1 mA to 150 mA as shown in Fig. 7 (d). In the simulated load-transient response, a maximum undershoot of 0.34 V and a settling time of 410 nsec are observed with the proposed VDC with NMOS for a load current variation from 1 mA to 150 mA at a rise time of 10 nsec.



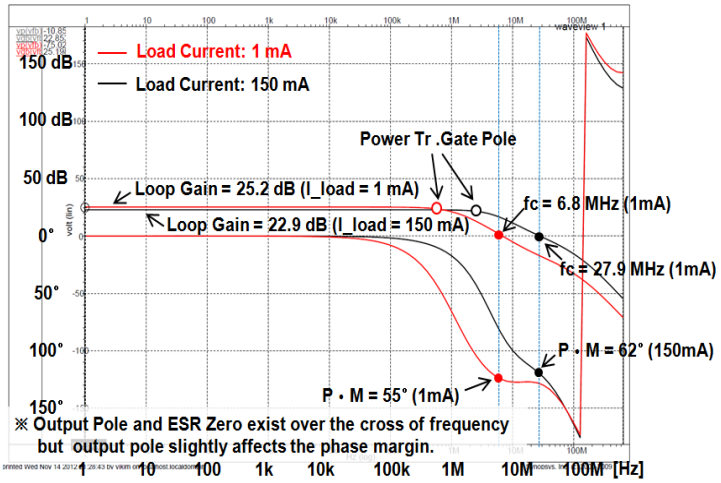
(a) Conventional VDC



(b) Proposed VDC



(c) AC simulation result of Conventional VDC



(d) AC simulation result of Proposed VDC

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Received February 19, 2013
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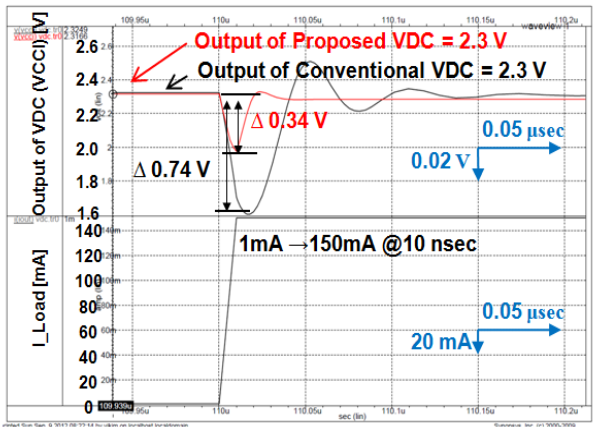
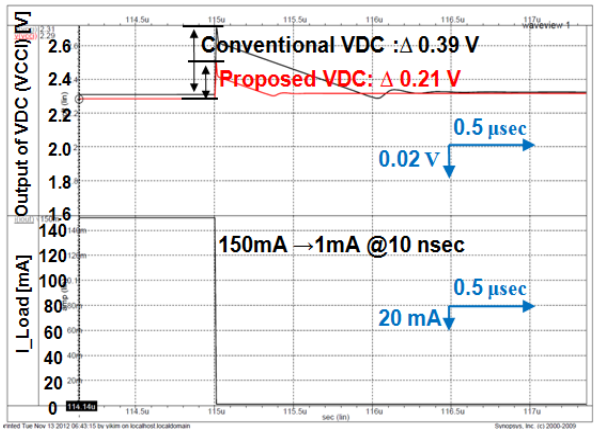


(e) Transient simulation result from 1 mA to 150 mA at a rise time of 10 nsec



(f) Transient simulation result from 150 mA to 1 mA at a failing time of 10 nsec

Fig. 7. Simulation Result.

These results are 400 mV better than the results obtained conventional VDC as shown in Fig. 7 (e).

The important parameters and a comparison of the peripheral circuit performance are summarized in Table I. The data show that the proposed circuit with external 12 V and 5 V has advantages in terms of its die size and analogue characteristic. Of particular importance is the fact that using additional external 5 V is improve the pumping voltage per one pumping cycle and rising time by using source of pumping clock. Moreover, the analogue characteristic of high voltage liner regulator, and active VDC is improved by using additional external 5 V as shown in Table I.

Table I. Comparison of the performances.

External Voltage	Charge Pump			Linear Reg.	Active VDC		
	Stage	Pumping Gain[mV]	Rising Time [µs]	DC Loop Gain [dB]	Pass Element (Size)	Unit Gain Freq. [Hz] (1m/150mA)	Peak Drop Voltage [V]
VCCE = 3.3V (Conventional)	16 or 24	31.0	12.78	32.1	PMOS (500/0.5 m=500)	375K / 13.4M	0.74
External 12V, VCCE = 3.3V	8	42.6	9.58	32.1	PMOS (500/0.5 m=500)	375K / 13.4M	0.74
External 12V/5V, VCCE = 3.3V	**5**	**102**	**4.93**	**85.1**	**NMOS (500/0.5 m=200)**	**6.8M / 27.9 M**	**0.34**

DOI: 10.1587/elex.10.20130127
Received February 19, 2013
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3 Conclusion

An area-efficient analog peripheral circuit technique for SSD with NAND flash memories was proposed in this letter. We can use external high voltage of 12 V instead of VPASS_PUMP to reduce the physical layout size of charge pump stage, and pumping clock voltage increase from VCCE of 3.3 V to external voltage of 5 V for improving the pumping voltage per one pumping cycle. We can achieve a more accurate target voltage when we get the larger open loop gain. Therefore, to increase the loop gain we proposed the cascode type operational amplifier using external high voltage of 5 V as supply voltage of operational amplifier. Also, the use of an NMOS transistor as the pass element with external high voltage of 5 V improve transient load response characteristic.

Acknowledgments

This work was supported by 'BK21', 'IDEC' and 'SK HYNIX'.

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Received February 19, 2013
Accepted February 20, 2013
Published March 14, 2013