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A CMOS OTA with extremely large DC open-loop voltage gain

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Abstract: The DC open-loop voltage Gain is a very important specification for amplifiers. In order to increase this specification, in this paper, we have proposed an improved folded cascode gain boosted amplifier (improved FCGBA) which has extremely large DC open-loop voltage gain. Compared to traditional FCGBA, this novel structure needs only one auxiliary amplifier, so it is energy saving. Finally, with SMIC 0.18 μm CMOS process of 1.8 V supply and Hspice simulator, a corresponding amplifier with a capacitor load of 1.6 pF is designed. Its voltage gain is 153 dB; unit gain bandwidth is 1.91 GHz; phase margin is 64°; 0.01% settling time is 2.36 ns; and the power dissipation is only 12.9 mW. This result confirms the validity of this new structure.

Keywords: CMOS OTA, amplifier, gain boosted

Classification: Integrated circuits

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1 Introduction

Operational transconductance amplifiers are usually fundamental blocks in analog circuits. And their DC Open-loop voltage gain A_{v0} is a very important specification. Traditionally, for obtaining higher A_{v0}, much more power dissipation and area have to be spent. If we can greatly increase voltage gain without deteriorating other specifications (such as power dissipation, unit gain bandwidth, phase margin, and so on), it will be rather satisfactory. On the other hand, although some papers [1, 2, 3] published in recent years

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have given new ways to improve voltage gain, the effectiveness is limited. So, learning from these papers, a new amplifier is proposed in this paper to get extremely large voltage gain with other specifications also favorable.

2 Principle of the amplifier

The schematic of this improved FCGBA is shown in Fig. 1. As we see, this differential amplifier is based on traditional gain boosted amplifier. However, there is only one auxiliary amplifier, and the other auxiliary amplifier has been replaced by transistors M13 to M18. For illustrating the function of these extra transistors, let us consider the single ended equivalent circuit of this improved FCGBA, shown in Fig. 2. As is obvious in this figure, if we calculate its output resistance (the input port is connected to ac ground, and an ac signal ΔV is applied to the output port), there is a current of i1 flowing into the circuit. Besides, because of the current mirror constituted by M16, M18, M12, and an Inverter, there is another current of i2 flowing out of the

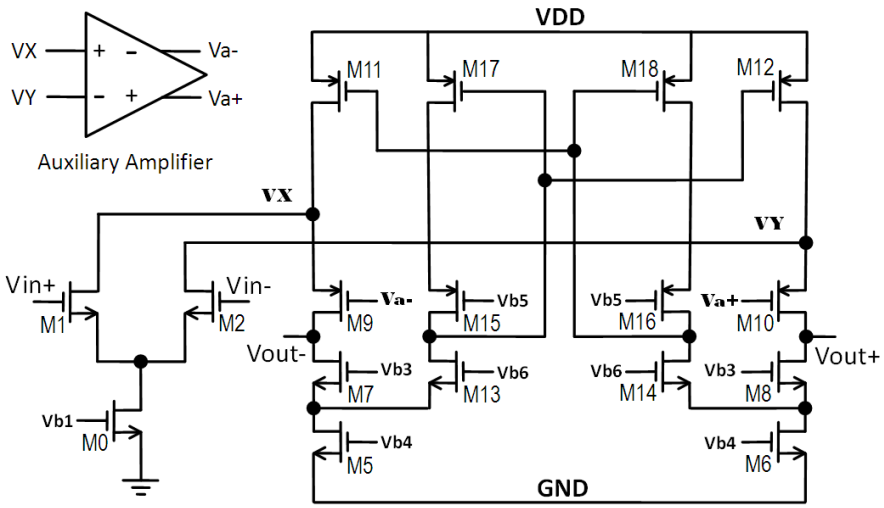

Fig. 1. Schematic of the Improved FCGBA

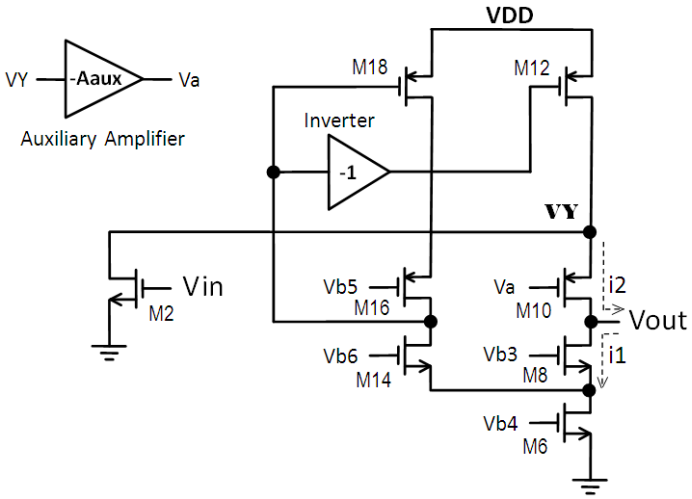

Fig. 2. Single Ended Equivalent Circuit of the Improved FCGBA

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circuit. As long as i1 equals i2, then the output resistance will be infinite, which can in turn provide infinite voltage gain. For working properly, the following inequality should be satisfied:

$$i_2 \leq i_1 \tag{1}$$

Note that the infinite output resistance does not deteriorate the frequency characteristic. In fact, the closer i2 approaches to i1, the larger the output resistance will be, which just pushes the first pole to the original point while increasing the zero-frequency gain, but do not change other characteristics (such as the product of Av0 and −3 dB bandwidth, the second pole, phase margin, unit-gain bandwidth, etc.).

As for thermal noise, let us consider the equivalent circuit of Fig. 2. When this amplifier has very large voltage gain and is working properly, it can be proved that g_{m12} is approximately equal to g_{m18}, and that the input-referred thermal noise voltage is as follows:

$$\overline{V_{n,in}^2} \approx \frac{4kT}{g_{m2}^2} \cdot (\gamma_2 \cdot g_{m2} + \gamma_{12} \cdot g_{m12} + \gamma_{18} \cdot g_{m18}) \tag{2}$$

That is to say, M2, M12, and M18 (in Fig. 2) contribute to the most of the thermal noise.

It should be noted that Fig. 2 is only an equivalent circuit of Fig. 1, and that the Inverter in Fig. 1 is omitted by cross-connection.

3 Transfer function of the amplifier

The dc gain of the equivalent circuit of Fig. 2 is shown below:

$$A_{v0\_equ} = -\frac{g_{m2}}{\frac{1}{R_3} + \frac{1}{R_5} - \frac{1}{R_3} \cdot \frac{r_{o6}}{R_2 + r_{o6}} \cdot R_1 \cdot g_{m12} \cdot \left(1 - \frac{r_{o10}}{R_5}\right)} \tag{3}$$

$$R_1 = \frac{1}{g_{m18} + \frac{-g_{m18} + \frac{1}{r_{o16}}}{g_{m16} + \frac{1}{r_{o16}} + \frac{1}{r_{o18}}} \cdot \frac{1}{r_{o18}}} \tag{4}$$

$$R_2 = \frac{R_1 + r_{o14}}{g_{m14} \cdot r_{o14} + 1} \tag{5}$$

$$R_3 = [1 + g_{m8} \cdot r_{o8}] \cdot (R_2 // r_{o6}) + r_{o8} \tag{6}$$

$$R_5 = [g_{m10} \cdot r_{o10} \cdot (A_{aux} + 1) + 1] \cdot (r_{o2} // r_{o12}) + r_{o10} \tag{7}$$

where A_{v0_equ} is the dc gain of the equivalent circuit of Fig. 2, A_{aux} is the dc gain of the auxiliary amplifier.

In order to get the transfer function of the amplifier in Fig. 1, we should analyze the poles at first. Let us consider how this amplifier is designed. To begin with, we should design a traditional differential folded cascode amplifier (named the first amplifier), whose ac performance is shown as the dotted line in Fig. 3; and then, we should add two auxiliary amplifiers and change the first amplifier to be a traditional differential folded cascode gain boosted

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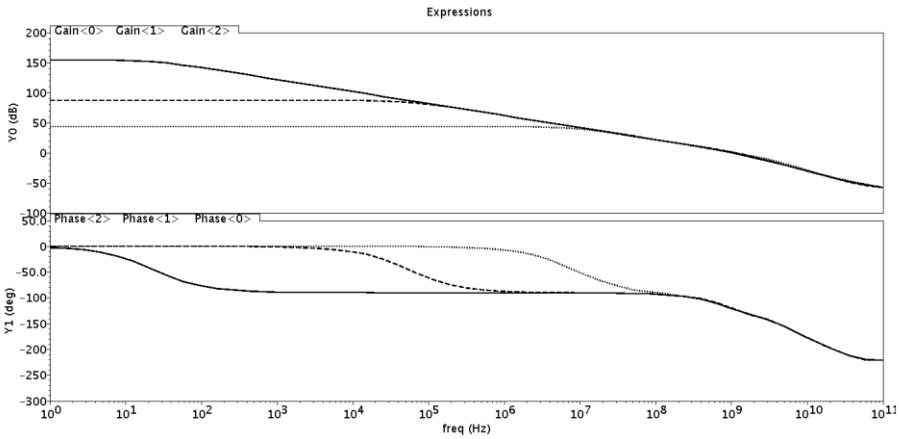

Fig. 3. The ac performance of the designed three amplifiers

amplifier (named the second amplifier), so its ac performance becomes to be the dashed line in Fig. 3; finally, we should delete the N auxiliary amplifier and change the second amplifier to be an improved FCGBA (named the third amplifier) as shown in Fig. 1, and hence its ac performance turns into the solid line in Fig. 3. Observing Fig. 3, we can find that, from the first amplifier to the third amplifier, the second pole does not change, and that the first pole changes with the dc gain. So, we can get the transfer function of the third amplifier (the improved FCGBA):

$$\begin{aligned} A_v(s) &\approx \frac{A_{v0}}{\left(1+\frac{s}{\omega_{p1}}\right)\cdot\left(1+\frac{s}{\omega_{p2}}\right)} \\ &= \frac{A_{v0}}{\left(1+\frac{s\cdot A_{v0}}{\omega_{p1\_first}\cdot A_{v0\_first}}\right)\cdot\left(1+\frac{s}{\omega_{p2\_first}}\right)} \end{aligned} \tag{8}$$

where A_{vo} is the dc gain of the third amplifier, ω_{p1} is the first pole of the third amplifier, ω_{p2} is the second pole of the third amplifier, A_{vo_first} is the dc gain of the first amplifier, ω_{p1_first} is the first pole of the first amplifier, ω_{p2_first} is the second pole of the first amplifier.

4 Problem and countermeasure

The problem is that the improved FCGBA (shown in Fig. 1) is susceptible to the variation of process and temperature. When process and temperature changes, the zero-frequency voltage gain and −3 dB bandwidth of the amplifier will also change accordingly, but the other characteristics (the product of Av0 and −3 dB bandwidth, the second pole, phase margin, unit-gain bandwidth and so on) will not change. Fortunately, as long as we regulate the bias voltage of Vb4 in Fig. 1, the voltage gain can revert to its original extremely large value. In fact, the optimal value of Vb4 (this optimal value is called Vtg) depends on process and temperature. When Vb4 = Vtg, infinite voltage gain will occur. If Vb4 ≥ Vtg, then the amplifier can operate properly; if Vb4 < Vtg, then the amplifier will go wrong and the output resistance will

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be negative. When Vb4 ≥ Vtg, we can find that the closer Vb4 approaches to Vtg, the larger the voltage gain will be. So the challenge is how to regulate Vb4 to get a large enough voltage gain.

As a result, we have devised a regulation circuitry shown in Fig. 4. This regulation circuitry can generate and regulate the voltage of Vb4 for the improved FCGBA in Fig. 1. And this regulation circuitry is devised for the process of 1.8 V power supply, where the Vtg can be approximately 530 mV and the threshold voltage of a diode is approximately 700 mV. As can be seen in Fig. 4, Vb4 is provided by the voltage across the capacitor C_bias.

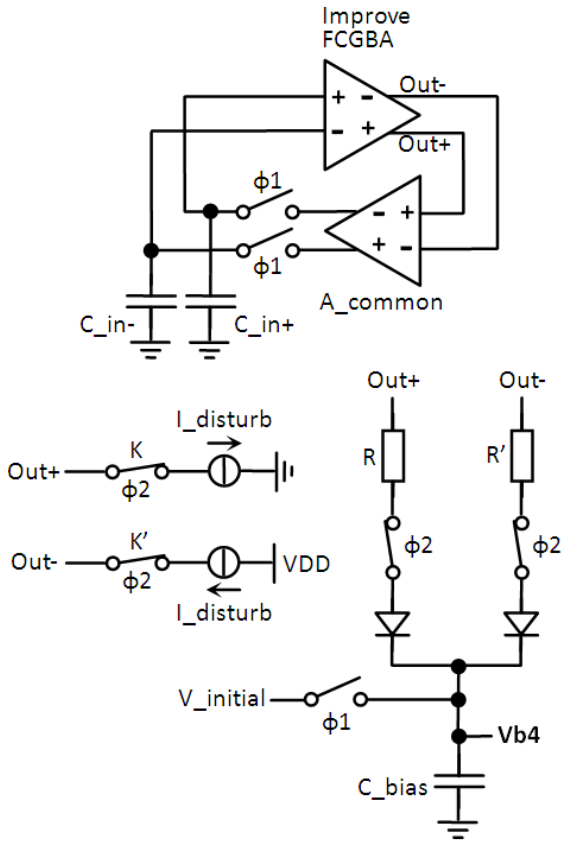

Fig. 4. Regulation Circuitry for the Improved FCGBA

In Fig. 4, there is a common amplifier called A_common. When we are using this regulation circuitry to generate and regulate Vb4, the regulation process can be as follows. In phase 1, C_bias is charged by V_initial, which is smaller than Vtg; and the offset voltage of the improved FCGBA is stored on C_in+ and C_in−, making the output voltage difference of the improved FCGBA to be zero. In phase 2, C_bias is indirectly connected to the two output ports of the improved FCGBA; and the current of I_disturb disturbs the two output ports (Out+ and Out−) of the improved FCGBA and cause a voltage difference between them. Because Vb4 is smaller than Vtg now, so the voltage difference between Out+ and Out− increase quickly to be very large, and because the common mode voltage of Out+ and Out− is about 900 mV, so one of the two diodes turns on to charge the capacitor C_bias and

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make Vb4 increase. When Vb4 is quite close to Vtg but still smaller than Vtg, the voltage difference between Out+ and Out− decreases to be small very fast, so the currents on the two diodes become very small, making the charge rate of C_bias very slow. After some time, the Vb4 is slightly larger than Vtg, which is a result we want. At this moment, the regulation process is over, so we can turn off all the switches in Fig. 4, and measure the value of Vb4 from out of the chip.

After the measurement, we can provide a fixed Vb4 from out of the chip for the improved FCGBA, so as to make the improved FCGBA work with extremely large voltage gain.

Notice that, for generating Vb4 appropriately, C_bias should be a large capacitor and the values of the two resistors R and R' should also be large, but the current of I_disturb should be small.

Besides, in Fig. 1, it should be mentioned that the change of the input common mode voltage may cause Vb4 < Vtg, which can make this amplifier to be a positive feedback latch. In fact, the variation of the input common mode voltage causes the variation of the current on M0, and in turn causes the variation of the output common mode voltage, which can cause Vb4 < Vtg and produce the positive feedback latch. For overcoming this problem, in Fig. 1, we should use an ordinary CMFB circuit which uses the common mode voltage of the two output ports to generate Vb1; and we should make M0 to be a long channel device, so the channel-modulation effect can be reduced. Thus, when the input common mode voltage changes, the CMFB circuit will make the current on M0 do not change, by regulating the voltage of Vb1; therefore, Vb4 < Vtg will not occur and the positive feedback latch will not come into being either. Empirically, in CMOS process of 1.8 V supply, by using this method, the input common mode voltage can change as large as 100 mV without having negative effects.

Finally, we will talk about device mismatch. In fact, device mismatch can also cause Vb4 < Vtg, which will make the output resistance to be negative, as has been described. However, as long as we use common-centroid layout, a precise matching can be obtained, where the typical three-sigma offset voltage is less than 1 mV. Having this kind of matching and using the regulation circuitry of Fig. 4 to regulate Vb4, we can ensure the proper polarity of the output resistance, and there will be no obvious influence on the extremely large voltage gain.

5 Simulation results

Based on the new structure in Fig. 1 and with SMIC 0.18 μm CMOS process of 1.8 V supply, we have designed and simulated an improved FCGBA using Hspice under 27°C. This amplifier has a capacitor load of 1.6 pF and a common feedback circuit which generates the voltage of Vb1 (shown in Fig. 1). There is also a common mode feedback circuit in the P auxiliary amplifier. As a result, the ac performance of the designed improved FCGBA is shown in Fig. 5 where the voltage gain is 153 dB, the bandwidth is 1.91 GHz, and

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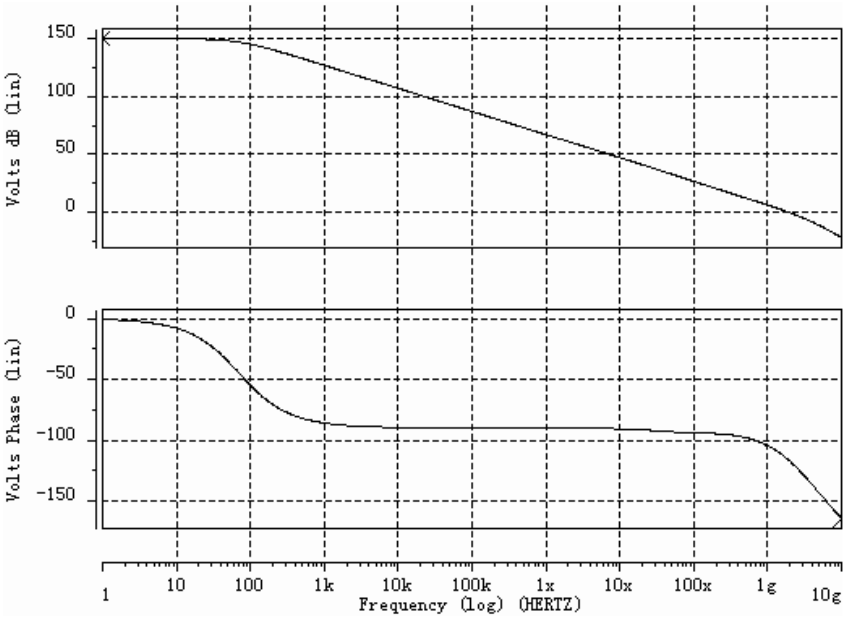

Fig. 5. The ac performance of the designed improved FCGBA

Table I. The ac performance under different process corners

Process Corner	Vtg (mV)	Voltage Gain (dB)	Phase Margin (^{o})	Bandwidth (Hz)
TT	533.7	153	64	1.91G
FF	520.1	149	62	2.02G
SS	550	155	65	1.86G
SNFP	543.7	150	61.5	1.89G
FNSP	526.3	150.5	65.2	1.95G

the phase margin is 64°. Its 0.01% settling time is 2.36 ns. It is noticeable that the power dissipation is only 12.9 mW.

After using the regulation circuitry to generate and regulate Vb4, Table I shows the ac performance of this designed amplifier under different process corners. Obviously, this result is rather satisfactory.

6 Conclusions

We have proposed an amplifier called improved FCGBA. After adjusting one of the bias voltages, this amplifier can have extremely large voltage gain, and without much power dissipation. Finally, an amplifier is designed as an example, demonstrating the validity of this new structure.

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