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LETTER

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A 1.2 V high conversion gain mixer with reused gm stage in 65 nm CMOS

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Abstract: A 1.2 V high conversion gain mixer which reuses the gm stage of the mixer as RF and IF amplifying stage is proposed in this paper. The gm stage of the proposed mixer converts the input RF voltage into current and also amplifies the down-converted IF signal. A high-pass network and a low-pass network are used in the mixer to block the RF signal and IF signal respectively in order to guarantee frequency stability. This mixer was designed and fabricated in 65 nm CMOS process. The measured IIP3 and DSB NF are −16 dBm and 13.5 dB respectively. A high conversion gain of 30 dB is achieved with the power consumption of 3 mW under a 1.2 V supply voltage.

Keywords: RF, mixer, reusing, low power

Classification: Integrated circuits

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1 Introduction

The growing demand for low cost and low power CMOS RF transceivers in the application of GPS, Wireless Body Sensor Networks and RFIDs encourages the researches on low-power and ultra-low-power RF circuit design techniques. Low power techniques such as current reusing have undergone development for several years [1, 2, 3]. Using the current sharing structure, the power consumption can be reduced significantly. However, the decoupling capacitor must be large enough to avoid cross talk between

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the stacked modules. Furthermore, the minimum supply voltage and the maximum voltage swing are restricted because of the stacked structure. In this letter, a novel mixer realizing low power consumption in receiving front-end is proposed. It makes the gm stage being used by both input RF and down-converted IF signals. The gm stage in the proposed mixer also acts as a cascading IF amplifier.

Fig. 1 illustrates the principle of the proposed returning mixer compared with a traditional down-converted mixer along with a following IF amplifier. A traditional down-converted mixer often composes of a gm stage, a mixing core and a low-pass filtering output stage. The gm stage converts the input RF voltage into current which is to be commutated by the mixing core. The low-pass filtering stage filters out the up-converted outcomes while letting pass the down-converted signal. The down-converted signal is then be amplified by a following IF amplifier. For the proposed returning mixer, the gm stage converts the RF input voltage into current, then the RF current feed into the mixing core through a high-pass filter. A low-pass network filters out the up-conversion product while retaining the down-converted IF signal. The IF signal returns to the gm stage and be amplified by the gm stage. The high pass filter prevents the amplified IF signal from feeding into the mixing core. An output low-pass filter is connected at the output of the gm stage, picking up the clean IF signal while isolating the RF signals. Since the proposed mixer can provide IF gain without the extra power consumption of a separated IF amplifier, a higher power efficiency are achieved compared with the traditional structure.

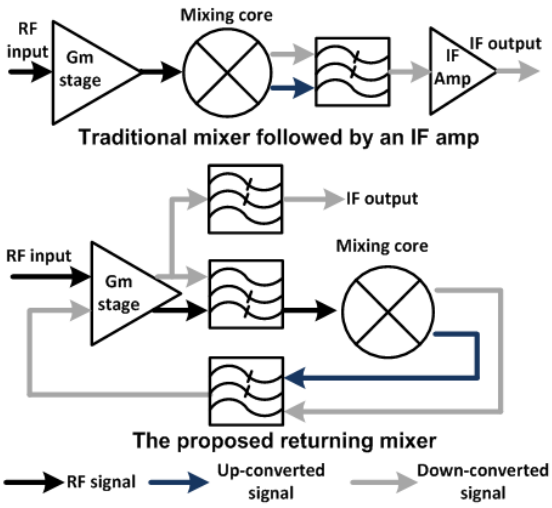

Fig. 1. The principle of the proposed returning mixer compared with a traditional mixer

2 Circuit design of the proposed mixer

Fig. 2 shows the circuit schematic of the proposed mixer. The CMOS transconductance stage is formed by NM0, PM0, NM1 and PM3. The input RF voltage signal is AC coupled into the gate of the gm transistors through C0, C1, C2 and C3. Capacitance C4 and C5 couple the RF currents into the mixing core and block out the IF signals, acting as a high-pass filter. The mixing core formed by PM4-PM7, commutates the RF current and

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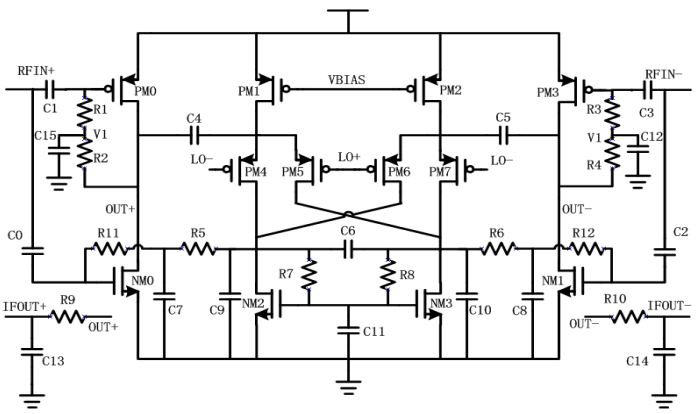

Fig. 2. Circuit schematic of the proposed mixer

produces the down-converted and up-converted signals. The load resistor R7 and R8 is also used as the common mode feedback circuits with NM2 and NM3. A low-pass filtering network made by R5-R6 and C6-C10 is connected between the output of the mixing core and the gate of NM0 and NM1. Finally, a low-pass filtering network formed by R9, R10, C13 and C14 is connected at the drain of NM0 and NM1 to separate the IF signal which has been amplified by the gm stage.

The double-balanced switching pair is biased by the current source PM1 and PM2. For DC current, NM2 and NM3 can be regarded as diode-connected and form a current mirror with NM0 and NM1 of the gm stage. PM0 and PM1 of the gm stage are biased by a self-adapted structure with large resistors connected between the gate and drain as shown in Fig. 1. To make the bias voltage of PM0 and PM3 stable under low output frequency, the common terminal of R1, R2 and the common terminal of R3, R4 are tied together, acting as a common mode feedback circuit. In order to keep the loop gain below 0 dB at any frequency point, the value of RF coupling capacitor C4 and C5 is chosen as 1 pF. The cut-off frequency of the low-pass filtering network connected between the output of the mixing core and the gm stage are set to be a little higher than the output IF frequency.

Fig. 3. shows the simulated loop gain versus frequency within the proposed mixer. The loop gain is below −40 dB at both low frequencies and high frequencies. At a medium frequency of 10 MHz, the loop gain reaches the peak value of −7 dB which is also in the safety range. So the circuit is stable at any frequency point.

The conversion gain of the proposed mixer is indicated by eq.(1). The input node is at the gate terminal of NM0, NM1, PM0 and PM3. The positive output node is at the common terminal of C13 and R9. The

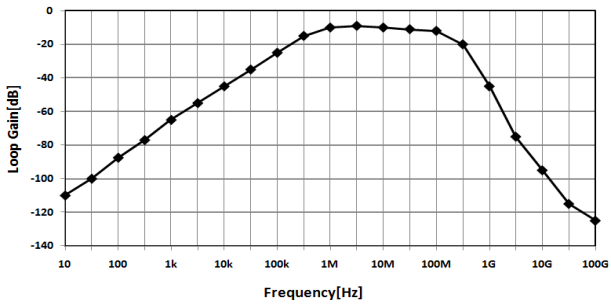

Fig. 3. Simulated Loop gain versus frequency within the proposed mixer

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negative output node is at the common terminal of C14 and R10. From this expression it is shown that NM0 (NM1) provide both RF and IF gain. Eq.(1) also indicates that, since both NM0 (NM1) and PM0 (PM3) contributes to the conversion gain, the bias current in the gm stage can be reduced to save the power consumption.

$$A_{CG} = \frac{2}{\pi} \cdot \left(\frac{r_{op0} \parallel r_{on0}}{\frac{1}{j\omega_{RF}C_4} + \frac{1}{g_{m4}} + r_{op0} \parallel r_{on0}} \right) \cdot (g_{mn0} + g_{mp0}) \cdot \frac{R_7}{1 + j\omega_{IF}(2C_6 + C_4)} \cdot \frac{1}{1 + j\omega_{IF}R_5C_7} \cdot g_{mn0} \cdot \frac{(r_{op0} \parallel r_{on0})}{1 + j\omega_{IF}R_9C_{13}} \tag{1}$$

If the IF output is at the drains of NM0 and NM1 without the returning path, the proposed mixer becomes a traditional folded mixer. The output node is now at the drain terminals of NM2 and NM3. The expression of the conversion gain is indicated by eq.(2).

$$A_{CGWO} = \frac{2}{\pi} \cdot \left(\frac{r_{op0} \parallel r_{on0}}{\frac{1}{j\omega_{RF}C_4} + \frac{1}{g_{m4}} + r_{op0} \parallel r_{on0}} \right) \cdot (g_{mn0} + g_{mp0}) \cdot \frac{R_7}{1 + j\omega_{IF}(2C_6 + C_4)} \tag{2}$$

As eq.(2) and eq.(1) indicates, with the help of NM0 (NM1) for providing the IF gain, the proposed mixer can obtain an additional IF gain as indicated in eq.(3), with no extra dc current be consumed. Thus the gain budget of the following modules is compressed. One or more stages can be removed from the following IF amplifier chain, saving the power consumption of those IF amplifiers.

$$A_{CGADD} = g_{mn0} \cdot \frac{(r_{op0} \parallel r_{on0})}{1 + j\omega_{IF}R_9C_{13}} \tag{3}$$

3 Measurement results and analysis

The proposed mixer is designed and fabricated in SMIC 65 nm RFCMOS process with 1.2 V supply voltage, and the die area is 0.032 mm^2. The layout and the die photography of the proposed mixer are shown in Fig. 4 (a) and (b) respectively. The overall DC bias Current is 2.5 mA. Fig. 5 shows the measurements of CG and IIP3 versus input frequency from 1 GHz to 2 GHz with a fixed output IF frequency of 2 MHz. The CG at 1 GHz is 30 dB; this value drops by 1.5 dB to around 28 dB at 2 GHz. The measured IIP3 results versus input frequency only fluctuate a little in the frequency band from 1 GHz to 2 GHz. The peak IIP3 is −15 dBm, measured at 1 GHz while the lowest IIP3 is −16.5 dBm measured at 1.7 GHz.

The performance comparison with other reported mixers is shown in Table I. The advantages of the proposed mixer are embodied in the high conversion gain, the low power consumption and moderate NF and OIP3. Because of the large conversion gain of the proposed mixer, the IIP3 is a little bit lower than the other reported mixers.

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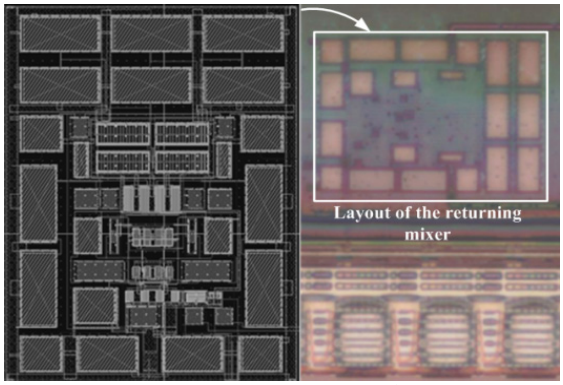

a *b*

Fig. 4. (a) Layout and (b) Photography of the proposed mixer

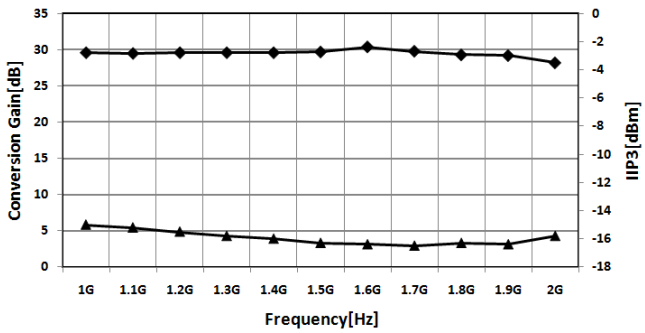

Fig. 5. Measured conversion gain and IIP3 versus frequency

Table I. Performance comparison of the proposed mixer with other reported works

	[4]	[5]	[6]	[7]	This work
Frequency (GHz)	2.4	5	0.9-3.7	0.5-3	1-2
Supply voltage (V)	1.8	1	1.2	1.5	1.2
Conversion Gain (dB)	17.5	4.5	14	9.5	30
IIP3 (dBm)	-12	-6	-10	10	-16
OIP3 (dBm)	5.5	-1.5	4	19.5	13.8
NF (dB)	10.5	13	6.5	16.5	13.5
Power (mW)	18	3.8	16.8	5.25	3.6

4 Conclusions

This paper proposes a high conversion gain mixer with reused RF and IF gm (transconductance) stage. Thanks to the returning structure, both RF gain and IF gain can be obtained in the mixer and resulting in high conversion gain of 30 dB with the power consumption of 3 mW under a 1.2 V supply voltage. This mixer structure shows promising application in low-power, low-cost WSN RF transceivers.

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