

RTS noise reduction of CMOS image sensors using amplifier-selection pixels

Mohd Amrallah Mustafa^{1a)2}, Min-Woong Seo³, Shoji Kawahito³, Keita Yasutomi³, and Kiichiro Kagawa³

¹ Graduate School of Science and Technology, Shizuoka University,
3–5–1 Johoku Hamamatsu 432–8011, Japan

² Department of Electrical & Electronic, Universiti Putra Malaysia,
43400 UPM Serdang, Selangor, Malaysia

³ Research Institute of Electronics, Shizuoka University,
3–5–1 Johoku Hamamatsu 432–8011, Japan

a) kawahito@idl.rie.shizuoka.ac.jp

Abstract: This paper describes a RTS (random telegraph signal) noise reduction technique for an active pixel CMOS image sensor (CIS) with in-pixel selectable dual source-follower amplifiers. In this CMOS image sensor, the lower-noise transistor in each pixel is selected in the readout operation using a table of determining the lower-noise transistors of all the pixels. A prototype image sensor with 65×290 pixels for demonstrating the effectiveness of this technique has been implemented using $0.18 \mu\text{m}$ CMOS image sensor technology with pinned photodiode option. The measured result shows that the maximum noise using the amplifier-selection technique is reduced to 9.6e- from 17.2e- which is the maximum noise of the image array using one of two amplifiers in each pixel without selection.

Keywords: active-pixel CMOS image sensor, amplifier-selection pixel, correlated multiple sampling, noise reduction, $1/f$ noise, RTS noise

Classification: Integrated circuits

References

- [1] P. P. K. Lee, R. C. Gee, R. M. Gidash, T. H. Lee and E. R. Fossum: Proc. IEEE Workshop CMOS and Advanced Image Sensors (1995) 84.
- [2] A. Krymski, N. Khaliullin and H. Rhodes: Proc. IEEE Workshop CCD and Advanced Image Sensors (2003) 1.
- [3] S. Suh, S. Itoh, S. Aoyama and S. Kawahito: Sensors **10** (2010) 9452.
- [4] K. Findlater, J. Vaillant, D. Baxter, C. Augier, D. Herault, J. Hurwitz, L. Grant and J-M. Volle: Proc. SPIE **5251** (2004) 187.
- [5] S. Kawahito and N. Kawai: Proc. Int. Image Sensors Workshop (2007) 226.
- [6] M. A. Mustafa, S. Itoh and S. Kawahito: J. Automation, Mobile Robotics & Intelligent Systems **3** (2009) 202.
- [7] M. W. Seo, S. H. Suh, T. Iida, T. Takasawa, K. Isobe, T. Watanabe, S. Itoh, K. Yasutomi and S. Kawahito: IEEE J. Solid-State Circuits **47** (2012) 272.
- [8] N. Kawai and S. Kawahito: IEICE Electron. Express **2** (2005) 379.
- [9] K. Mabuchi, N. Nakamura, E. Funatsu, T. Abe, T. Umeda, T. Hoshino, R.

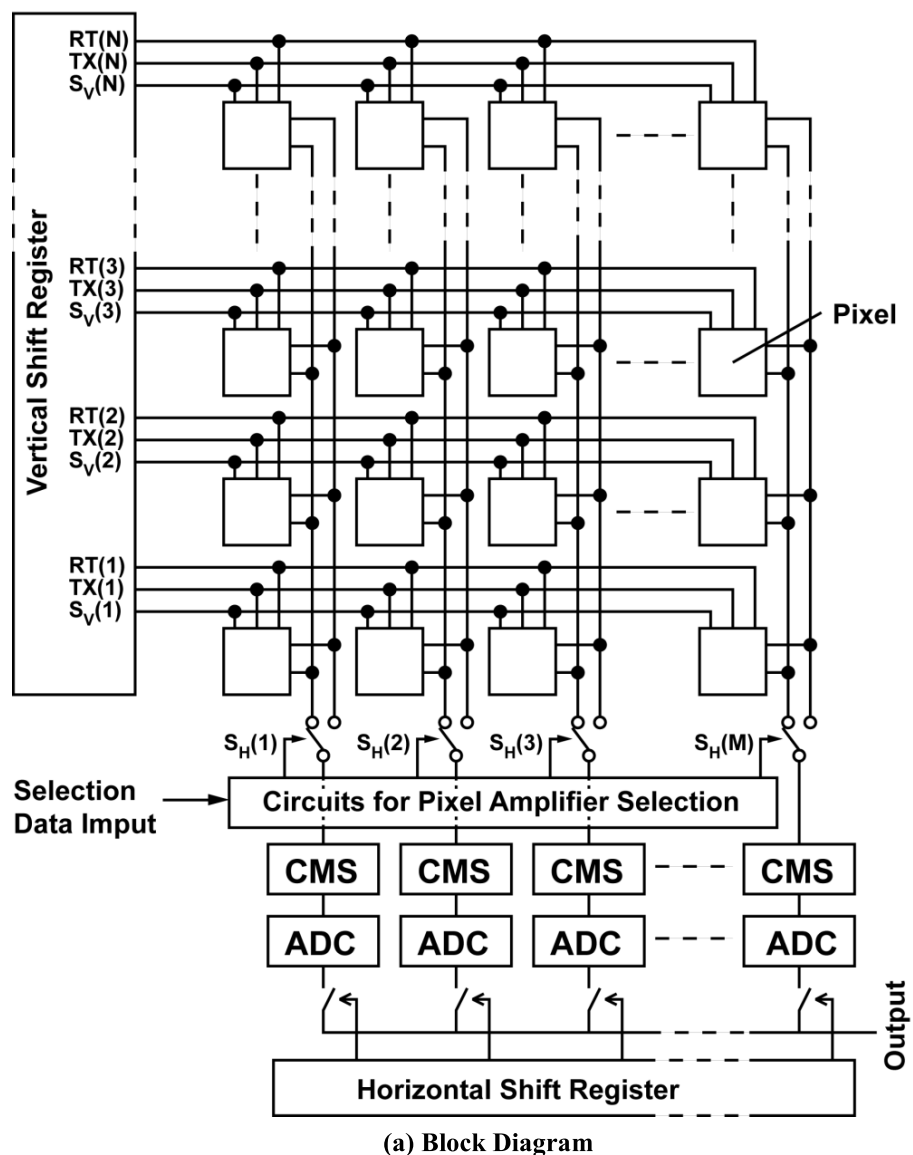
1 Introduction

Temporal random noise of active pixel CMOS image sensors has been drastically reduced by the introduction of pinned photo diodes and column analog processing [1, 2]. A column parallel processing for noise reduction, so-called correlated multiple sampling (CMS) has a great effect for pixel amplifier noise particularly for thermal noise [3]. However, such an analog signal processing is not always effective for reducing the random telegraph signal (RTS) noise of the in-pixel source-follower amplifier. The noise amplitude of the active pixels deviates from pixel to pixel and some pixels have very large noise level due to the RTS noise when compared to the mean noise level of the entire image array though the population of such very large RTS noise is very small [4]. A RTS noise reduction technique using a temporal histogram of the RTS noise has been reported [5, 6]. However, this method requires complicated column parallel digital processing circuits and may not be suitable for cost-effective implementation of the image sensors.

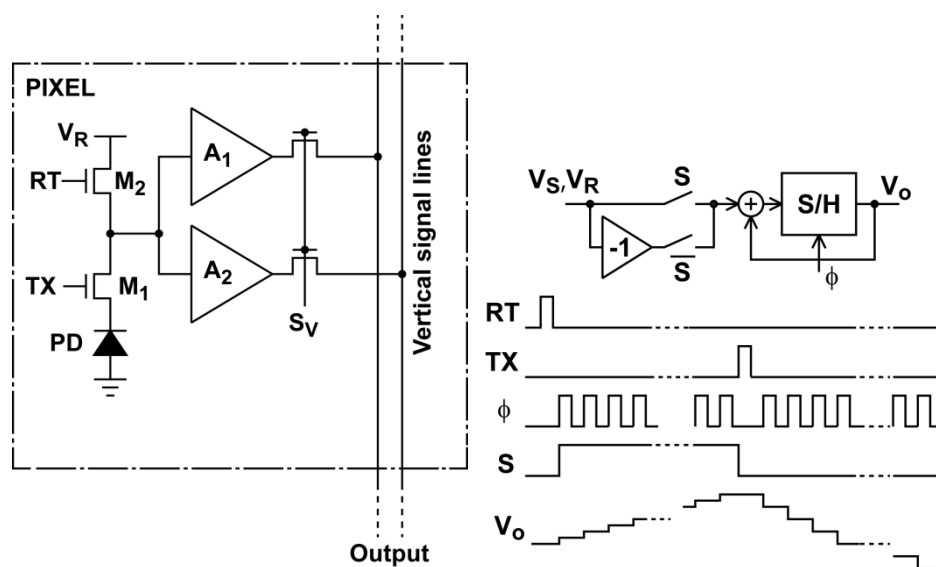
This paper proposes a technique for reducing the noise of large RTS noise pixels in CMOS image sensors. Each pixel has selectable two source-follower amplifiers. Because the population of large RTS noise pixels is very small, the probability that the two amplifiers in each pixel simultaneously have large RTS noise is very small because the distribution of large RTS noise transistors is random in space. Based on this fact, the proposed pixel has a function of selecting a lower-noise amplifier from two amplifiers in the pixel for readout operation. To do this, a one-bit memory per column for amplifier selection is used and data for the amplifier selection is uploaded just before the readout operation for every row of pixel signals. To reduce the possible noise increase by connecting two source follower amplifiers to charge detection node, a technique for inactivating the unused amplifier is also introduced. An experimental CMOS image sensor chip has been implemented and the effectiveness of the proposed technique for reducing the population of the large noise pixels has been demonstrated.

2 Architecture and operation

Fig. 1(a) shows the block diagram of the CMOS image sensor using the amplifier-selection technique. As shown in Fig. 1(b), each pixel is based on an active pixel sensor with a pinned photodiode [1]. The readout operation of the pixel is controlled by TX for charge transfer, RT for resetting the charge detection node, and S_V for row selection of the pixels. The photo charge transferred to the charge detection node can be read out using one of two readout amplifiers, A_1 and A_2 . The two amplifiers may have different noise amplitude mainly due to the $1/f$ noise and RTS noise. Once the image sensor is implemented, the mean noise level of the amplifiers due to the $1/f$ noise and RTS noise is fixed. Therefore, if we have prior knowledge on the mean noise level of the two amplifiers, the lower-noise amplifier can be selected during the readout operation of each pixel for realizing a low-noise



(a) Block Diagram



(b) Pixel Schematic

(c) Correlated Multiple Sampling (CMS) Circuits

Fig. 1. (a) Architecture of the CMOS image sensor with amplifier-selection pixels.

image sensor. To do this, the mean noise levels of the amplifiers, A_1 and A_2 of all the pixels are measured beforehand and a table of one bit per pixel for selecting a lower-noise amplifier for all the pixels is created in an external system. The selection data of the j -th row of the table are uploaded to the image sensor just before reading the j -th row signals.

For the readout operation, column-parallel correlated multiple sampling (CMS) circuits for pixel noise reduction and column cyclic ADCs for digital signal readouts are used [7]. Fig. 1(c) shows a block diagram and operation timing diagram of the CMS circuits. Both the reset and photo-signal levels are sampled for M times and summated the sampled signals in an analog integrator. The multiple sampling for the photo-signal levels is done by different polarity from that for the reset levels. Then the final integrator output V_O is expressed as

$$V_O = \sum_{i=1}^M (V_R(i) - V_S(i)) \quad (1)$$

where $V_R(i)$ and $V_S(i)$ are the reset and photo-signal levels of the i -th sample, respectively. This operation has a gain of M for both reset and signal levels and this large gain of M and averaging effect of the integration has a great noise reduction effect to the pixel source follower, particularly for thermal noise [3]. The CMS has a better noise reduction effect to $1/f$ noise than that of correlated double sampling (CDS) [8]. Using the CMS, the thermal and $1/f$ noise can be sufficiently smaller than the RTS noise. As a result, the noise of large-noise pixels is dominated by the RTS noise.

The pixel circuit for actual implementation with the selectable dual amplifiers is shown in Fig. 2(a). An amplifier sharing technique is used for the actual implementation of the pixels [9], i.e., two pixels share one charge detection node, hence the reset transistor M_3 and the two source-follower amplifiers for selection are shared by the two pixels. The readout timing diagram is shown in Fig. 2(c). To read out j -th row signals, amplifier-selection data $D_{AS}(j, i)$, $i=1, \dots, N_H$, are uploaded and stored in a shift register in the sensor chip. The stored data are used for controlling the switch transistors, M_{10} and M_{11} in the column to select the lower-noise amplifier in the amplifier-selection pixel. Then the pixel outputs for the reset and photo-signal levels are read out using multiple sampling in the column CMS circuits. Because of the amplifier sharing in two pixels, photo-charges in PD1 and PD2 are read out sequentially by TX1 and TX2, respectively.

In this amplifier-selection pixels, two transistors, M_6 and M_9 are also used for inactivating the unused amplifier and therefore reducing the extra-noise due to the positive feedback effect of the unused source follower amplifier. To explain this effect, a low-frequency equivalent circuit of the pixel source follower is shown in Fig. 2(b). The noise of MOS transistors which appears at the source follower output is fed back to the input through C_{GS} and the resulting low-frequency gain to the noise source, $G_n = v_{FD}/v_n$ is approximately given by

$$G_n = \frac{\beta_F}{1 - \beta_F + g_o/g_m} \quad (2)$$

where g_o and g_m are, respectively, the output conductance and the transconductance, measured at the source of M_4 or M_7 and β_F is the positive

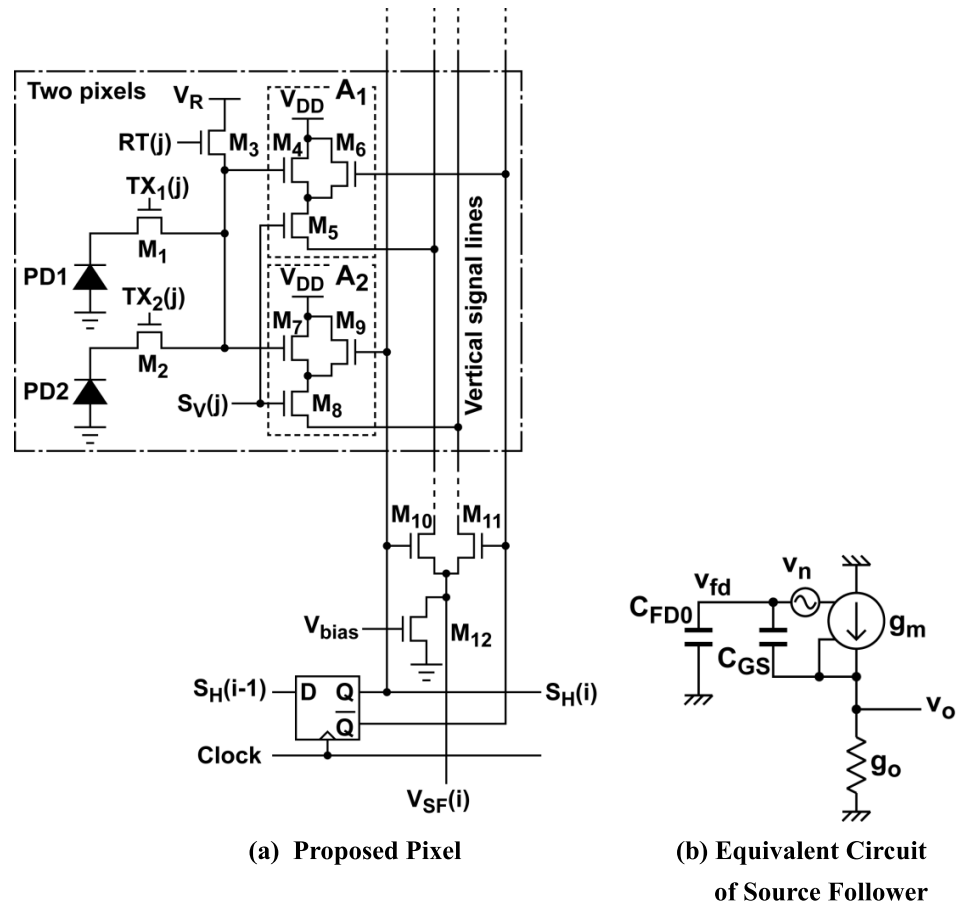


Fig. 2. Amplifier-Selection Pixel Circuits and Operation Timing.

feedback factor of the source follower given by $C_{GS}/(C_{FD0}+C_{GS})$ where C_{GS} is the gate-to-source capacitance and C_{FD0} is the other capacitance at the floating diffusion node. If the amplifier A_1 is selected, M_{10} is turned on and M_{11} is turned off. Then the source terminal of M_7 becomes high impedance and both g_o and g_m of M_7 become very small, but their orders are comparable. For instance, if $g_o = g_m$ and $\beta_F = 0.5$, then $G_n = 1/3$. Therefore, the noise of the unused amplifier A_2 is superimposed on the signal in

addition to the noise due to the used amplifier A_1 . This effect may become a noise penalty of the amplifier-selection pixels. In order to eliminate this effect, transistors M_6 or M_9 are used. If the amplifier A_1 is selected, the transistor M_9 is turned on and the source terminal of M_7 becomes low impedance, which is equivalent to g_o to be very large compared to g_m and the resulting low-frequency gain to the noise source calculated by Eq. (2) becomes very small. This makes the noise of the unused amplifier A_2 to be uninfluenced.

3 Implementation and measurement results

In order to demonstrate the noise reduction effect of the amplifier-selection pixels, a prototype image sensor chip has been implemented and measured. A $0.18\text{ }\mu\text{m}$ CMOS image sensor technology with pinned photodiode option is used for the implementation. The prototype includes a unit array of $65(\text{H}) \times 290(\text{V})$ pixels each of which has a size of $7.5\text{ }\mu\text{m}(\text{H}) \times 15\text{ }\mu\text{m}(\text{V})$ for two shared pixels. The gain of the CMS circuits can be controlled in the range of 1 through 128 by changing the number of samplings. Fig. 3 shows noise distribution in the pixel array for three cases of reading the signal with the amplifier A_1 only, the amplifier A_2 only and the amplifier selected from A_1 and A_2 . The CMS gain is set to 16 ($M=16$). In order to reduce the influence of dark current noise, TX gates are always closed during the measurement. In Fig. 3, the cumulative probability (CP) of noise as a function of the r.m.s. (root mean square) noise is plotted. The amplifier-selection technique has a significant noise reduction effect for large noise pixels. The large noise pixels in CMOS image sensors have much larger noise than that of the majority of pixels. For instance, if the amplifier A_1

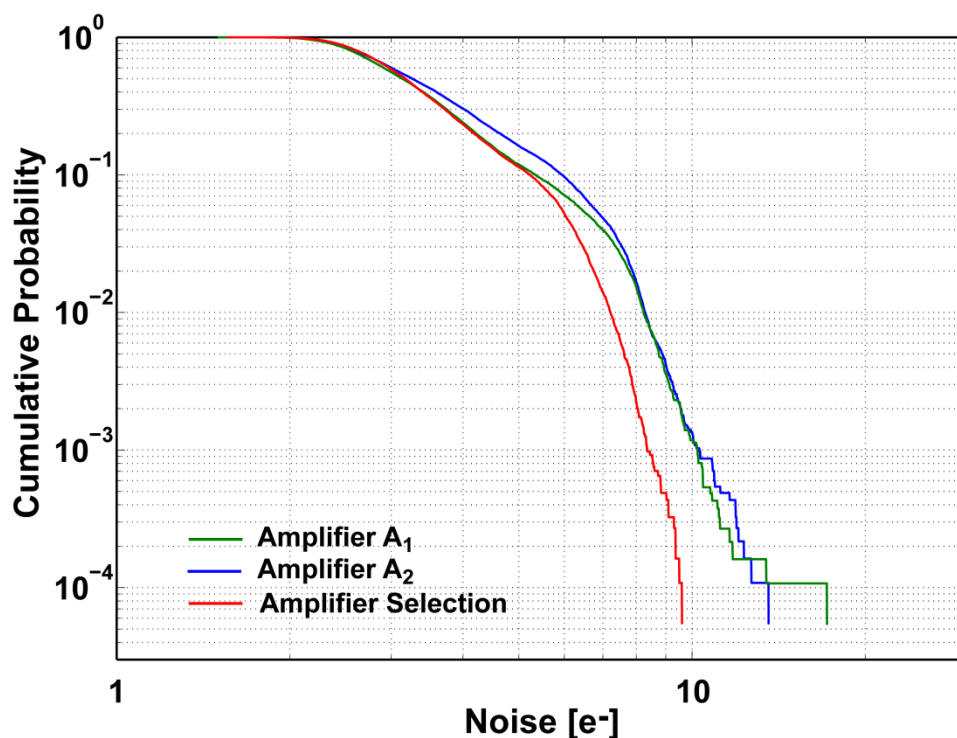


Fig. 3. Noise Distributions for signal readout methods with the amplifier A_1 only, amplifier A_2 only and the amplifier-selection technique.

only is used, the maximum noise where $CP=6 \times 10^{-5}$ is 17.2e-, while the noise at the median ($CP=0.5$) is 3.1e-. The large-noise pixels are mainly due to the RTS noise [4] and such large RTS noise in CMOS image sensors is visible though the population of large noise pixels is very small. As shown in Fig. 3, the maximum noise is reduced to 9.6e- by using the amplifier-selection technique, showing the effectiveness of the proposed technique for the reduction of the RTS noise.

Because of the relatively large number of transistors per pixel, the amplifier-selection technique is not always suitable for small-pixel image sensors, but useful for scientific image sensors which require large pixel size for high sensitivity. The designed amplifier-selection pixel has a fill factor (the ratio of photodiode area to pixel area) of 25.5% for the size of $7.5 \mu\text{m} \times 7.5 \mu\text{m}$ per pixel. By using on-chip microlens, the effective fill factor is enhanced to larger than 80%.

4 Conclusion

A technique for reducing the RTS noise in CMOS image sensors has been described. Each pixel has two selectable transistors and the lower-noise transistor is chosen for reading the signal. An experimental image sensor chip shows that the amplifier selection in pixels is effective for reducing large-noise pixels due to the RTS noise.

Acknowledgments

The present work was partially supported by the Knowledge Cluster Initiative of the Ministry of Education, Culture, Sports, Science and Technology and SENTAN, JST.