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Design space exploration of inductive degenerated Common – Source Low Noise Amplifiers (CS-LNA)

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Abstract: The inductive degenerated Common Source (CS) Low Noise Amplifier (LNA) is one of the widely used topology for realizing narrow band Radio Frequency (RF) CMOS LNAs. Though this scheme has been in use for a long time, realizing an optimum design still remains a challenging task. The present paper reports a simple and direct design space exploration procedure for the inductive degenerated CS LNA. The procedure first involves the use of a circuit simulator (Cadence Spectre) to generate a Look Up Table of small signal parameters. These are then used in a numerical simulator (MATLAB) to explore the entire design space by computing the various performance parameters and arrive at the final optimal designs. The predicted performances of the optimum designs were then verified using UMC 180 nm CMOS process parameters in Cadence Spectre. Completing all the computations on a typical low end desktop system within about an hour, the results presented indicate that one can search a design space of nearly fourteen million design candidates and arrive at an optimum of one's choice.

Keywords: inductive degenerated Common Source LNA, design methodology, design space exploration

Classification: Integrated circuits

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1 Introduction

In the wireless communication receiver design, the characteristics of the Low Noise Amplifiers (LNA) play a critical role and can impact the overall performance in different ways. For narrowband applications, the inductive degenerated Common-Source (CS) LNA is attractive since it permits resistorless input impedance match which leads to the realization of low Noise Figures (NF). Different approaches have been followed for its design and can be divided under three major category (i) classical noise matching, (ii) simultaneous input and noise match, and (iii) power constraint simultaneous input and noise match [1]. In many of the designs reported for the inductive degenerated CS LNA shown in Fig. 1, a simple small signal transistor model shown in Fig. 2 a has been made use of [1, 2, 3]. This model includes the gate to source capacitor and a dependent current source controlled by the voltage between gate to source terminals, but other capacitance and transconductance effects are not included. This simple model has also been used to derive the performance related analytical equations to arrive at a nominal design systematically [4, 5]. The neglect of parasitic effects results in the shift of expected performance from its desired resonant frequency, and calls for considerable effort by way of fine tuning with circuit simulators to meet the required specification. The inclusion of g_{ds} as shown in Fig. 2 b leads to a more realistic model for the transistors, however it impacts not only the real part of the input impedance, but also shifts the resonant frequency [6]. The accuracy of performance estimation could further be improved by incorporating the gate-drain capacitance (C_{gd}) in the small signal model of the transistor as shown in Fig. 2 c. The resulting ranges of circuit parameters and bounds on performances obtained are discussed in [7]. However, this further complicates the expression for determination of L_s, and hence the model in Fig. 2 a has been followed by many authors [1, 2, 3, 4, 5, 7]. Further, in all the models of Fig. 2 (a,b,c), the small signal model parameters used are heavily bias dependant, and also the accuracies of the values used for them are limited by the procedure used in their estimation. These values are normally extracted via DC simulation followed by curve fitting techniques [1, 2, 5, 8].

Although the inductor degenerated CS LNA had been in popular use for quite some time, there are still many issues associated with obtaining an

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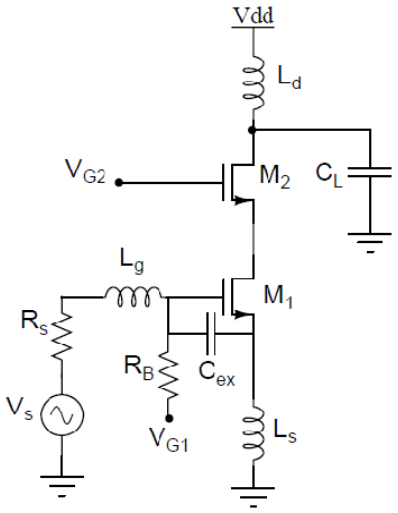

Fig. 1. Circuit of inductive degenerated common source LNA

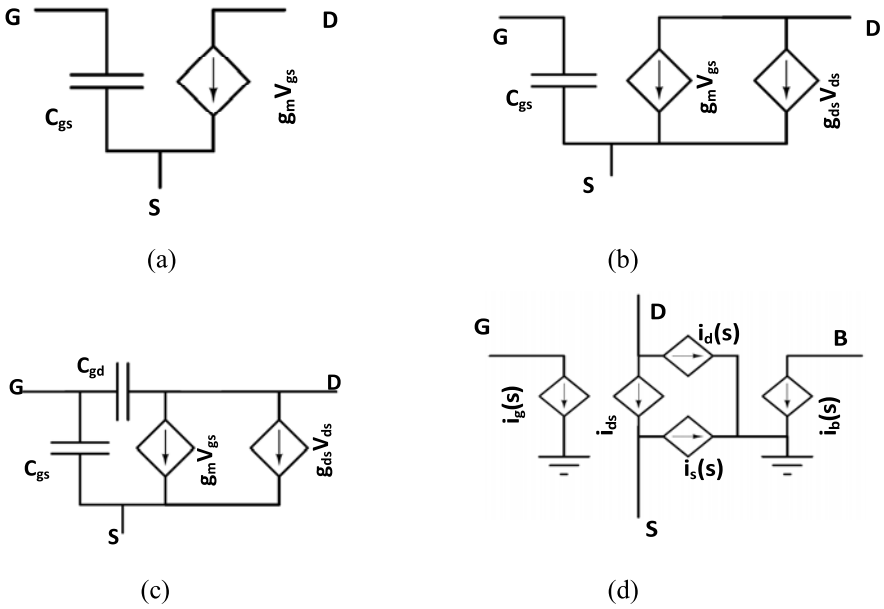

Fig. 2. Different small signal models of transistors used in LNA design and performance analysis (a) traditional model, (b) g_{ds} added model, (c) g_{ds} and C_{gd} included mode, and (d) model that utilizes BSIM3v3 model

optimum design. These issues have been spelt out very clearly and addressed in [7]. The present work addresses the same set of problems as in [7], but without involving any curve fitting techniques adopted in the latter. The small signal model used in the present work is shown in Fig. 2 d, and considers all the relevant transconductances and capacitances associated with a MOS transistor [9]. The model parameters have been created at each combination of bias voltages using a circuit simulator (Cadence Spectre) and stored in the form of a Look-Up-Table (LUT). Given the availability of accurate small model parameter values in an LUT, the performance predictions carried out

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by a numerical simulator such as MATLAB are also expected to be accurate. The effectiveness of the present methodology has been already demonstrated for the design space exploration of Common-Gate Common-Source (CGCS) LNA in [9].

The rest of the paper is organized as follows: The details of the proposed design space exploration technique for the inductive degenerated CS LNA given in Section 2. The results of simulations carried out and the various possible performance tradeoffs predicted by the design space exploration are presented in Section 3, and finally the conclusions of present work are given in Section 4.

2 Proposed design methodology for inductive degenerated CS LNA

In the present work, a bottom-up approach has been proposed. For selecting the biases and sizes of transistors to meet the given design specifications the performance is estimated for each selected bias and size combination with using an exhaustive search procedure. The combinations that satisfy the given constraints are identified as feasible designs.

The design work starts with the creation of LUT as the first step. Specifically, the values of all the critical small signal parameters as defined in BSIM3v3 model including all the transconductances (g_m, g_{ds}, and g_{mbs}), the terminal capacitances (C_{xy}, x, y = d, g, s, b) and junction capacitances (C_{jd}, C_{js}) of MOS transistor in Fig. 2 d are determined and stored in an LUT. This is carried out using a circuit simulator such as Cadence Spectre through DC simulation for all preselected permissible combinations of V_{GS}, V_{DS} and for fixed values of width (W) and length (L) of the MOS transistor. For different values of W, these entries are appropriately scaled. It may be noted that the LUT needs to be created only once, and can be used for any circuit design subsequently [9].

In the second step, the analytical expressions are derived for estimating the various performance parameters of interest including the input reflection coefficient (S_{11}), the forward gain (S_{21}) and the Noise Figure (NF). The expressions for S11 and S21 can be determined with the help of Fig. 3 which gives the equivalent circuit for Fig. 1 using the small signal model of Fig. 2 d. In order to include induced gate noise, a resistance (r_g) has been explicitly shown in the gate terminal of M_1. Although the drain noise current sources explicitly not shown in Fig. 3, the closed form expression for NF has been derived after inclusion of these appropriately.

In the present design exploration work, the gate voltages (V_{G1}, V_{G2}), the drain-source voltage (V_{DS1}) and width (W_1) are selected independently (free parameters). Since, the drain of cascade transistor M_2 is connected to the supply voltage via an inductor (L_d), the width (W_2) of M_2 can be fixed based on the DC current through M_1 and gate-source potential (V_{GS2}) of M_2. The introduction of an external capacitor C_{ex} between the source and gate terminals of M_1 is known to provide an additional degree of freedom

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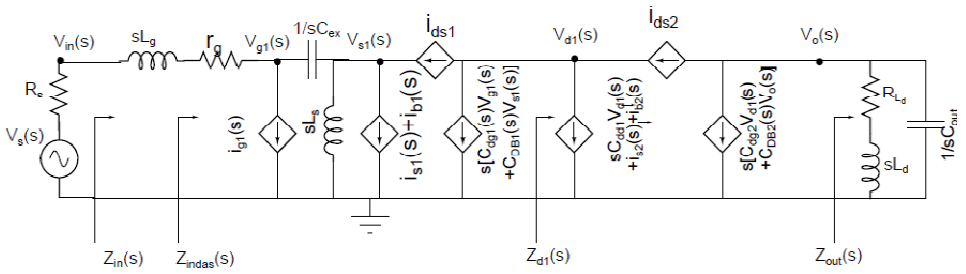

Fig. 3. Small signal model of inductive degenerated CS LNA circuit

in the selection of the quality factor of input stage (Q_s) which also impacts the values of NF and power consumption [7]. Thus, the five parameters W_1, V_{G1}, V_{DS1}, V_{G2} and Q_s considered as free parameters, constitute a design point in the present design framework. All other circuit and performance parameters are treated as functions of these five free parameters.

Sizing and biasing of Transistors: Without loss of generality, the transistors are operated with minimum length set by the technology. In order to reduce the size of LUT and reducing the dimension of free parameters, the source and bulk are tied together. For a given design point, i.e., for a given combination of (W_1, V_{G1}, V_{DS1}, V_{G2}, Q_s) the DC drain current through M_1 and M2 get fixed, and can be obtained from the LUT already generated. This in turn fixes W2 also.

Estimation of Inductors and Capacitor: The inductors and capacitors in a circuit decide the performance of the circuit over the frequencies of interest. For the small signal model in Fig. 2 d, the closed form expressions for various performance parameters have been derived using Fig. 3. These expressions are complicated in terms of number of parameters involved, but help in maintaining accuracy in the determination of performance parameters. For a selected design point, the determination of L_d, R_{Ld}, L_s, L_g and C_{ex} of Fig. 1 for a given load capacitance C_L will complete the design of the circuit. First, the external capacitor C_{ex} is obtained in terms of the quality factor (Q_s) of the input side from

$$Q_s = \frac{1}{2\omega_o R_s C_{tot}}, \tag{1}$$

where ω_o, R_s denote the desired angular resonant frequency of operation and source resistance respectively, and C_{tot} is sum of gate-source capacitance (C_{gs1}) of M_1 and external capacitance C_{ex}. Next, the inductor L_d used at the drain of the cascade transistor is decided based on ω_o and the resultant capacitance at drain of M_2 (denoted as C_{out} which is a sum of capacitances C_{dd2}, C_{jd2} of M_2 and C_L).

Next, using the small signal model of Fig. 2 d, and referring to Fig. 3, the closed form expression for the input impedance can be put in the form of Eq. (2). The equations in is given as,

$$Z_{in}(s) = s.L_g + Z'_{in}(s), \tag{2}$$

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In the above equation, the actual complete expression for Z'_{in} is lengthy and will be used only in the estimation of input reflection coefficient. But use of the expression for Z'_{in} which retains only terms upto the second power of 's' in its numerator and denominator as shown in Eq. (3) below was found adequate for the estimation of L_s. It may be noted here that the BSIM3v3 model does not account for r_g. Hence its inclusion here in Eq. (3) assumes that it would be determined using the expressions available for induced gate noise, for example in [6].

$$Z'_{in}(s) = r_g + \frac{a_0 + (a_1.L_s + a_2).s + (a_3.L_s^2 + a_4.L_s + a_5).s^2}{a_6.s + (a_7.L_s + a_8).s^2}, \tag{3}$$

To avoid loss of continuity, the details of other quantities used in Eq. (3) have been provided in the Appendix. Substituting '$j\omega_o$' for 's' and equating the real part of Eq. (3) to R_s yields the following polynomial equation for L_s

$$K_3 L_s^3 + K_2 L_s^2 + K_1 L_s + K_0 = 0, \tag{4}$$

Where,

$$\begin{aligned}
K_3 &= \omega_o^2 a_3 a_7, \\
K_2 &= \omega_o^2 (a_3 a_8 + a_4 a_7 - a_7^2 R_s), \\
K_1 &= a_1 a_6 - a_0 a_7 + \omega_o^2 (a_4 a_8 + a_5 a_7 - 2 a_7 a_8 R_s), \\
K_0 &= a_2 a_6 - a_0 a_8 - R_s a_6^2 + \omega_o^2 (a_5 a_8 - R_s a_8^2),
\end{aligned}$$

The existence of non-negative, real solution for L_s in Eq. (4) can be easily determined using MATLAB. If real solutions to Eq. (4) do not exist, it implies that the selected design point is not a feasible solution. Once a real L_s has been found, the value of L_g can be determined using Eq. (2).

The identification of all circuit parameters (C_{ex}, L_d, L_s, L_g) completes the design of CS LNA circuit in Fig. 1 and the performance evaluation of this circuit has to be carried out next. The power dissipation can be easily estimated from the product of drain current of M_1 and supply voltage (V_{DD}). Similar to Z_{in} given in Eq. (2), closed form expressions derived for the S_{11}, S_{21}, NF and could be used to estimate the respective performances. As their derivations are quite straight forward (but lengthy), the actual closed form expressions for S11, S21 and NF have not been presented here.

Design Space Exploration of CS LNA: For the design space to be explored, the performance corresponding to each point in the design space has been evaluated in the numerical simulator using the LUT and analytical expressions. A relaxed set of target performance specifications has been imposed on the circuit of Fig. 1, and provides flexibility to the designer to tradeoff and improve upon the specifications. All the design points that simultaneously meet the target specifications are identified as feasible design points and stored. At the end of design space exploration, all the non-dominated design points are extracted and these alone preserved. A variety of optimal solutions can then be selected at the end by sorting this non-dominated design set.

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3 Simulation and results

To validate the proposed design space exploration methodology, detailed simulations have been carried out using UMC 180 nm CMOS technology process parameters. The target specifications are given in Table I for 2.4 GHz and 10 GHz design. A nominal set of initial specifications have been assumed to demonstrate the possible further refinement and an optimum selection ones choice.

Table I. Design Goal Considered for CS LNA

Design Constraint Parameter	Value
Supply Voltage (V_{dd})	1.8V
Input reflection (S_{11})	< -10dB
Forward gain (S_{21})	> 10dB
Noise Figure (NF)	< 6dB
Bias current (I_{tot})	< 25 mA
Resonant frequency	2.4 GHz / 10 GHz
Source Impedance	50 Ω
Load capacitance (C_L)	5 pF
Q of L_d	30

To begin with, the LUT for the small signal and DC parameters for an NMOS transistor is created by setting a length of 0.18 μm (minimum possible), width of 50 μm, and zero source-bulk potential. In the overall design space exploration for the present case, a design point is denoted by the set [W_1, V_{GS1}, V_{DS1}, V_{G2}, Q_{sopt}]. The range of values explored for W_1 is from 1 μm to 400 μm in a step of 1 μm. With a step size of 0.1 V, the sweep ranges for V_{GS1}, V_{DS1}, and V_{G2} are chosen as (0.3 V to 1.8 V), (0.2 V to 1.6 V) and (V_{DS1} + 0.3 V, V_{DD}) respectively. The sweep range for Q_{sopt} has been chosen from 0.25 to 10 with an increment of 0.25.

The above ranges give approximately 14.2 million design combinations which constitute from the design space for the present case. Using the component values, small signal and DC parameters stored in the LUT, an exhaustive search of the design space carried out by computing the performance parameters using MATLAB. This resulted in identifying about 368 thousand design points satisfying all the specifications of Table I and these are the feasible design candidates. Based on the five performance parameters namely S_{11}, S_{21}, NF, ($W_1 + W_2$) and (I_{D1}), only 7179 points have been extracted as non-dominated solutions from the set of feasible candidate designs. On a typical low end personal computer with a 1.7 GHz processor with 1 GB RAM, this design space exploration takes about 45 minutes to search the entire design space and consolidate the non-dominated design points. The ranges of values of the circuit and performance parameters corresponding the non dominated set are listed in Table II (can this table also include the data for 10 GHz). This data is helpful since normally one is not aware of what potential performance values can be attained by the circuit of Fig. 1, and

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Table II. of Realized Ranges of Design Parameters and Performance Metrics

	Parameter/metric	Minimum Value	Maximum value
Dependent circuit Parameters	Ls	0.1 nH	0.9 nH
	Lg	5.3 nH	64.5 nH
	C_{ex}	0.0 fF	302.0 fF
Performance Parameter	NF	1.2 dB	6.0 dB
	S_{21}	13.6 dB	35.5 dB
	I_{D1}	0.35 mA	5.2 mA
	$W_1 + W_2$	5.8 µm	419.1 µm

Table III. Identified Design by Proposed Methodology and Their Verification in Cadence Spectre

Free parameters		Designed Parameters		Performance metric	Simulation Tool	
					MATLAB	Cadence Spectre
2.4GHz Design						
W_1	100 µm	I_{D1}	3.73 mA	S_{11}	-30.7 dB	-35.7 dB
		r_g	6.1 Ω			
V_{GS1}	0.7 V	W_2	15.8 µm	S_{21}	30.2 dB	30.3 dB
		L_s	0.46 nH			
V_{G2}	1.4 V	L_g	13.2 nH	NF	1.2 dB	1.2 dB
		L_d	0.88 nH			
V_{DS1}	0.3 V	R_{Ld}	0.4 Ω	fo	2.4 GHz	2.399 GHz
Q_{sopt}	3.75	C_{ex}	58.3 fF			
10GHz Design						
W_1	24 µm	I_{D1}	7.5 mA	S_{11}	-25.9 dB	-17.8 dB
		r_g	6.2 Ω			
V_{GS1}	1.3 V	W_2	86.4 µm	S_{21}	18.2 dB	19.1 dB
		L_s	0.15 nH			
V_{G2}	1.6 V	L_g	5.7 nH	NF	1.4 dB	1.5 dB
		L_d	0.05 nH			
V_{DS1}	0.8 V	R_{Ld}	0.1 Ω	fo	10.0 GHz	10.05 GHz
Q_{sopt}	5.5	C_{ex}	0.5 fF			

whether these call practically realizable component values.

To confirm the correctness of the MATLAB based design identification and performance prediction, these were cross checked with Cadence Spectre based simulations. As a comparison, from the identified non-dominated design set, those offering minimum NF at 2.4 GHz and at 10 GHz are listed in Table III. It may be seen that all the MATLAB performance predictions agree closely with those obtained using Cadence Spectre simulations. The values obtained for V_{GS}-V_{TH}, bias current and noise performance are comparable to those given in [7]. The 10 GHz design shows a deviation of 50 MHz between MATLAB and Cadence resonant frequency predictions. This devia-

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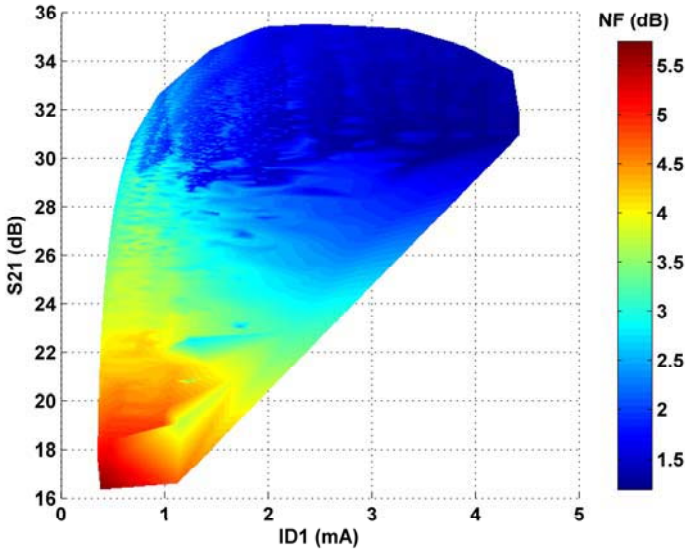

Fig. 4. NF Contour in S_{21}-I_{D1} plane

tion at higher frequency designs could be possibly be attributed to restricting the number of poles and zeros in the expression used for the determination of L_s (Eq. (5)).

The data available in the form non-dominated solutions can also be used to perform multiobjective optimization. Since the design solution space that needs to be searched is quite small, one can select the mulitobjective optimum merely by sorting and there is no need to invoke any of the well known optimization techniques. The available trade-off between different performance metrics could be explored by analyzing the hyperplane connecting all non-dominated design solutions. Due to limitations in the graphical presentation, the NF of all feasible designs has been projected in a S_{21}-I_{D1} plane and shown in Fig. 4 and pertains to the 2.4 GHz design. In this figure, the colored portions show the possible combinations of performance parameters (non-dominated) for which feasible designs exist within the design space. It may be observed that above 1.5 mA, the minimum feasible gain achievable increases with the current consumption. And lower noise figures are realized jointly with high gains above 30 dB. Low power designs below 2 mW has need to tolerate higher NF (> 4.5 dB) and lower gain (< 20 dB). While on the low power consumption side, there is a wide range of trade off possible between gain and NF, it is not so for higher power consumption.

Plots similar to those in Fig. 4 relating other design parameters such as bias potentials and transistor width, performance metrics such as S_{11} etc. can also be generated to facilitate multi-objective.

4 Conclusion

A fast and accurate design methodology for designing inductive degenerated common source LNA has been presented. The use of an appropriate model to utilize the small signal parameters extracted with the help of circuit simulator enhances the speed and accuracy in the design cycle. This is carried

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out with the exhaustive search of entire design space and sorting of the non-dominated design solutions. The collected solutions enable a designer to get an optimal solution quickly with minimum effort and also enable a flexible tradeoff between multiple performance metrics. A similar design space exploration consisting of a few million design points is almost impossible to accomplish solely with conventional simulation techniques using tools like Cadence Spectre. One limitation of the present work is that only BSIM3v3 models have been used for LUT generation, but however, the induced gate noise effect has been suitably taken into account while simulating in MATLAB as well as Cadence. The same methodology could be easily extended to utilize higher versions of BSIM descriptions.

A. Appendix

The details of the parameters associated with the Eq. (3) of the main text are provided in this Appendix. Since the methodology used in this work makes extensive use of BSIM3v3 model parameters, the same symbols have been retained as in BSIM3v3 with added subscripts related to M_1 and M_2. Hence, these symbols are not explained explicitly here. The remaining symbols and parameters associated with Eq. (3) are as follows,

$$r_g = \frac{1}{5g_{d0}}$$
$$a_0 = b_{0zd} + g_{ds1}.a_{0zd}$$
$$a_1 = G_{m1}.(b_{0zd} + a_0)$$
$$a_2 = b_{1zd}$$
$$a_3 = {G_{m1}}^2.b_{0zd}$$
$$a_4 = 2.C_{BB1}.(b_{0zd}+g_{ds1}.a_{0zd})+G_{m1}.b_{1zd}-a_{0zd}.(G_{m1}.C_{BD1}+g_{ds1}.C_{DB1})$$
$$a_5 = b_{2zd}$$
$$a_6 = C_{gg1}.(b_{0zd} + g_{ds1}.a_{0zd}) - C_{gd1}.g_{m1}.a_{0zd}$$
$$a_7 = C_{gg1}.G_{m1}.(2.b_{0zd} + g_{ds1}.a_{0zd}) - C_{gd1}.G_{m1}.g_{m1}.a_{0zd} + C_{GB1}.g_{m1}.b_{0zd}$$
$$a_8 = C_{gg1}.b_{1zd} - C_{gd1}.C_{dg1}.a_{0zd}$$
$$a_{0zd} = 1 + g_{ds2}.R_{out}$$
$$b_{0zd} = G_{m2}$$
$$b_{1zd} = Cx.(1 + g_{ds2}.R_{out}) + G_{m2}.R_{out}.C_{BD2} + g_{ds2}.R_{out}.C_{DB2}$$
$$b_{2zd} = -R_{out}.C_{DB2}.C_{BD2}$$
$$G_{m1} = g_{m1} + g_{ds1}$$
$$G_{m2} = g_{m2} + g_{ds2}$$
$$C_{DD1} = C_{dd1} + C_{jd1}$$
$$C_{BB1} = C_{ss1} + C_{bb1} + C_{sb1} + C_{bs1}$$
$$C_{DB1} = C_{db1} + C_{ds1} - C_{jd1}$$
$$C_{BB2} = C_{ss2} + C_{bb2} + C_{sb2} + C_{bs2}$$
$$C_{DB2} = C_{db2} + C_{ds2} - C_{jd2}$$

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$$C_x = C_{BB2} + C_{DD1}$$
$$R_{out} = Q_{Ld}^2 R_{Ld}$$

In this work, the current through external capacitance C_{ex} has been appropriately accounted in the current sources associated with the gate and source terminals of M_1 by considering C_{gg1}, C_{ss1}, C_{gs1} and C_{sg1} as, $C_{gg1} + C_{ex}$, $C_{ss1} + C_{ex}$, $C_{gs1} - C_{ex}$ and $C_{sg1} - C_{ex}$ respectively to simplify the expressions.

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