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Configurable transmitter with de-emphasis scheme supporting wide range data rates

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Abstract: This paper presents a configurable driver with programmable impedance, output slew rate and de-emphasis control scheme. The proposed driver is implemented using 45 nm CMOS technology which can be configured as a differential push-pull driver or differential current-mode driver. In push-pull mode, the driver can operate with mid-rail swing. In current-mode, it can support 400 mV and 500 mV low voltage swing. Configurable driver provides multiple impedances of 50, 75 or 150 Ω that can be selected for transmit impedance and receive terminator. Besides that, with slew rate control scheme, the driver slew rate can be programmed at 2–5 V/ns for data rate below 4 Gbps. However, slew rate control scheme is bypassed and de-emphasis control scheme is activated to gives 6 dB de-emphasis to equalize ISI losses at date rate above 4 Gbps and thus, improving signal integrity.

Keywords: CMOS, I/O driver, integrated circuit

Classification: Integrated circuits

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1 Introduction

Microprocessor and application specific integrated circuit (ASIC) vendors often offer a fixed output driver circuit that is optimized for a single system application. Alternatively, vendors also can offer a fixed output driver that is compromise of various system applications [1]. This is because each MCM vendor has a different cost-performance-risk-schedule trade-off for the combination of application and chip supplier [2]. Thus, it is challenging for an IC with fixed input/output (I/O) circuit achieving optimum performance across variety of applications.

Besides, the trend in chip area reduction has led to the development of new packaging approaches. Parasitic components in package and substrate can cause system noises such as simultaneous switching noise (SSN) and reflection noise which can deteriorate the I/O circuit performances [3, 4, 5, 6, 7, 8, 9, 10, 11]. Moreover, with the increase of I/O frequency, inter-symbol interference (ISI) between successive signals caused by frequency dependent attenuation of transmission line are more pronounce and degrade signal integrity [11, 12, 13, 14, 15]. Those system noise considerations force a fixed output driver designed to compromise for multiple applications which can impact the overall system performance [1].

Several attempts were reported to address these problems. Paper [3, 4, 5, 6] proposed the output drivers that are adaptable to various loads or applications. However, the driver's full-swing nature is restricting it from operating toward high data rates and is susceptible to reflection noise due to the nonlinear characteristics of output impedance. Paper [7] proposed a dual-mode transmitter with adaptive slew rate and impedance control to overcome sys-

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tem noise and support different signal swing across wide range data rates. However, the symmetric error in current mirror can cause the output swing of current-mode driver has large deviations from desired value across PVT corners. Besides, paper [12] presented a voltage mode de-emphasis driver to overcome ISI losses, however, the output impedance is not always constant and this can cause signal reflection problem.

Therefore, this paper presents a configurable output driver circuit that is integrated with on-chip impedance, slew rate and de-emphasis control scheme to address reflection noise, minimize output oscillations and overcome transmission loses across a variety of intended processor applications. The rest of this paper is organized as follows. Section 2 describes the overall system architecture. The details of transmitter design are presented in Section 3. Section 4 discusses the post-layout simulations while Section 5 concludes the performance of the proposed design.

2 Overall architecture

The overall architecture of proposed system is depicted in Fig. 1. Data controller is used to process input for output driver. Input and output can be two single-ended or differential data, depending on mode control signal (MODE). The proposed output driver consists of three driver modules and each module is further decomposed to four driver stages. Pull-up and pull-down segment in each driver stage are PVT-compensated at 600 Ω. This gives an equivalent output impedance of 150 Ω when all the four stages in a module are activated. Thus, by enabling different number of driver modules in parallel using MODULE_EN[2:0] signal, multiple impedance values of 50, 75 or 150 Ω can be obtained.

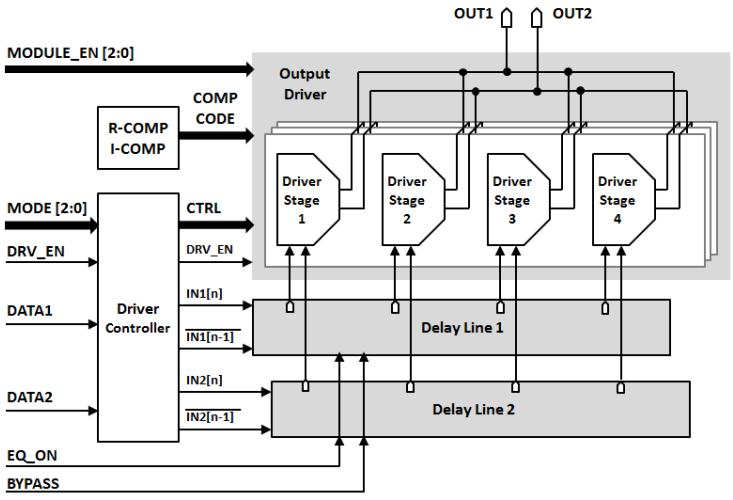

Fig. 1. Overall system block diagram.

Impedance compensation R-COMP block is used to calibrate on-chip impedance value. When the proposed driver is configured as current-mode driver, current compensation I-COMP block can be used to calibrate out-

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put swing across PVT variations [15, 16]. Besides, output slew rate and de-emphasis control scheme are applied to reduce switching noise and ISI noise respectively. The details of these control schemes will be discussed in the following sub-sections.

2.1 Slew rate control scheme

Digital time domain splitting technique is widely used when an I/O circuit requires a stable control of slew-rate and output impedance.

This scheme is effective as simultaneous switching noise and reflection noise can be reduced at the same time. Fig. 2 shows a simplified diagram of a driver module designed using time split technique. Output driver in each module is segmented into four driver stages with pull-up and pull-down impedance are four times larger than desired module impedance Z, i.e. 150 Ω so that total impedance is always constant at 150 Ω during switching. By activating each driver stage in sequence after T_d delay interval, output transition time can be controlled.

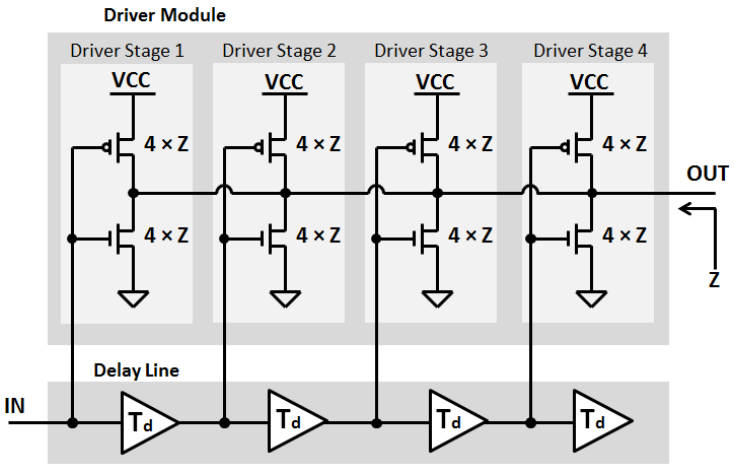

Fig. 2. Time split technique: Simplified diagram of one driver module with delay line.

The delay interval of each delay cell is calibrated at 40 ps using Delay Locked Loop (DLL) [7] to control the output transition time to be approximately 160 ps. For data rate higher than 4 Gbps, delay cells should be bypassed so that the output transition is no longer restricted by delay intervals. Fig. 3 shows the architecture of delay line with bypass circuit. A multiplexer is added at the output of each delay cell and controlled by signal BYPASS. When BYPASS is low, multiplexers will select output of delay cells for driver stages. If BYPASS is high, delay cells are bypassed and the multiplexers will select IN for all the driver stages.

2.2 De-emphasis control scheme

A basic concept for de-emphasis is shown in Fig. 4. This is two-tap de-emphasis with a main tap driver and a post-cursor tap driver. Main cursor tap driver outputs ordinary data, while post-cursor tap driver outputs

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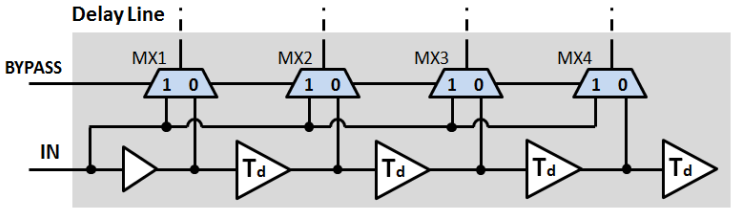

Fig. 3. Delay line with bypass circuit.

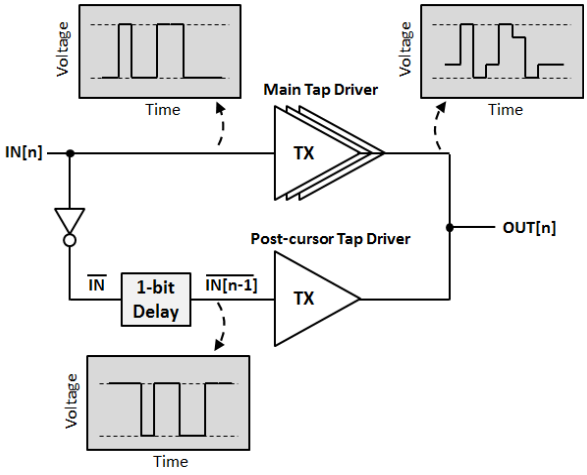

Fig. 4. Basic de-emphasis diagram.

inverted one bit shifted data and these output signals are connected together [12, 13, 14, 15].

Fig. 5 shows the generic idea of integrating de-emphasis control scheme into the proposed design. First three driver stages in a driver module can be connected as main tap driver, while last driver stage is connected as post-cursor tap driver. To drive main tap driver and post-cursor tap driver with their corresponding data, the delay lines should be bypassed and a new multiplexer can be added in the existing delay lines architecture. Fig. 6 shows the delay line modified to support de-emphasis control scheme. A multiplexer MXEQ added to output post-cursor tap data IN[n−1] to post-

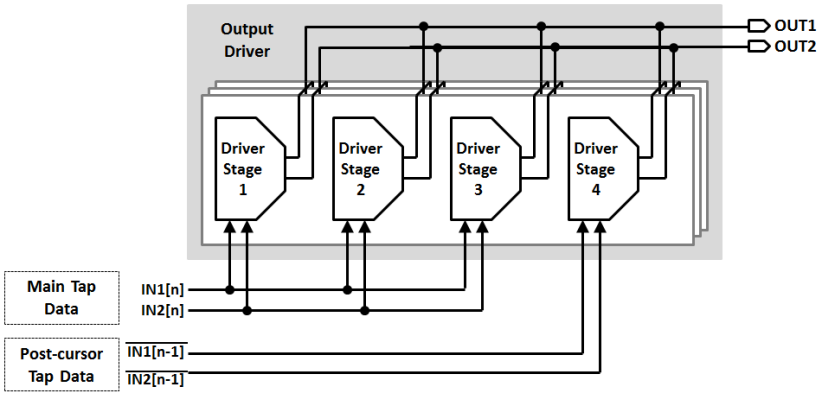

Fig. 5. Generic idea of adding de-emphasis control scheme in proposed output driver.

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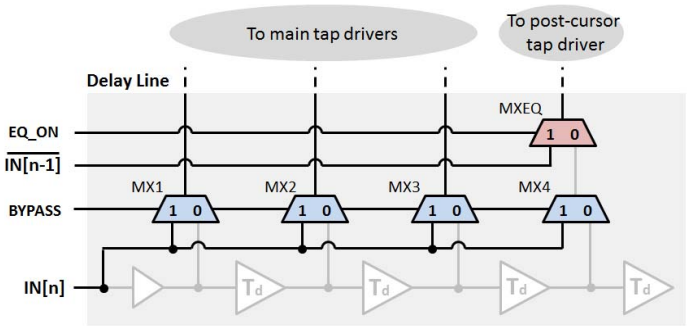

Fig. 6. Modified delay line to support de-emphasis control scheme.

cursor tap driver when de-emphasis is required. Besides, de-emphasis ratio can be calculated by using the Eq. (1) in the following [13]:

$$\text{De-emphasis (dB)} = -20\log[(\text{J} - \text{K})/(\text{J} + \text{K})] \tag{1}$$

where J is number of instances in main tap driver and K is number of instance in post-cursor tap driver. Thus, de-emphasis achieved by proposed driver is $-20\log[(3-1)/(3+1)] = 6\,\text{dB}$ that is independent of output impedance. This is because de-emphasis is only depends on number of instances in main tap and post-cursor tap driver, while the output impedance is constant due to calibration in the driver stage. This gives a constant de-emphasis across PVT variations as compared to de-emphasis transmitter in [12] where the number of instances in main tap and post-cursor tap driver are not constant due to output impedance tuning.

3 Output driver design

3.1 Driver architecture

Fig. 7 shows the architecture of driver stage that consists of pre-driver and main driver. Pre-driver provides appropriate VP1, VP2, VN1, VN2 and VSW signal based on mode control signal and data. Main driver comprises of two half drivers with a switch M7 between them. Series resistor R1 and

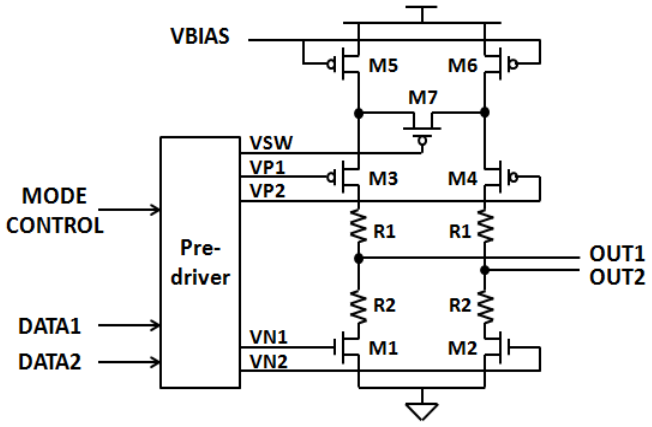

Fig. 7. Pre-driver and main driver architecture in a driver stage [9].

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R2 can help to improve the linearity of pull-up and pull-down segment [7, 8, 9, 10, 11, 12, 13, 14, 15].

3.2 Single-ended, differential push-pull driver and current-mode driver

Main driver can be configured as two single-ended push-pull drivers, a differential push-pull driver or differential current-mode driver, as discussed in paper [8]. The macro-model of push-pull driver is shown on Fig. 8.

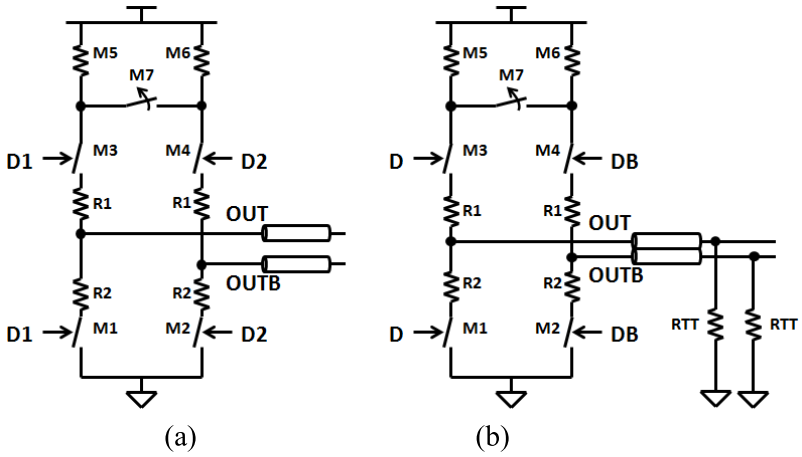

Fig. 8. Macro-model of push-pull driver configured from main driver: (a) Single-ended driver. (b) Differential driver.

Besides, Fig. 9 shows the current-mode driver configured from main driver and the operations are discussed in [8]. It can be noticed that current-mode driver in the proposed design has tail current sources and transistor M7 as a switch. The reason of splitting single tail current source into two current sources is to increase the flexibility of proposed design to be configured as two single-ended push-pull drivers. However, the existence of switch M7 can affect high impedance of tail current sources which can further affect

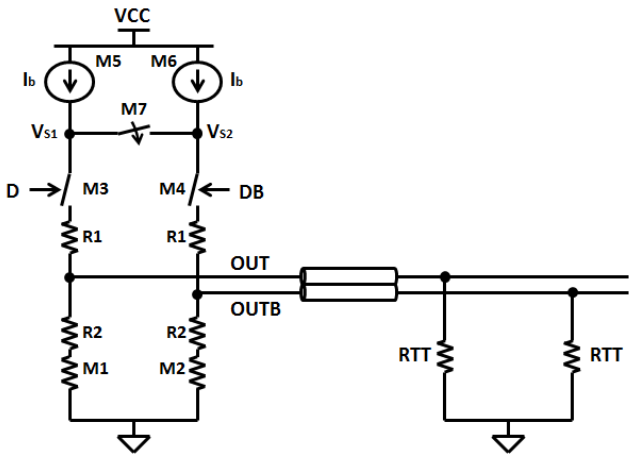

Fig. 9. Macro-model of differential current-mode driver.

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output impedance. Thus, the output impedance of current-mode driver in the proposed design is derived to investigate the effect of switch M7. The inputs are set as shown in Fig. 10 (a). Two tail transistors with the size are half of that in conventional current-mode driver (W/L). Thus, the output impedance of each tail transistor in saturation is $2 \times R_o$. Transistor M7 and M3 are in linear region and modeled as R_{sw} and R_{M3} respectively, while transistor M4 is off and modeled as open-circuit. Obviously, when input switch M4 is off, output impedance at node OUTB is equal to Rt. The output impedance at node OUT can be determined from the AC model of Fig. 10 (b).

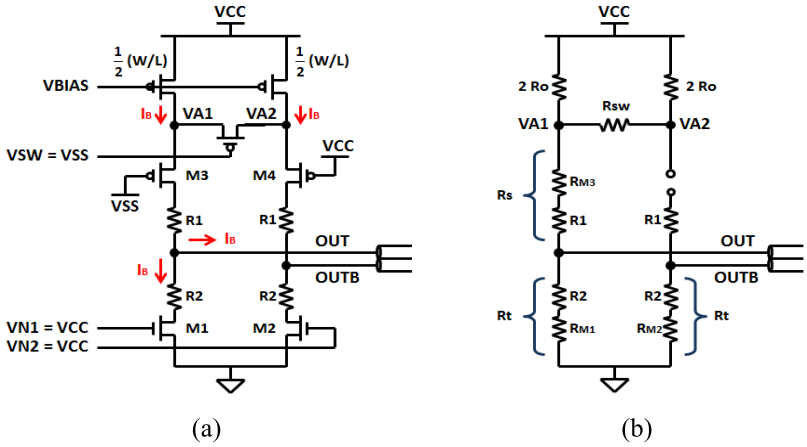

Fig. 10. Current-mode driver configured from proposed design with one input transistor is on and another is off. (b) Equivalent resistance model in (a).

Fig. 11 (a) shows the AC model of current-model driver in Fig. 10 (a). Equivalent output impedance of two tail transistors with a switch between them can be determined by evaluating the impedance between node v_{a1} and ground

$$R_o' = 2R_o||(2R_o + R_{sw}) = \frac{4R_o^2 + 2R_oR_{sw}}{4R_o + R_{sw}} \tag{2}$$

By simplifying AC model in Fig. 11 (a) to Fig. 11 (b) with expression of R_o' in (2), the output impedance at node *out* can be determined as

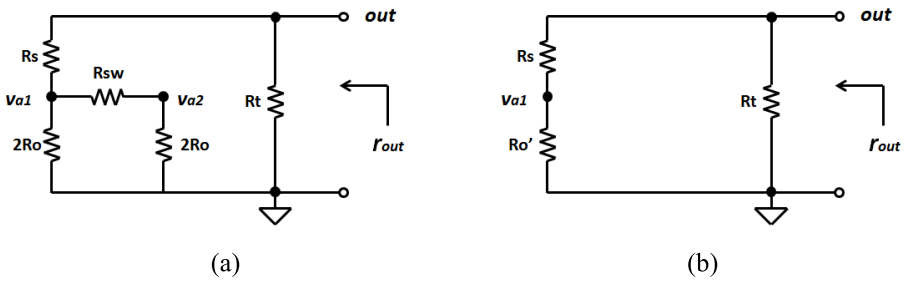

Fig. 11. (a) AC model from Fig. 10 (b). (b) Simplified AC model.

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$$r_{out} = R_t||(R'_o + R_s) = R_t|| \left(\frac{4R_o^2 + 2R_oR_{sw}}{4R_o + R_{sw}} + R_s \right) \tag{3}$$

$$r_{out} = \frac{R_t \left[4R_o^2 \left(1 + \frac{R_{sw} + 2R_s}{2R_o} \right) + R_sR_{sw} \right]}{4R_o^2 \left(1 + \frac{R_{sw} + 2R_s + 2R_t}{2R_o} \right) + R_{sw}(R_s + R_t)} \tag{4}$$

Assuming R_o is very large compared to R_s, R_t and R_{sw},

$$r_{out} \approx \frac{R_t[4R_o^2 + R_sR_{sw}]}{4R_o^2 + R_{sw}(R_s + R_t)} \tag{5}$$

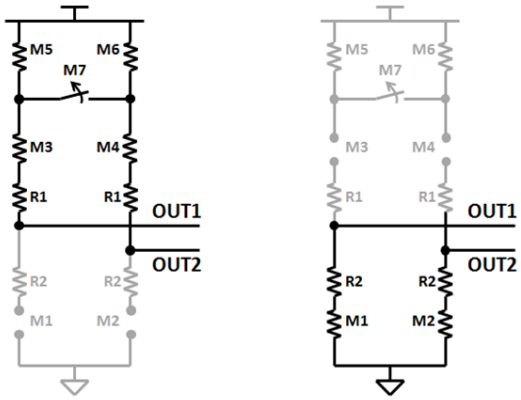
By making R_{sw} very small compared to R_o, the r_{out} in (5) can be approximated to

$$r_{out} = \frac{R_t \cdot 4R_o \left(1 + \frac{R_sR_{sw}}{4R_o^2} \right)}{4R_o \left(1 + \frac{R_{sw}(R_s + R_t)}{4R_o^2} \right)} \approx R_t \tag{6}$$

Thus, by making R_{sw} very small (by increasing transistor size), output impedance r_{out} of driver can be approximated to terminator R_t to avoid signal reflections. However, the size of switch should not be too large as it is silicon area inefficient.

3.3 Receive terminator

In receiving mode, the driver can be configured as near-end receive ODT to power supply or ground, as shown in Fig. 12. The operation is the same as push-pull driver, except that the data is set to high or low for termination to supply or ground, respectively. This receive termination-merged driver can reduce output pin capacitance as compared to conventional implementations which had separate structure for transmit drivers and receive termination [8, 9].



(a) (b)

Fig. 12. Receive ODT (a) to power supply. (b) to ground.

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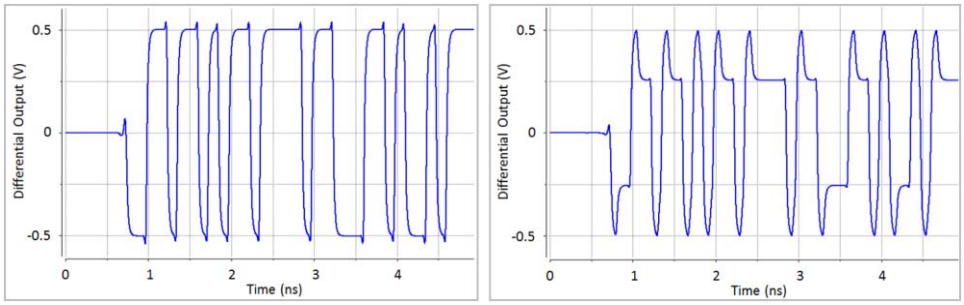
4 Post-layout simulation results

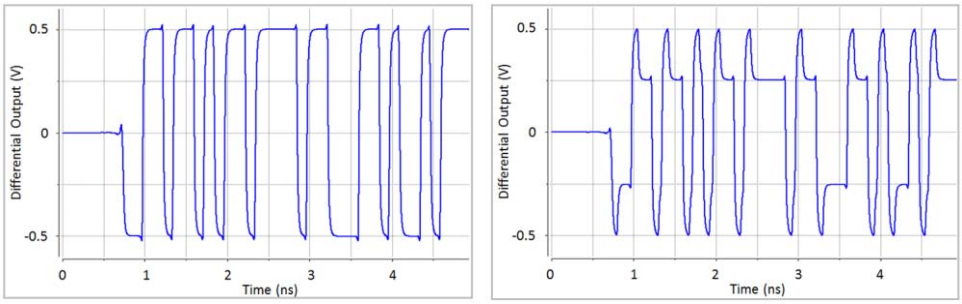
4.1 Differential voltage-mode and current-mode driver

The proposed design can support wide range of data rates from 0.4 to 8 Gbps. De-emphasis scheme can be activated for long transmission and high data rates since frequent dependant attenuations of transmission line become significant and cause ISI problem. Fig. 13 shows the differential output of push-pull driver with driving impedance of 50 Ω and 6 dB de-emphasis scheme is deactivated and activated at 8 Gbps in typical condition. Besides, Fig. 14 (a) shows the differential output of current-mode driver with single-ended swing calibrated at 500 mV, while Fig. 14 (b) shows the differential output of current-mode driver with driving impedance of 50 Ω and 6 dB de-emphasis at 8 Gbps in typical condition.



(a) (b)

Fig. 13. Differential output waveform of push-pull driver at 8 Gbps (a) without de-emphasis, (b) with de-emphasis.



(a) (b)

Fig. 14. Differential output waveform of current-mode driver at 8 Gbps (a) without de-emphasis, (b) with de-emphasis.

4.2 Driver performance with high data rates

When the proposed design is operated with long transmssion line up to 30 mm, de-emphasis scheme has to be activated to allow adequate eye opening at high data rates. Eye mask of 200 mV (differential) and 0.6 UI is used

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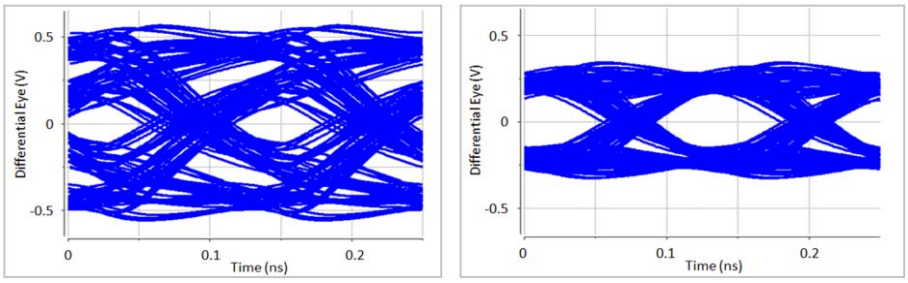
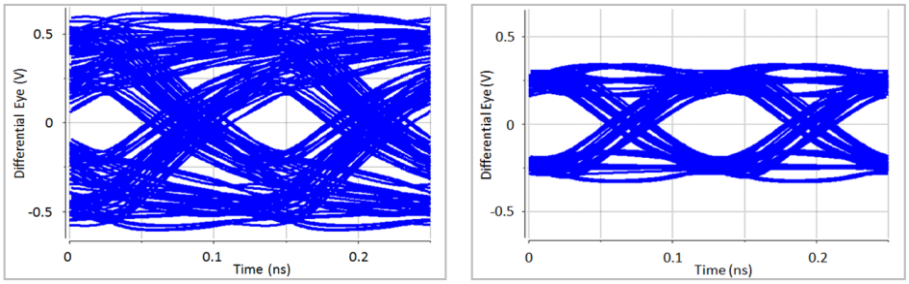
for performance validity. Fig. 15 (a) shows the far-end differential eye digram of push-pull driver at 8 Gbps. Eye jitter and maximum eye height are 0.5 UI and 226.9 mV respectively. Fig. 15 (b) shows the far-end differential eye signal of push-pull driver simulated at 8 Gbps with de-emphasis with eye jitter and eye height are improved to 0.29 UI and 312.8 mV. Besides, Fig. 16 (a) shows the far-end differential eye diagram of current-mode driver simulated at 8 Gbps and 30 mm transmission line without applying de-emphasis. Simulated eye jitter and eye height are 0.47 UI and 316.7 mV which are better than that in voltage-mode driver without de-emphasis. By applying 6 dB of de-emphasis, the far-end differential eye opening in Fig. 16 (b) is improved with eye jitter and eye height value of 0.26 UI and 367.5 respectively.



(a) (b)

Fig. 15. Far-end differential eye waveform of push-pull driver simulated at 8 Gbps and 30 mm transmission line, simulated (a) without de-emphasis, (b) with de-emphasis.



(a) (b)

Fig. 16. Far-end differential eye waveform of current-mode driver simulated at 8 Gbps and 30 mm transmission line, simulated (a) without de-emphasis, (b) with de-emphasis.

4.3 ODT performance with 50 Ω and 75 Ω

When receiving data from far-end, the proposed design can be configured as near-end receive ODT with 50 or 75 Ω. Fig. 17 (a) shows eye diagram with 50 Ω ODT at 8 Gbps and 20 mm transmission line. Simulated jitter and eye height are 0.10 UI and 807.2 mV. Besides, 75 Ω ODT can be used as

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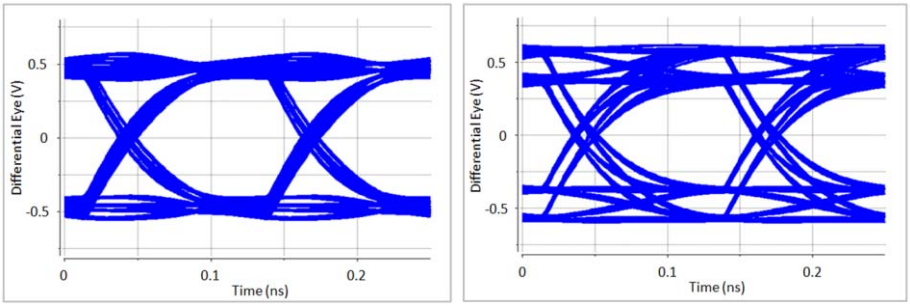

(a) (b)

Fig. 17. Eye diagram with ODT value of (a) 50 Ω, and (b) 75 Ω, simulated at 8 Gbps.

termination for power saving purposes, at the expense of eye opening due to impedance mismatched, as shown in Fig. 17 (b). Eye jitter and eye height is 0.15 UI and 666.3 mV, but in overall the eye opening is still sufficient for data detection and sampling.

Table I shows the performance summary of the proposed design. Average

Table I. Performance summary of proposed design.

Driving Impedance		Voltage-Mode	Current-Mode
Process Technology		45 nm CMOS	
Silicon Area (Four Driver Modules)		312 X 196 μm^2	
Operating Speed		0.4 Gbps - 8 Gbps	
Operating VCC		1.0 V ± 5 %	
Average Power (at 8 Gbps)	50 Ω ODT (mW)	5.40	
	75 Ω ODT (mW)	4.98	
	50 Ω Driver (mW)	25.64	29.36
Without De-emphasis (at 8 Gbps, 30 mm of TL length)	Eye Jitter (ps)	0.50	0.47
	Eye Height (mV)	226.90	316.70
With De-emphasis of 6 dB (at 8 Gbps, 30 mm of TL length)	Eye Jitter (ps)	0.29	0.26
	Eye Height (mV)	312.80	367.50

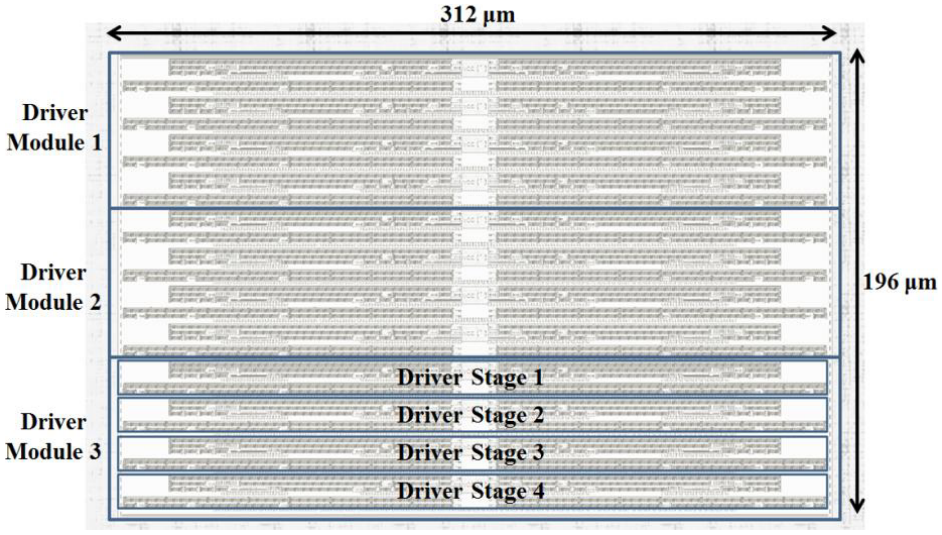

Fig. 18. Layout of output driver consists of four driver modules.

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power consumption is 5.40 mW with 50 Ω ODT. The 75 Ω ODT can be selected to reduce average power to 4.98 mW at the expense of eye opening. Besides, current-mode driver has better jitter and eye height performance as compared to push-pull driver in the cases of de-emphasis and without de-emphasis. Fig. 18 shows the layout of four driver modules with total area of $321 \times 196\,\mu m^2$.

5 Conclusion

A configurable output driver supporting wide range data rates from 0.4–8.0 Gbps is proposed. Termination impedance mismatches and output swing deviations (in current-mode driver) are solved by digital calibration schemes. Output slew rate can be controlled between 2–5 V/ns. With de-emphasis scheme, both the push-pull driver and current-mode driver are capable of reducing 42.0% and 44.7% of far-end eye jitter, respectively. Current-mode driver has relatively large far-end eye opening, but it consumed extra 12.7% of average power as compared to voltage-driver.

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