ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.13, 1–6

# A low phase noise FBAR based multiband VCO design

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**Abstract:** In this letter, design methodlogy of a low phase noise multiband film bulk acoustic resonator (FBAR) based voltage controlled oscillator (FBAR-VCO) is presented. It employs a 1.9 GHz cross-coupled FBAR-VCO core, and extends oscillation to 0.65 GHz, 0.98 GHz, 1.96 GHz and 3.92 GHz by a divider and a multiplier. By analyzing the low frequency instability and proposing the solution based on a capacitor, cross-coupled architecture is employed in 1.9 GHz FBAR-VCO core and phase noise degradation is extensively studied for extended frequencies. By considering the effect of transistors' size on the Q-factor and impedance of FBAR, excellent phase noise and high loop gain are obtained. The post-layout simulation shows the proposed multiband FBAR-VCO achieves the lowest phase noise below −150 dBc/Hz at 1 MHz offset frequency.

**Keywords:** FBAR, low phase noise, low frequency instability, multiband, VCO

**Classification:** Integrated circuits

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DOI: 10.1587/elex.10.20130425
Received June 02, 2013
Accepted June 17, 2013
Publicized June 28, 2013
Copyedited July 10, 2013

## 1 Introduction

In the fields of frequency reference and high precision sensors which use frequency as the output variable, low phase noise miniature oscillator is greatly demanded [1, 2, 3, 4]. Traditionally, quartz crystal oscillators are widely used because of the excellent phase noise performance [1, 2]. However, large physical size, incompatibility with CMOS technology and low frequency output have severely limited the applications of quartz crystal oscillators in GHz-range and in highly miniaturized sensors in the future.

In response to the growing demand for GHz-range frequency and miniaturization, FBAR resonators which have Q-factor around 1000 or even more, have been used to design low phase noise GHz-range oscillators [1, 2, 3, 4] for frequency reference and highly reliable sensors to replace quartz crystal oscillators in recent years. Nevertheless, simple single-ended architecture is employed and the possibility of multiband FBAR-VCO has never been studied.

In this letter, a multiband FBAR-VCO to oscillate at 0.65 GHz, 0.98 GHz, 1.96 GHz and 3.92 GHz is presented. By analyzing the low frequency instability and proposing the solution based on a capacitor, a cross-coupled architecture is employed in 1.9 GHz FBAR-VCO core and phase noise optimization for FBAR-VCO by considering the effect of transistors' size on the Q-factor and impedance of FBAR has been studied for the first time.

## 2 Reviews on FBAR resonator

Figure 1 (a) shows the equivalent circuit of the Modified Butterworth Van Dyke (MBVD) model [5] of FBAR, where $R_s$, $R_0$, $R_m$, $C_0$, $C_m$ and $L_m$ are the electrical parameters of FBAR. FBAR resonators have two resonance frequencies, series resonance frequency ($f_s$) and parallel resonance frequency ($f_p$) as shown in Fig. 1 (b). The estimated Q-factor at the series resonance frequency ($Q_s$) and that at the parallel resonance frequency ($Q_p$) are about 800 and 1200, respectively.

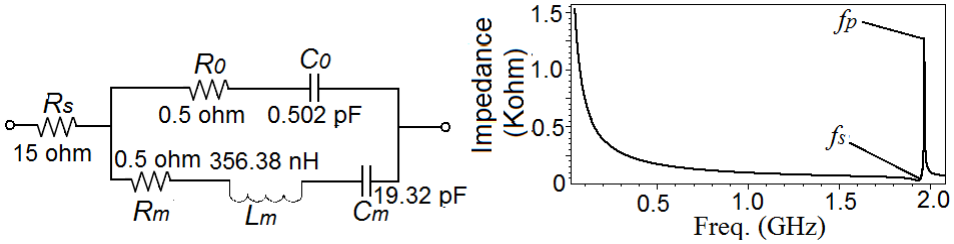


**Fig. 1.** MBVD model (a) and impedance response (b) of FBAR

## 3 Proposed multiband FBAR-VCO design

### 3.1 Circuit design

The proposed multiband FBAR-VCO is composed of a 1.9 GHz cross-


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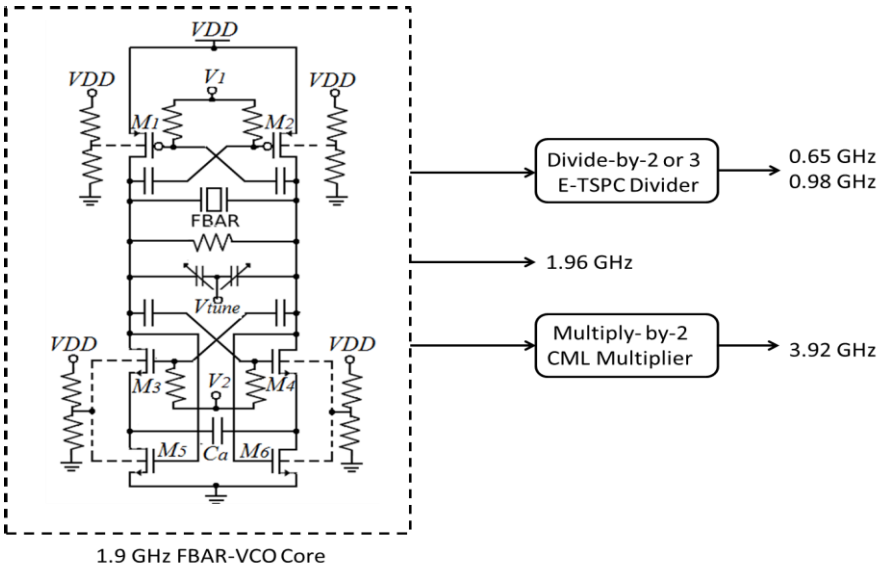


**Fig. 2.** Proposed multiband FBAR-VCO

coupled FBAR-VCO core, and extends oscillation frequencies by a divide-by-2 or 3 divider and a multiply-by-2 multiplier as as shown in Fig. 2.

Because cross-coupled FBAR-VCO suffers from low frequency instability problem, simple single ended architecture is employed in most of the published FBAR-VCO [1, 2, 3]. In [4], although a cross-coupled FBAR-VCO is proposed, the phase noise performance is not good and the reason and solution of low frequency instability is not explained in theory. In our design of FBAR-VCO core, both NMOS ($M_1$, $M_2$) and PMOS ($M_3$, $M_4$) transistors are used to constitute two cross-coupled pairs to reuse current and provide larger negative resistance and their bias voltages are provided by $V_1$ and $V_2$ respectively. A tail feedback current source, composed of $M_5$ and $M_6$, is used to control the common-mode drain voltage of the cross-coupled pairs. $V_{tune}$ is used to control the oscillation frequency of the VCO. Capacitor $C_a$ creates a high frequency path to eliminate the low frequency instability, which will be presented in detail in subsection 3.2. The sizes of all transistors are well optimized, which prevents large Q-degeneration of FBAR caused by parasitic capacitance and on-resistance to get a low phase noise and a high loop gain. The optimized method will be described in subsection 3.3. Finally, an extended true single phase clock logic (E-TSPC) based divide-by-2 or 3 divider is used to generate 0.65 GHz and 0.98 GHz output, and a current mode logic (CML) based multiply-by-2 multiplier is employed to generate 3.92 GHz frequency.

### 3.2 Low frequency instability analyses and elimination

In the design of a cross-coupled FBAR-VCO, the major challenge is to solve the instability in low frequency which causes parasitic oscillation. In this subsection, not only the reason of instability is analyzed in theory, but also the solution method based on a capacitor is proposed. Considering the definition of loop gain, the small signal loop gain of the proposed FBAR-VCO core is


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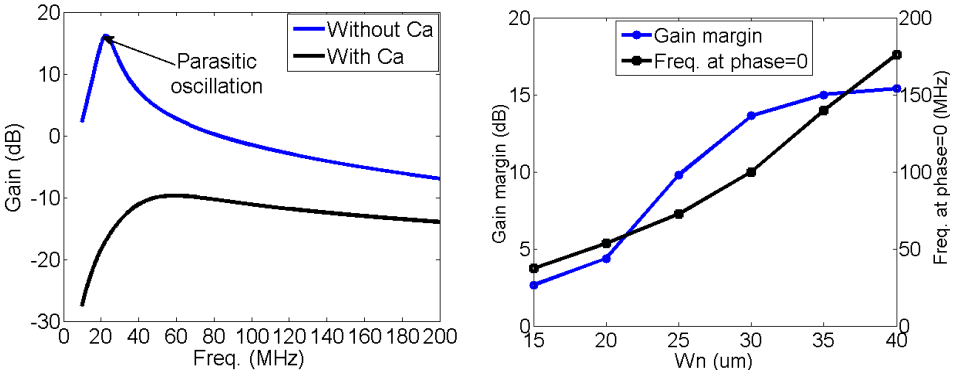
$$Gain = \left( \frac{(g_{pm} + g_{nm}) \left( R_{non} || R_{pon} || \frac{Z_f}{2} \right)}{1 + (g_{pm} + g_{nm}) \frac{Z_s}{2}} \right)^2 \quad (1)$$

where $g_{pm}$ and $g_{nm}$ are the trans-conductance of PMOS transistors and NMOS transistors respectively; $R_{pon}$ and $R_{non}$ are the on-resistance of PMOS transistors and NMOS transistors respectively; $Z_f$ is the impedance of FBAR, and $Z_s$ is the impedance between the sources of $M_3$, $M_4$. From Eq. 1, it is clear that high loop gain occurs not only at the frequency $f_p$, but it also occurs in low frequency as FBAR also has high impedance in low frequency as shown in Fig. 1 (b), and $Z_s$ is always small in normal condition. For this reason, low frequency instability and parasitic oscillation will happen if loop gain exceeds 0 dB satisfying Barkhausen's criterion which is illustrated in Fig. 3 (a).




(a) (b)

**Fig. 3.** (a) Low frequency loop gain comparison between with $C_a$ and without $C_a$, (b) low frequency gain margin with the changing of $W_n$

To prevent parasitic oscillation, the high loop gain in low frequency should be reduced by increasing $Z_s$ in low frequency. The capacitor $C_a$ is added between the sources of $M_3$, $M_4$, which creates a high frequency path reduces the loop gain in low frequency, as shown in Fig. 3 (a). If the value of $C_a$ is not large enough, it will cause an undesirable reduction of the loop gain at the frequency $f_p$. If the value of $C_a$ is too large, parasitic oscillation will not be eliminated. In this letter, $C_a$ is set to 2 pF for the trade-off between low frequency stability and loop gain.

In addition, the effect of the size of NMOS transistors on the gain margin in low frequency is also considered. Fig. 3 (b) shows that the gain margin in low frequency decreases with the decrease in the size of NMOS transistors ($W_n$). The reason is that the impedance of FBAR has a great growth with frequency decrease and the frequency in which phase margin is equal to zero, is decreasing with the decrease of $W_n$. In this letter, $W_n$ is set to 30 $\mu$m.

### 3.3 Optimization of phase noise and loop gain

In Leeson phase noise model [6], the relationship between Q and phase noise is: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$$L(f_m) \propto \frac{kT}{P_{out}} \bullet \frac{1}{2Q^2} \bullet \frac{f_0^2}{f_m^2} \tag{2}$$

where $k$ and $T$ are constants; $L(f_m)$ is the phase noise at the offset frequency $f_m$ from the oscillation frequency $f_0$ and $P_{out}$ is the output power. It is known that phase noise improves as both the carrier power and Q-factor increase. Because the Q-factor of FBAR will be deteriorated by the on-resistance reduction of transistors, large size transistors should be avoided. Both the size reduction of PMOS transistors and that of NMOS transistors can raise the on-resistance, but based on the analysis in subsection 3.2, the size reduction of NMOS transistors will decrease the gain margin in low frequency. Therefore, only the size of PMOS transistors is adjusted to optimize the phase noise. In Fig. 4 (a), it is shown that when the size of PMOS transistor ($W_p$) is decreasing from 110 $\mu$m to 50 $\mu$m, the Q-factor of FBAR is increasing and the phase noise is improving. Thus, this region is called Q limit region. When $W_p$ is below 50 $\mu$m, although the Q-factor is still increasing, the phase noise is not improving because of the reduction of the oscillation amplitude, which is called peak to peak voltage ($V_{pp}$) limit region. For the loop gain, it can be known from Eq. 1 that as the loop gain also increases with the increase in on-resistance of transistors, the optimal size which can get the best phase noise, can also obtain high loop gain, as shown in Fig. 4 (b).

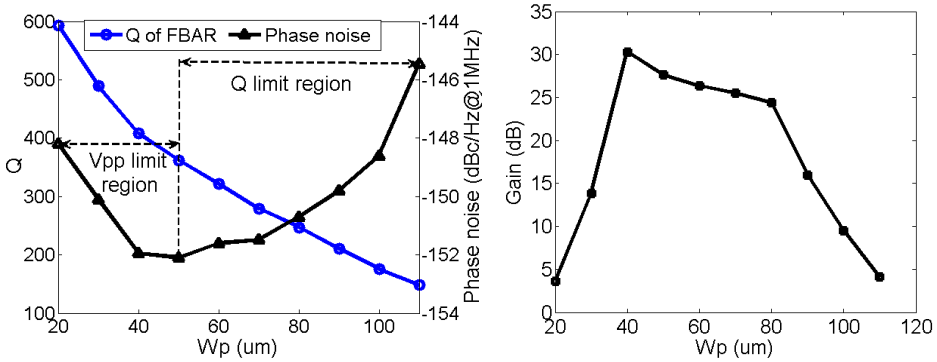


**Fig. 4.** Relationship among $W_p$, Q-factor, phase noise (a) and loop gain (b)

## 4 Post-layout simulation results

The proposed multiband FBAR-VCO designed in 0.18 $\mu$m CMOS operates at 0.65 GHz, 0.98 GHz, 1.96 GHz and 3.92 GHz successfully. The layout is shown in Fig. 5 (a) and the post-layout simulation phase noise is shown in Fig. 5 (b). Table I is the comparison with other published works. It is shown that below 1.96 GHz, the proposed multiband FBAR-VCO has very low phase noise below −150 dBc/Hz at 1 MHz offset and even in 3.9 GHz, the phase noise is still below −140 dBc/Hz. All the FOMs of four bands are below −200 dB and the minimum FOM is as low as −215 dB, much better than other published works. The analyses and simulation results demonstrates that a very low phase noise and low power multiband VCO using FBAR based VCO could be designed and developed for future


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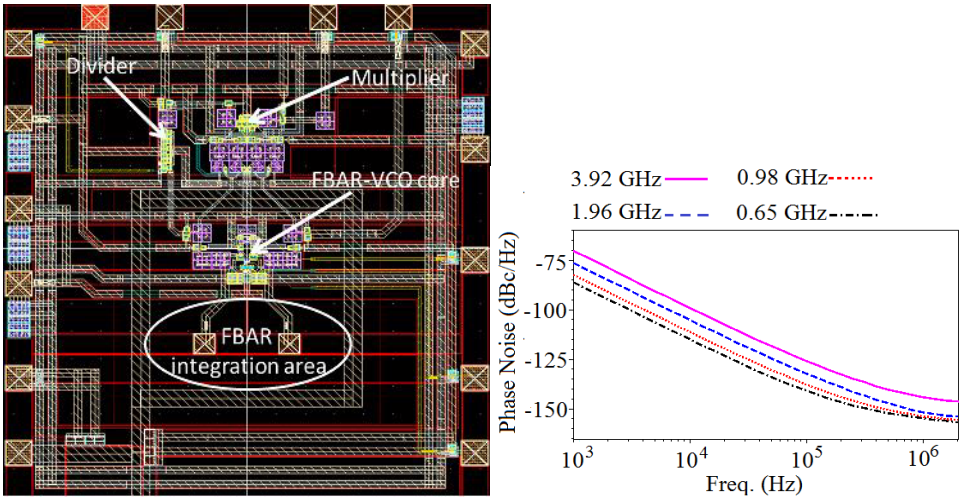


(a) (b)

**Fig. 5.** Layout (a) and simulation phase noise (b) of the proposed multiband FBAR-VCO

**Table I.** Comparison with other published oscillators

| | This work | | | | [1] | [4] |
|---|---|---|---|---|---|---|
| Process | 0.18μm CMOS | | | | 0.35μm CMOS | 0.13μm CMOS |
| Vdd (V) | 1.1 | | | | 2 | 1.0 |
| $f_0$ (MHz) | 650 | 980 | 1960 | 3920 | 1500 | 1575 |
| Power (mW) | 3.97 | 4 | 1.7 | 4.3 | 1.2 | 0.5 |
| Tuning range (MHz) | 0.67 | 1 | 2 | 4 | 0.3 | 1.35 |
| $L(\Delta f)$ @ 1MHz (dBc/Hz) | -154.6 | -153.5 | -151.5 | -143.2 | -147 | -138 |
| FOM | -205 | -207 | -215 | -209 | -209 | -204 |

generation wireless communication systems. In fact, this multiband VCO is under fabrication process which will be reported in a future publication.

## 5 Conclusion

In this letter, a multiband FBAR-VCO operating at 0.65 GHz, 0.98 GHz, 1.96 GHz and 3.92 GHz for narrow band applications such as frequency reference and highly miniature sensors is presented. Low frequency instability is solved and by novel optimization method, it obtains an excellent phase noise and FOM value. Futhermore, the possibility of a multiband VCO using FBAR-VCO as a core circuit has been demonstrated. However, the problem of narrow tuning range has still been prevailed which is under investigation and will reported in near future.

## Acknowledgement

This work was supported by "Funding Program for World-Leading Innovative R&D on Science and Technology" and a Grant-in-Aid for Scientific Research (B) (KAKENHI-B). This work was also partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with CADENCE Corporation and Agilent Corporation.


DOI: 10.1587/elex.10.20130425
Received June 02, 2013
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