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A novel delay optimization method for a critical path in VLSI design

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Abstract: This paper presents a new method for optimizing the delay of a critical path with an embeded long wire for global routing. And an appropriate effective fan-out factor (EFOF) for optimizing the sizes of the devices in the critical path is derived. Simulations show that the new optimization method can obtain more accurate delay estimation for a critical path than traditional method, which offers significant result for automatic floor-plan and routing in VLSI design.

Keywords: critical path, fan-out factor, path delay, VLSI

Classification: Integrated circuits

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1 Introduction

In deep sub-micron processes, in order to simulate the delay of logic path more accurately, a variety of path delay models have been built [1]. Usually, two independent aspects are considered in delay optimization and/or calculation, which are modeling the wire to estimate the delay of wires and optimizing the sizes of the devices in a critical path to shorten the path delay, respectively. This divide-and-rule method is generally used in design and/or simulation of high-performance chips. However, with the rapid development of the IC technology and the persistent increasement of the routing complexity in VLSI, more accurate models are required for optimizing the delay of a critical path [2, 3].

Wire delays not only increase with wire length, but also affect the total

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delay of a critical path if it is connected in different positions. This paper shows that the wire delay and logic chain optmization should be considered as a whole. Based on this concept, we build a new model to optimize the delay of a critical path with an embedded long global wire. Meanwhile an appropriate EFOF is derived to optimize the sizes of the devices in critical path. The work reported here is a significant extension of global routing optimizing in VLSI design.

2 Traditional delay optimization method of a critical path

In the following discussions, the inverter chain is given as an example of logic path.

The delay of a inverter can be expressed as:

$$t_p = t_{p0}\left(1 + \frac{C_{ext}}{SC_{iref}}\right), \tag{1}$$

where t_{p0} is the intrinsic delay, which denotes the delay of the inverter itself without external load, and is only determined by the specific process. C_{ext} is the external load capacitance of the inverter, and C_{iref} is the intrinsic input capacitance of a standard minimum size symmetry inverter (SMSSI, i.e. the NMOS in the inverter adopts the smallest size, while the PMOS is chosen to have the equivalent resistance as NMOS.). S is the size ratio of the other inverters to the SMSSI [1].

According to Eq. (1), if the size of a logic gate is large enough, then its impact on the path delay will become obvious. Thus, the sizes of the latter gates in the logic path should be larger [4]. In fact, when optimizing one critical path, we must consider the trade-off between the delay and device area.

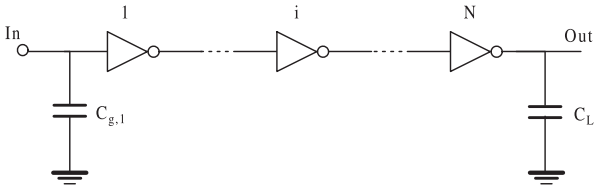

Fig. 1. The inverter chain model.

An inverter chain model with N inverters is shown in Fig. 1, wherein $C_{g,1}$ is the input gate capacitance of the first inverter. We assume that the first inverter is a SMSSI. C_L is the total external load capacitance. The total delay of the inverter chain is

$$t_p = t_{p0}\sum_{i=1}^{N-1}\left(1 + \frac{C_{g,i+1}}{C_{g,i}}\right) + t_{p0}\left(1 + \frac{C_L}{C_{g,N}}\right). \tag{2}$$

In Eq. (2), the minimum delay can be found by taking N-1 partial derivatives and equating them to zero, then the following relation can be obtained

$$C_{g,i} = \sqrt{C_{g,i-1}C_{g,i+1}}. \tag{3}$$

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According to Eq. (2) and Eq. (3), if the delay of each inverter is equal, the minimum total delay of inverter chain can be

$$t_p = N t_{p0} \left(1 + \sqrt[N]{F}/\gamma\right), \tag{4}$$

In Eq. (4), the total EFOF of the circuit F is equal to $C_L/C_{g,1}$, while γ is a process constant, and its value is about 1. The EFOF of each inverter is

$$f = \sqrt[N]{F} = \sqrt[N]{\frac{C_L}{C_{g,1}}} = \frac{C_{g,i+1}}{C_{g,i}}. \tag{5}$$

Thus, if the size ratio of the adjacent inverters in logic chain is f, then the minimum total delay of a logic path can be achieved by Eq. (4) [1].

3 Optimizing the delay of a critical path with an embeded long wire

We assume that there is a long wire connecting the i-th and the (i+1)-th inverters in the logic path, as shown in Fig. 2. The π-type wire model is adopted here, which is shown inside the rectangular box in Fig. 2.

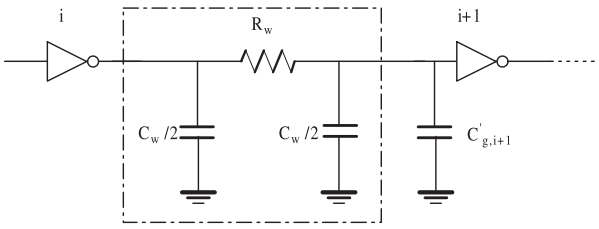

Fig. 2. Inverter chain with a long wire in it.

The i-th inverter's gate capacitance is denoted as $C'_{g,i}$. We assume that the EFOF of the inverter chain in Fig. 2 is same as Fig. 1, the total path delay of the inverter chain in Fig. 2 is given by (The delay time of a π-type wire model with parasitic resistance R and parasitic capacitance C is 0.69RC/2)

$$\begin{aligned} t_p = t_{p0} \sum_{i=1}^{N-1} \left(1 + \frac{C'_{g,i+1}}{C'_{g,i}}\right) + t_{p0} \left(1 + \frac{C_w/2}{C'_{g,i}}\right) + \\ 0.69 R_w \left(\frac{C_w}{2} + C'_{g,i+1}\right) + t_{p0} \left(1 + \frac{C_L}{C_{g,N}}\right). \end{aligned} \tag{6}$$

just as Eq. (2), the minimum delay can also be found by taking N-1 partial derivatives, and equating them to zero. To solve the i-th and the (i+1)-th gate capacitances, we have use the following two differential equations:

$$\frac{\partial t_p}{\partial C'_{g,i}} = \frac{1}{C'_{g,i-1}} - \frac{C_w/2}{C'^2_{g,i}} = 0 \tag{7}$$

$$\frac{\partial t_p}{\partial C'_{g,i+1}} = 0.69 R_w - \frac{t_{p0} C'_{g,i+2}}{C'^2_{g,i+1}} = 0. \tag{8}$$

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Now we define the new EFOF of the inverter chain as $f' = C'_{g,i+1}/C'_{g,i}$. From the above deduction, we can arrive at the following equation

$$f'^{N+1} = \frac{0.69R_wC_w}{2t_{p0}} \cdot \frac{C_L}{C_g, 1} \approx \frac{0.35rcL^2f^N}{t_{p0}}. \tag{9}$$

If the wire delay is considered, only under the condition that the EFOF of the inverters comply with Eq. (9), the total path delay can be minimized.

Then the optimized gate capacitance of the (i+1)-th inverter is $C'_{g,i+1} = f'^i C_{g,1}$. The total path delay of the logic chain with a embeded long wire is gived by

$$t_p = Nt_{p0}(1 + f') + 0.69R_w \left(\frac{C_w}{2} + f'^i C_{g,1} \right). \tag{10}$$

From Eq. (10) we can see that the total path delay is related with the location of the wire.

In the above discussion, we have assumed that the EFOFs of all devices are equal. However, after independently optimizing the delays of two sub-segments of the inverter chain separated by the long wire, we can obtain the total delay of the inverter chain.

$$\begin{aligned} t_p = it_{p0} \left(1 + \sqrt[i]{\frac{C_w/2}{C''_{g,1}}} \right) + 0.69R_w \left(\frac{C_w}{2} + C''_{g,i+1} \right) + \\ (N-i)t_{p0} \left(1 + \sqrt[N-i]{\frac{C_L}{C''_{g,i+1}}} \right). \end{aligned} \tag{11}$$

In Eq. (11), for a specific i, although the value of the second term on the right-hand side increases with the increasement of $C''_{g,i+1}$, the third term decreases with the increasement of $C''_{g,i+1}$. Then, the variation of the delay will be smaller. We can conclude that it is reasonable to choose the same EFOF in the two sub-segments of the logic path when optimizing the total path delay. This conclusion will be further verified by the incoming simulation.

4 Simulations

TSMC 0.18 μm CMOS technology with standard digital library is employed to perform the simulations.

In Eq. (11), i and $C''_{g,i+1}$ are the variables of t_p. The simulation results of the relations of t_p, i, and $C''_{g,i+1}$ are shown in Fig. 3 (a). It can be seen from Fig. 3 (a) that if $C''_{g,i+1}$ is relative larger, and the long wire is located in the hind part of the logic path, the total path delay will become smaller. However, if the wire is located in the fore segment of the logic path, the total path delay will increase obviously.

It also can be seen from Fig. 3 (a) that when $C''_{g,i+1}$ increases to a specific value, the path delay will reach the minimal value. But if $C''_{g,i+1}$ increases continuously, the delay has only a small increasement relative to the minimum delay. And this indicates that the value of $C''_{g,i+1}$ can be selected in a quite large-scale range if we want to obtain a small delay. And this conclusion is also verified at the end of the previous section.

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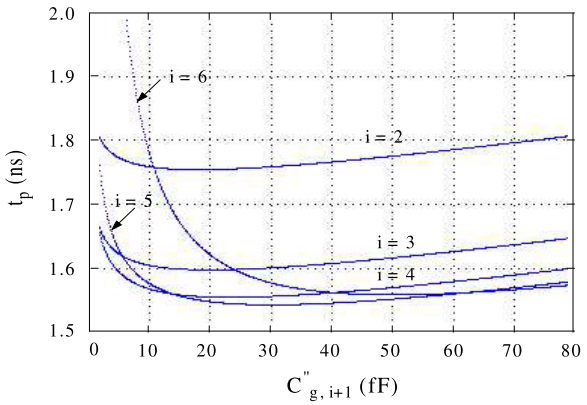

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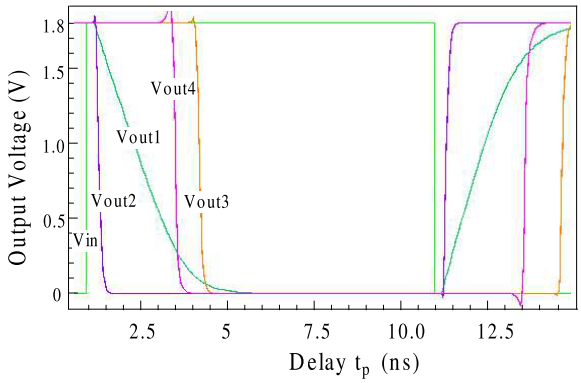
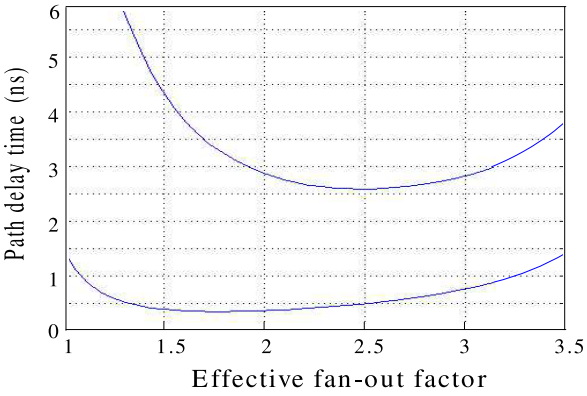


(b)



(c)

Fig. 3. (a) The relations of t_p, i and $C''_{g,i+1}$; (b) Delay simulations of 4 different cases; (c) The relations between the EFOF and path delay.

Next, we simulate the delays in four different cases. In the simulations, the external load capacitances are the same, and the input signal Vin is an ideal square wave. The four cases are described as follows, respectively.

Case 1) The inverters in the critical path are all SMSSI. The output wave is Vout1.

Case 2) The inverter chain adopts the EFOF calculated from Eq. (5), but the influence of the wire is not considered. The output wave is Vout2.

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Case 3) The EFOF is chosen to be the same as that in case 2), and a long wire is connected between the i-th and the (i+1)-th inverters. The output wave is Vout3.

Case 4) The delay model is same as that in case 3), but the value of EFOF is calculated from Eq. (9) ($f' = 2.7$). The output wave is Vout4.

Simulation results are shown in Fig. 3 (b). Because the invert chain in case 1) are not be optimized, so the delay of the Vout1 is worse. By comparing the simulation results of case 3) and case 4), it can be seen that if we use the EFOF that is derived from Eq. (9), the path delay is 0.8 ns shorter than that adopting the traditional EFOF derived from Eq. (5).

The simulation results of the relations between the EFOF and path delay are shown in Fig. 3 (c). The lower curve corresponds to the case that the influence of the wire in logic path is not considered, and the optimal EFOF value is about 1.7. The upper curve corresponds to the case that a long wire is connected between the 4-th and the 5-th inverters in a logic chain (the logic chain consists of 7 inverters). It can be seen from Fig. 3 (c) that the smallest delay can be achieved when the value of EFOF is about 2.6. And this value quite approaches the value of 2.7 calculated from Eq. (9).

5 Conclusion

A new method for optimizing the delay of a critical path with an embeded long wire is proposed. In the proposed method, a new EFOF for optimizing the sizes of the devics in the critical path is derived. Simulation results show that the new method can obtain better accuracy than the conventional methods by considering the wire and logic chain as a whole. The proposed method is well suited for optimizing the delay of a critical path when routing a global long wire in VLSI design.

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