ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.21, 1–6

Highly linear low voltage low power CMOS LNA

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Abstract: A highly linear, low voltage, low power, low noise amplifier (LNA) using a novel nonlinearity cancellation technique is presented in this paper. Parallel Inductor (PI) matching is used to increase LNA gain by 3 dB at the desired frequency. The linear LNA was designed and simulated in a TSMC 0.18 μm CMOS process at 5 GHz frequency. By employing the proposed technique, the IIP_3 is improved by 12 dB in contrast to the conventional folded cascode LNA, reaching -1 dBm without having any significant effect on the other LNA parameters such as gain, NF and also power consumption. The proposed LNA also delivers a voltage gain (S_{21}) of 12.25 dB with a noise figure of 3.5 dB, while consuming only 1.28 mW of DC power with a low supply voltage of 0.6 V.

Keywords: low noise amplifier (LNA), folded cascode, high linear, low power, low voltage, current reuse

Classification: Integrated circuits

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DOI: 10.1587/elex.10.20130557
Received July 16, 2013
Accepted September 04, 2013
Publicized October 22, 2013
Copyedited November 10, 2013

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1 Introduction

The increasing demands upon portable wireless devices have motivated the development of CMOS radio frequency integrated circuits (RFIC). These devices require low power dissipation to maximize battery lifetime. Some low power applications, such as wireless medical telemetry, require the portable devices to operate at low supply voltage with a small battery or environment energy, thus the power and supply voltage constriction is a crucial issue for these designs [1].

On the other hand, due to the possible large interference signals at the input of a low-noise amplifier (LNA), the LNA has to provide high linearity to prevent the intermodulation tones created by the interference signal from corrupting the carrier signal. This linearity improvement should not be at the cost of gain or noise figure (NF). This requires the use of linearization techniques implemented with minimal current overhead. In order to improve the linearity of LNAs, several linearization techniques have been proposed recently [2]. In [3, 4], the linearity factor was improved without paying attention to the NF parameter. In [5], linearity was dramatically enhanced, but the presented topology requires a high supply voltage and consumes more power. In this paper, a new implementation of the linearization technique which is recommended for low voltage and low power LNAs is proposed while gain and NF are maintained approximately constant.

2 Circuit description

The cascode structure is extensively used in the LNA design; however, it is not suitable for low voltage applications due to its stacking configuration. Since, with the NMOS stacking architecture of the common-source and common gate transistors, relatively large bias voltage is required for transistor biasing, and the performance degrades significantly as the supply voltage decreases. For low-voltage applications, a folded topology is one of the popular structures.

Although source inductive degeneration is one of the popular methods for input impedance matching, it leads to reducing the LNA gain. Therefore, more power should be consumed to compensate the missing gain. In order to increase the power gain, a new input impedance matching called Parallel Inductor (PI) was presented in details by the author in [1]. The source inductor has been removed and the parasitic gate resistance can be converted to 50 Ω by a simple LC matching circuit network.

Considering Fig. 1 (a), the input impedance of the LNA designed with the PI method can be expressed as [1]:

$$Z_{in-PI} = \left(\left(\omega L_{p1}\right)^2 / R_p\right) + j\left(\omega L_{p1} - 1/(\omega C_s)\right) \quad (1)$$

where $R_p = 1/\left(R_{inM}\left(\omega C_{gs}\right)^2\right)$ and C_{gs} and R_{inM} are gate to source

DOI: 10.1587/elex.10.20130557
Received July 16, 2013
Accepted September 04, 2013
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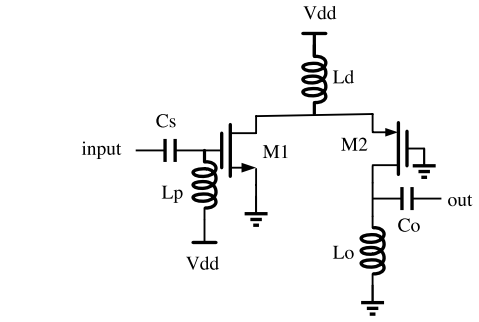
capacitance and parasitic input resistance of MOSFET, respectively. In addition, L_{p1} is the inductance which is seen by C_s when looking towards the LNA. Therefore, when the input of the LNA is matched, one obtains $(\omega L_{p1})^2/R_p=50$, and $\omega L_{p1}=1/(\omega C_s)$, which yields:

$$C_s = C_{gs}\sqrt{\frac{R_{inM}}{50}} \tag{2}$$

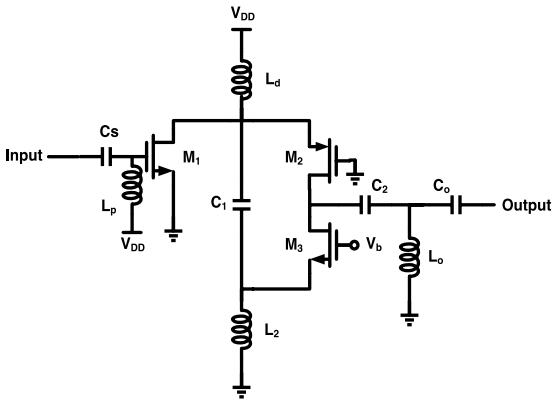
$$L_p = \frac{1}{\omega^2 C_{gs}\left(1+\sqrt{\frac{R_{inM}}{50}}\right)} \tag{3}$$

Moreover, the effective transconductance of transistor M1 can be calculated as [1]:

$$G_{m-PI} = \left|\frac{i_{out1}}{v_{in}}\right| \approx \frac{\omega_T}{50\omega}\sqrt{\frac{50}{R_{inM}}} \tag{4}$$



(a)



(b)

Fig. 1. (a) conventional folded cascode LNA with PI input matching, (b) Proposed folded cascode LNA

Furthermore, as demonstrated in [1], the PI matching technique results in enhancing the LNA gain by 3 dB at the desired frequency band while it consume no extra power. The schematic of a low voltage low power folded cascode LNA based on the PI matching network is shown in Fig. 1 (a).

One of the important parameters that should be considered in the design of the LNA is linearity. The linearity of a low voltage low power LNA is generally degraded by other design limitations, thus linearity improvement techniques should be applied to enhance the linearity. The

DOI: 10.1587/elex.10.20130557
Received July 16, 2013
Accepted September 04, 2013
Publicized October 22, 2013
Copyedited November 10, 2013

main source of nonlinearity of origin in a MOS transistor is the nonlinear transconductance g_m, which converts the linear input voltage to nonlinear output drain current. As can be seen in Fig. 1 (b), a feed forward structure by adding an NMOS transistor (M3) and inductor L2 is utilized in contrast to the conventional folded cascode. Therefore, the output current is obtained from the difference between the drain currents of M2 and M3. The aspect ratio, the bias voltage, and the value of L2 associated with the auxiliary transistor are chosen to tune the magnitude and phase of M3 3rd order intermodulation component, IM3, cancelling the IM3 components generated by the main amplifier causing high linear characteristic of conventional folded cascode. C1 and C2 are coupling capacitors. Since the auxiliary transistor (M3) is added in the second stage of the amplifier, it has a negligible effect on the amplifier's noise figure. Moreover, it does not also dissipate any extra power because of the bias current reusing via M3.

The drain current of the MOSFETS can be expressed with (5) using Taylor series expansion [6]:

$$\begin{aligned} i_d(v_{gs}) =& g_{m1}v_{gs} + g_{d1}v_{ds} + g_{m2}v_{gs}^2 + g_{md1}v_{gs}v_{ds} \\ &+ g_{d2}v_{ds}^2 + g_{m3}v_{gs}^3 + g_{md2}v_{gs}^2v_{ds} \\ &+ g_{md2}v_{gs}v_{ds}^2 + g_{d3}v_{ds}^3 \end{aligned} \tag{5}$$

Here, g_{mx} is the nth-order transconductance nonlinearity coefficient, g_{dx} is the nth-order drain conductance nonlinearity coefficient, and g_{dmx} is the nth-order cross-modulation coefficient. v_{gs} is the gate-to-source voltage, and v_{ds} is the drain-to-source voltage. We neglect the cross modulation coefficients (g_{mdx}), which are very low in a typical MOSFET, and the drain conductance nonlinearity coefficient (g_{dx}), which has a minor effect on IIP3 calculation for simplicity. Consequently, the simplified small signal output current of the proposed LNA which includes the difference between i_{d2} and i_{d3}, can be written as follows:

$$i_{out} = (g_{21} + g_{31})V_{sg2} + (g_{22} - g_{32})V_{sg2}^2 + (g_{23} + g_{33})V_{sg2}^3 \tag{6}$$

where g_{xn} shows the nth-order transconductance nonlinearity coefficient of transistor x. while, $V_{sg2} = V_{sg3}$.

According to (6), it can be shown that the amplifier's total transconductance increases; the IM2 term decreases, as g_{22} and g_{32} have the same sign; and the IM3 term decreases, because g_{23} and g_{33} could have different signs. By properly choosing the circuit parameters such as the transistor's aspect ratio and the biasing voltage, V_b, the optimum criteria could be achieved, where $g_{22} = g_{32}$ and $g_{23} = -g_{33}$, and therefore:

$$i_{out} = (g_{21} + g_{31})V_{sg2} \tag{7}$$

As can be clearly seen from (7), the output current of the proposed LNA is proportional with the first order transconductance of the transistors M2 and M3. Furthermore, the second and third order transconductance nonlinearity coefficients of the transistors M2 and M3 are cancelled.

3 Simulation results

The proposed LNA has been simulated by Advanced Design System (ADS)

DOI: 10.1587/elex.10.20130557
Received July 16, 2013
Accepted September 04, 2013
Publicized October 22, 2013
Copyedited November 10, 2013

simulator using 0.18 μm CMOS process BSIM3 model parameters. All of the elements are implemented on chip. The LNA operates with a 0.6 V power supply and consumes 1.28 mW of DC power. Fig. 2 shows the IIP3 of the LNA before and after linearization. The IM3 of the LNA was simulated by two input tones with 10 MHz offset. It can be verified that the value of IIP_3 is improved by more than 12 dB reaching -1 dBm. At 5 GHz, the linear LNA has noise figure (NF) of 3.5 dB, voltage gain of 12.25 dB, input return loss of -11 dB, and the output return loss of -9 dB. The return loss, S_{12}, is less than -25 dB over the bandwidth.

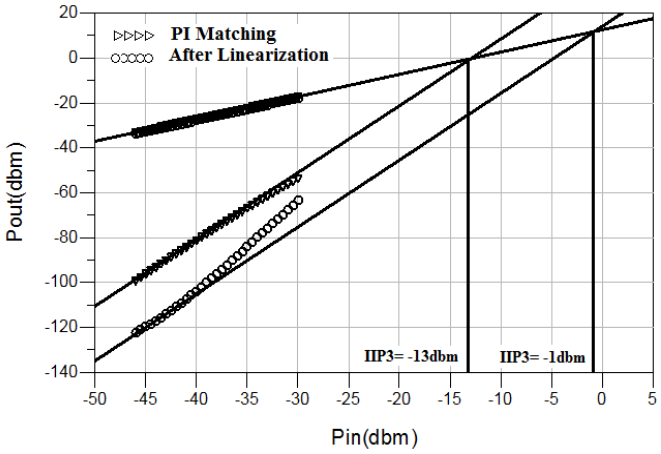


Fig. 2. Simulation results of IIP3 before and after linearization

To evaluate the performance of an ultra low voltage LNAs, different figures of merit (FOMs) are commonly used in the literature such as follow;

$$FOM = \frac{gain(abs).IIP_3(mW)}{(NF-1)(abs).power(mw)} \tag{8}$$

Table I. : comparison results with other published papers, in F_0=5Ghz

Ref.	After linearization	Before linearization	[7]	[8]	[9]	[10]
Tech (µm)	**0.18**	0.18	0.18	0.18	0.18	0.13
Vdd (V)	**0.6**	0.6	0.6	0.6	0.6	0.4
Power(mw)	**1.28**	1.3	0.9	0.8	1.68	1.03
NF(dB)	**3.5**	3.5	4	3.7	3.5	5.3
S_{21}(dB)	**12.25**	12.7	9.5	11.2	14.1	10.3
S_{11}(dB)	**-11**	-9	-15	-18	-17	-17.7
S_{22}(dB)	**-9**	-13	-20	-21	-17	-11.4
FOM	**1.42**	0.093	0.042	0.043	0.033	N/A
IIP_3(dBm)	**-1**	-13	-16	-17.5	-17.1	N/A
Body biasing	**Not used**	Not used	Not used	Used	Used	Used
S/M*	**S**	S	S	S	S	M

* Simulation/Measurement results

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Received July 16, 2013
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Table I represents the summary of the simulation results and comparison with other published papers. The results prove that the proposed technique for linearization of the folded cascode LNAs is very efficient because, NF, gain and also power dissipation that are the most important parameters of LNAs have the same value compared to the conventional folded cascode.

4 Conclusion

A new linearization technique was presented in this paper which is recommended for low voltage LNAs. Due to the reusing of DC current, the proposed method does not consume extra power. According to simulation results, the proposed technique improves IIP3 more than 12 dB without any significant effect on the other parameters such as NF, voltage gain and power dissipation. The gain and NF of the proposed LNA are 12.25 dB and 3.5 dB, respectively. Employing the folded cascode configuration, the fully integrated LNA can operate with small supply voltage of 0.6 V while consuming only 1.28 mW of power. The simulation results show that the proposed LNA is suitable for ultra low power and ultra low voltage applications.

DOI: 10.1587/elex.10.20130557
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