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High Speed Comparator for the Moduli $\{2^n, 2^n-1, 2^n+1\}$

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Abstract: $\{2^n, 2^n-1, 2^n+1\}$ is one of the most commonly used moduli in residue number systems. In this express, we propose a novel comparator for the moduli $\{2^n, 2^n-1, 2^n+1\}$. Based on the proposed architecture, we can design high speed comparator for the moduli $\{2^n, 2^n-1, 2^n+1\}$, which is the fastest among all known comparators for the moduli $\{2^n, 2^n-1, 2^n+1\}$. The performance of the proposed comparator is evaluated and compared with the earlier fast comparators for the moduli $\{2^n, 2^n-1, 2^n+1\}$, based on a simple gate-count and gate-delay model. The proposed comparator can improve the state-of-art by 8% on the average in terms of area and 6% on the average in terms of performance delay.

Keywords: Residue number systems (RNS), comparator

Classification: Integrated circuits

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1 Introduction

Residue number systems (RNS) are a good alternative to the conventional arithmetic, based on a weighted number system. In applications requiring intensive computation, such as digital signal processing [1], the carry free characteristics of RNS allow for concurrent computation in each of the RNS moduli channels. The most common moduli set used in RNS applications is the traditional moduli set $\{2^n, 2^n-1, 2^n+1\}$ [1]. However,

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the comparison operation is very difficult because RNS are non-weighted number systems.

There are several works to address this problem. The method in [2] uses the Chinese Reminder Theorem (CRT) and complex computation to make a comparison. The authors of [3] presented a RNS comparison technique, which performs comparison without using a redundant module and complete converting from RNS to binary systems. The authors of [4] proposed the comparison technique based on sign detection.

In this paper, we propose a new representation for RNS comparison. Based on the new representation for RNS comparison, a novel comparator for the moduli $\{2^n, 2^n-1, 2^n+1\}$ is proposed.

2 New representation for RNS comparison

As is well known, RNS are defined by a set of pairwise relatively prime moduli $\{m_1, m_2, \cdots, m_k\}$ and the legitimate range of the RNS is

$$M_K = \prod_{i=1}^{k} m_i \tag{1}$$

Herein we divide $[0, M_K)$ into two parts: $[0, M_P)$ and $[M_P, M_K)$.

$$M_P = \begin{cases} \dfrac{M_K}{2} & \text{when}(M \textit{ is even}) \\ \dfrac{M_K}{2} - 1 & \text{when}(M \textit{ is odd}) \end{cases} \tag{2}$$

For any integer $X \in [0, M_P)$, there is one and only $M_K - X \in [M_P, M_K)$. Therefore, we can define $M_K - X$ as negative integers. Thus, $[0, M_K)$ is divided into two part: the positive part $[0, M_P)$ and the negative part $[M_P, M_K)$.

3 The proposed comparator

Based on the new presentation for RNS comparison, we can simply compare two residues in RNS by subtracting and converting the final result to binary for comparison.

Assume that the minuend is $A = \{a1, a2, \cdots, ak\}$ and the subtrahend is $B = \{b1, b2, \cdots, bk\}$. The difference D can be given as:

$$D = A - B = \{\langle a1 - b1\rangle_{m_1}, \langle a2 - b2\rangle_{m_2}, \cdots, \langle ak - bk\rangle_{m_k}\} \tag{3}$$

Since $A \in [0, M_P)$ and $B \in [0, M_P)$, there is $D \in [0, M_K)$

Therefore, we can get that

$$\begin{cases} D = 0 & when(A = B) \\ D \in [1, M_P) & when(A > B) \\ D \in [M_P, M_K) & when(A < B) \end{cases} \tag{4}$$

If only we can get the value of D, the comparison result can be achieved.

Let us consider the common used moduli $\{2^n, 2^n-1, 2^n+1\}$. And we have $D = \{d1, d2, d3\}$. The residue value of D can be computed as:

$$\langle d1\rangle_{2^n} = \langle a1 - b1\rangle_{2^n} = \left\langle a1 + \overline{b1} + 1\right\rangle_{2^n} \tag{5}$$

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$$\langle d2\rangle_{2^n-1} = \langle a2 - b2\rangle_{2^n-1} = \langle a2 + \overline{b2}\rangle_{2^n-1} \tag{6}$$

$$\langle d3\rangle_{2^n+1} = \langle a3 - b3\rangle_{2^n+1} \tag{7}$$

(7) can be implemented with the subtracter in [5].

Once $\{d1, d2, d3\}$ is known, the binary value of D can be given as [6]:

$$D = \langle U + V + W - d3\rangle_{2^{2n}-1} \times 2^n + d1 \tag{8}$$

$$U = d1[0]\#d1[n-1:0]\#d1[n-1:1] \tag{9}$$

where $Z[w:v]$ represents bits of Z originally located in positions from v (less significant) to w (more significant) and the symbol $\#$ is used to concatenate bits.

$$V = \overline{d2}[n-1:0]\#\overbrace{1\cdots1}^{nbit} \tag{10}$$

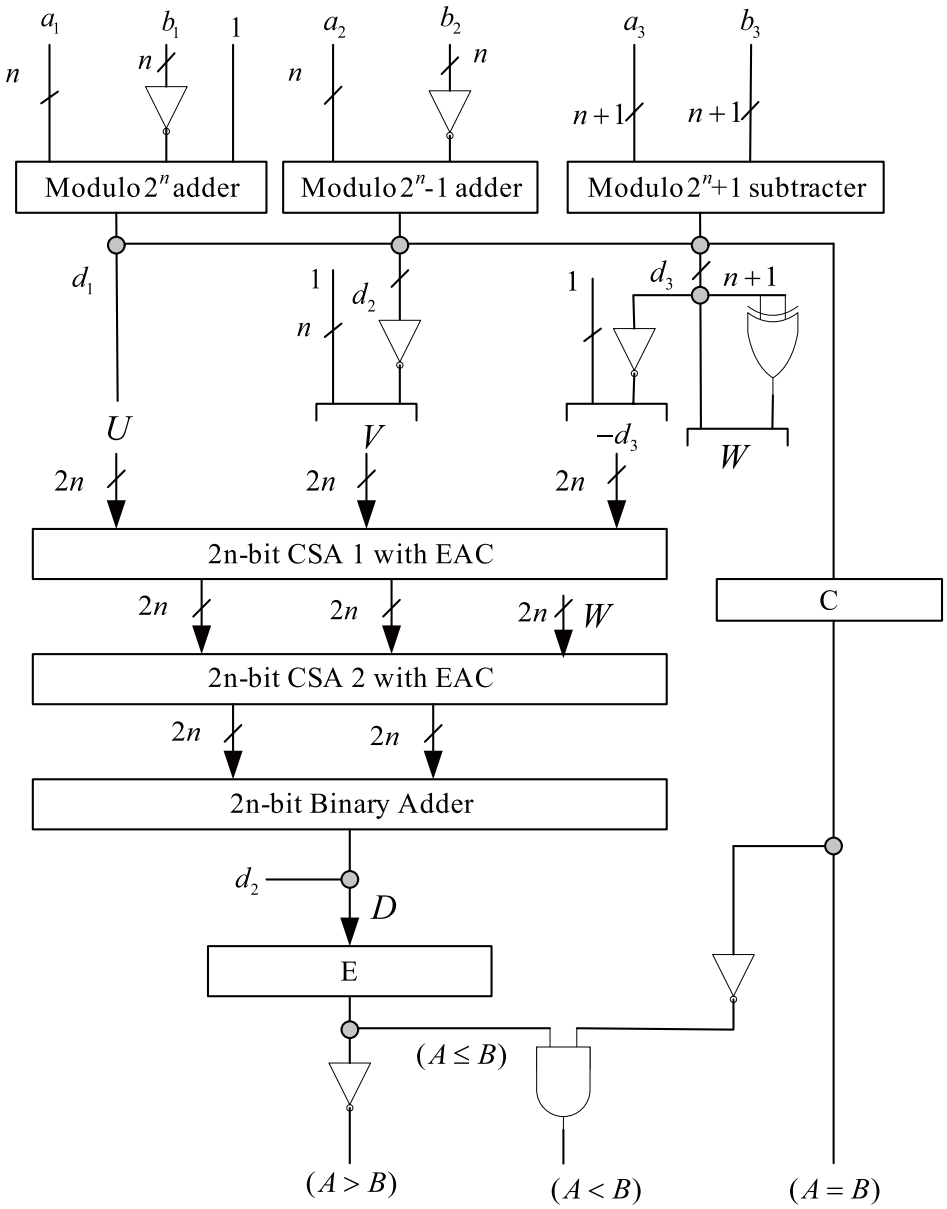

Fig. 1. The proposed architecture for RNS comparison

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$$W = (d3[n] \oplus d3[0])\#d3[n-1:1]\#(d3[n] \oplus d3[0])\#d3[n-1:1] \quad (11)$$

where $\oplus$ denotes XOR.

$$\langle -d3\rangle_{2^{2n}-1} = \overbrace{1\cdots 1}^{(n-1)bit} \#\overline{d3}[n:0] \quad (12)$$

The comparison result $(A = B)$ can be achieved by

$$(A{=}B){=}\overline{d1[n{-}1]{+}\cdots{+}d1[0]{+}d2[n{-}1]{+}\cdots{+}d2[0]{+}d3[n]{+}\cdots{+}d3[0]} \quad (13)$$

Since $M_P = 2^{n-1}(2^{2n}-1) = 0\#\overbrace{1\cdots 1}^{2nbits}\#\overbrace{0\cdots 0}^{(n-1)bits}$, the comparison result $(A \le B)$ can be achieved as:

$$(A \le B) = \overline{D[3n-1] + D[3n-2]\cdot\cdots\cdot D[n-1]} \quad (14)$$

Once $(A = B)$ and $(A \le B)$ are achieved, we can get $(A < B)$ and $(A > B)$ as:

$$(A < B) = \overline{(A = B)} \cdot (A \le B) \quad (15)$$

$$(A > B) = \overline{(A \le B)} \quad (16)$$

Fig. 1 plots the proposed architecture for RNS comparison, where module C and module E are used to implement the logic operations in Eq. (13) and Eq. (14), respectively.

4 Comparison and analysis

In this section, we demonstrate the improved performance of the proposed comparator against the comparators of [3, 4].

Based on the simple gate-count and gate-delay model used in [3, 4], the performance comparison can be listed as:

Unit Gate Delay:

[3]: $4n + \log n + 36$

[4]: $2n + 39$

Proposed: $6\log n + 26$

Unit Gate Area:

[3]: $115n + 186$

[4]: $132n + 55$

Proposed: $6n\log n + \frac{5}{2}(n-1)\log(n-1) + \frac{131}{2}n + 1$

From the above analysis, it can be concluded that the proposed comparator has less latency than that in [3, 4]. The proposed comparator has a very significant delay reduction. Based on the proposed architecture, we can design high speed comparator for the moduli $\{2^n, 2^n-1, 2^n+1\}$, which is the fastest among all known comparators for the moduli $\{2^n, 2^n-1, 2^n+1\}$. In the express, we have shrank the legitimate range of the moduli $\{2^n, 2^n-1, 2^n+1\}$ from $[0, M_K)$ to $[0, M_P)$ and sometimes it is not important. For example, to represent 16-bit binary integers, $n = 6$ will be chosen for the moduli $\{2^n, 2^n-1, 2^n+1\}$. All the 16-bit binary integers will fall into $[0, M_P)$, when $n = 6$.

To demonstrate the efficiency of the proposed comparators, the chosen

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designs for the proposed comparators and the reference comparators were designed in VerilogHDL and implemented using TSMC 90 nm CMOS process technology. The Synopsys Design Compiler tool version Y-2006.06-SP4 was used to get the synthesized results. The obtained results are plotted in Fig. 2 and Fig. 3.

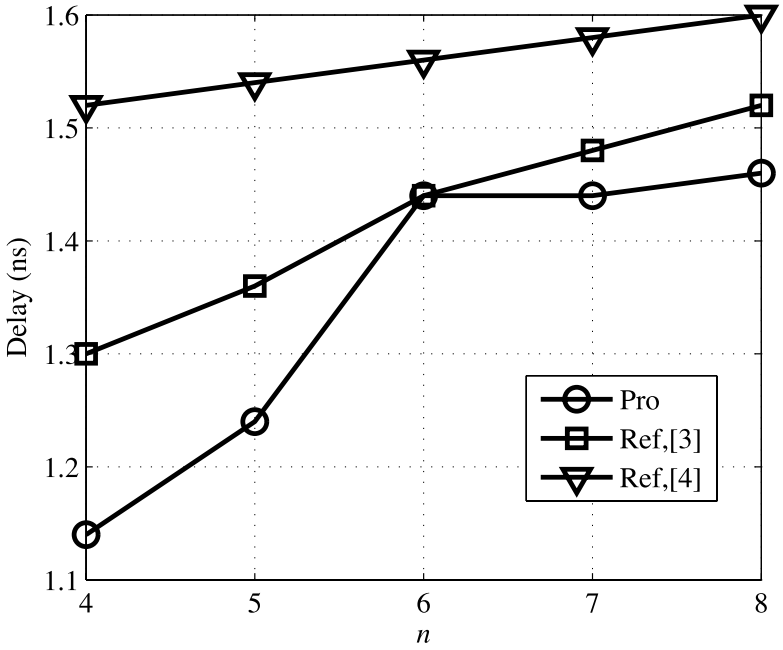

Fig. 2. The delay performance of the proposed comparators and the reference comparators in [3, 4]

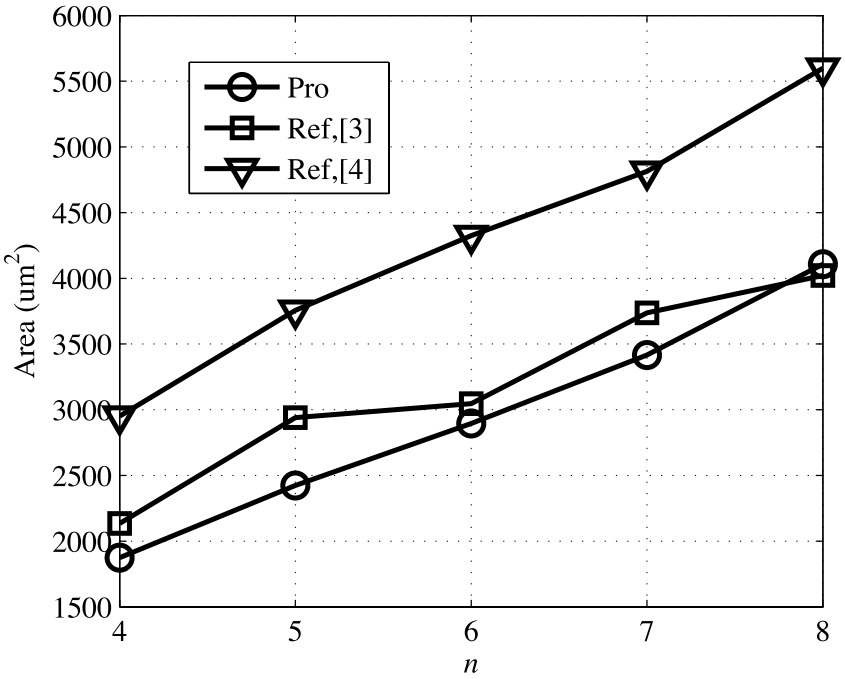

Fig. 3. The synthesized area of the proposed comparators and the reference comparators in [3, 4]

From the synthesized results, it can be concluded that the proposed comparators can achieve an average delay savings of about 6% with an average area saving of 8% against the reference comparators in [3] and

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obtain delay savings of about 8%–25% with an average area saving of 32% against the reference comparators in [4]. Compared with the reference comparators in [3], the synthesized results demonstrate that the proposed comparators need less latency and area overhead.

Compared with the reference comparators in [4], the proposed comparators compare two residues in RNS by subtracting and converting the final result to binary for comparison, reducing two converting logics in the reference comparators in [4] into one converting logic. Based on the new presentation, the proposed architecture is more efficient that in [4], which is shown in the synthesized results.

5 Conclusion

In this express, we propose a novel comparator for the moduli $\{2^n, 2^n-1, 2^n+1\}$. Based on the proposed architecture, we can design high speed comparator for the moduli $\{2^n, 2^n-1, 2^n+1\}$, which is the fastest among all known comparators for the moduli $\{2^n, 2^n-1, 2^n+1\}$. The synthesized results demonstrate that the proposed comparator can improve the state-of-art by 8% on the average in terms of area and 6% on the average in terms of performance delay.

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