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An ultra low power OTA with improved unity gain bandwidth product

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Abstract: An operational transconductance amplifier (OTA) using dynamic threshold MOS (DTMOS) and hybrid compensation technique is presented in this paper. The proposed topology is based on a bulk and gate driven input differential pair. Two separate capacitors are employed for the OTA compensation where one of them is used in a signal path and the other one in a non-signal path. The circuit is designed in the 0.18 μm CMOS TSMC technology. The proposed design technique shows remarkable enhancement in unity gain-bandwidth and also in DC gain compared to the bulk driven input differential pair OTAs. The Hspice simulation results show that the amplifier has a 92 dB open-loop DC gain and a unity gain-bandwidth of 135 kHz while operating at 0.4 V supply voltage. The total power consumption is as low as 386 nW which makes it suitable for low-power bio-medical and bio-implantable applications.

Keywords: ultra low power, ultra low voltage, operational transconductance amplifier, dynamic threshold MOS (DTMOS)

Classification: Integrated circuits

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1 Introduction

As the size of modern CMOS processes scales down, the maximum allowable power supply continuously decreases. The main challenge to implementing low-voltage CMOS circuits is the threshold voltage which does not scale down with the same rate as the power supply. To combat this conflict without requiring the development of expensive CMOS technologies with lower threshold voltages, novel circuit design techniques must be developed that are compatible with future CMOS standard technologies [1].

A promising approach in low voltage analog circuits is the "bulk-driven" MOSFET method. In this method, the gate-source voltage is set to a value sufficient to form an inversion layer, and an input signal is applied to the bulk terminal. In this way, the threshold voltage of a MOSFET can be reduced or even removed from the signal path. One important drawback of the bulk-driven method is that the body transconductance, g_{mb}, is approximately five times smaller than the gate transconductance, g_m, [2] therefore, when the input differential pair of an amplifier is composed of bulk-driven transistors, the resulting DC gain is relatively low.

In this paper, a 0.4 V using weak inversion MOSFETs is presented. A DTMOS technique is used to increase the gain to the level of 92 dB and remarkable enhancement in unity gain-bandwidth.

2 Proposed DTMOS OTA with hybrid compensation

In the standard bulk CMOS technology, it is possible to use the body of PMOS transistors as a fourth terminal to the MOSFET. By changing the absolute value of V_{BS}, the threshold voltage reduces more than 25% [3]. Despite the limitations of using the bulk terminal of a PMOS transistor, the DTMOS technique can have several advantages in low-voltage analog circuits. First, in low-voltage applications there is not much voltage headroom for signal swing, and reducing the threshold voltage can be useful. Second, having a fourth terminal can be advantageous since it can result in a simpler circuit with a fewer number of transistors. Third, the voltage range at the body terminal of a PMOS transistor normally covers the range of voltages which is not covered by the gate of the transistor. Therefore, using the bulk terminal makes it possible to extend the input voltage range of a circuit.

The transconductance in the DTMOS technique is more than that in the bulk driven method, and g_m (DTMOS)=βg_m (BTMOS). β is equal to 1 +(C_d/C_{ox}) and C_d is the depletion dynamic capacitance, and have constant values. The improved DTMOS current drive is due to the following: (1) Inversion charge is increased as [1]:

$$dQ_n = C_{ox}\left(dV_g - \frac{\partial V_t}{\partial V_g}dV_g\right) \tag{1}$$

$$C_{eff} = C_{ox}\left(1 + \left|\frac{\partial V_t}{\partial V_g}\right|\right) \tag{2}$$

Thus, DTMOS leads to an effectively thinner oxide. (2) DTMOS carrier

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mobility is higher because the depletion charge is reduced and the effective normal field in the channel is lowered [1]. We realize that the DTMOS gate capacitance is larger than the regular MOS gate capacitance. However, the gate capacitance and the current drive of DTMOS are much higher than those of regular MOS. Thus, DTMOS gates are expected to switch faster than regular MOS gates. Thus, DTMOS gates are expected to switch faster than regular MOS gates. Obviously, the unity gain bandwidth is proportional to input transconductance [2]; therefore, by applying the DTMOS technique at the input transistors, meaning that bulk and gate are tied together, results in enhancing UGB because of adding g_m to g_{mb}. More explanation about DTMOS technique was presented by authors in [1] and will not be discussed here.

The proposed circuit of OTA using DTMOS technique is shown in Fig. 1 (a). Observe that transistor pairs M_{3a}-M_{3b} and M_{4a}-M_{4b} form the composite transistors. They allow the differential pair active load and the common gate amplifier to be biased by the same potential, without using any additional biasing sources. From the composite transistor equations, it is possible to conclude that V_{DS3a} is given by (3), [5]. An analogous expression is obtained for calculatingV_{DS4a}:

$$V_{DS3a} = \frac{KT}{q}\ln\left(1 + 2\frac{(W/L)_{3b}}{(W/L)_{3a}}\right) \tag{3}$$

In terms of DC analysis, voltages $V_{DS3a}$and $V_{DS4a}$are equal and constant. Therefore, voltages V_{DS1} and V_{DS2} should be equal and constant, thus optimizing matching of the differential pair M_1 and M_2, consequently reducing the differential offset voltage. The dimensions of transistors M_8 and M_9 should be carefully matched in order to avoid the differential pair unbalancing. In order to avoid any systematic offset, it is possible to derive an equation as follows:

$$(W/L)_6 = \frac{2(W/L)_{3a}(W/L)_7}{2(W/L)_8 + (W/L)_5} \tag{4}$$

There will be no systematic offset voltage as long as (4) is satisfied. Although the weak inversion operation implies large transistors dimensions, it minimizes the noise figure, especially reducing flicker noise which is important in a MOS transistor in low-frequency applications. Using small signal analysis, the open loop gain is given by:

$$A_0 = \frac{(g_{m1} + g_{mb1})g_{m6}}{g_{o67}\left(\dfrac{g_{o4b} + g_{o9}}{g_{m4b} + g_{mb4b} + g_{o4b}}g_{o24a} + \dfrac{g_{o11}\cdot g_{o9}}{g_{m11} + g_{mb11}}\right)} \tag{5}$$

Where g_{oi} is output conductance of M_i transistor, and g_{oij} shows parallel conductance of M_i and M_j transistors. As can be clearly seen from (5), thanks to using DTMOS technique, transconductance of input transistors have increased and consequently open loop gain has enhanced.

Obviously, a disadvantage of the Miller frequency compensation technique is the inconvenience of the right half plane (RHP) zero. This RHP zero degrades the phase margin and leads to instability of operational amplifiers.

In this work, the output impedance of the first stage is increased, mainly

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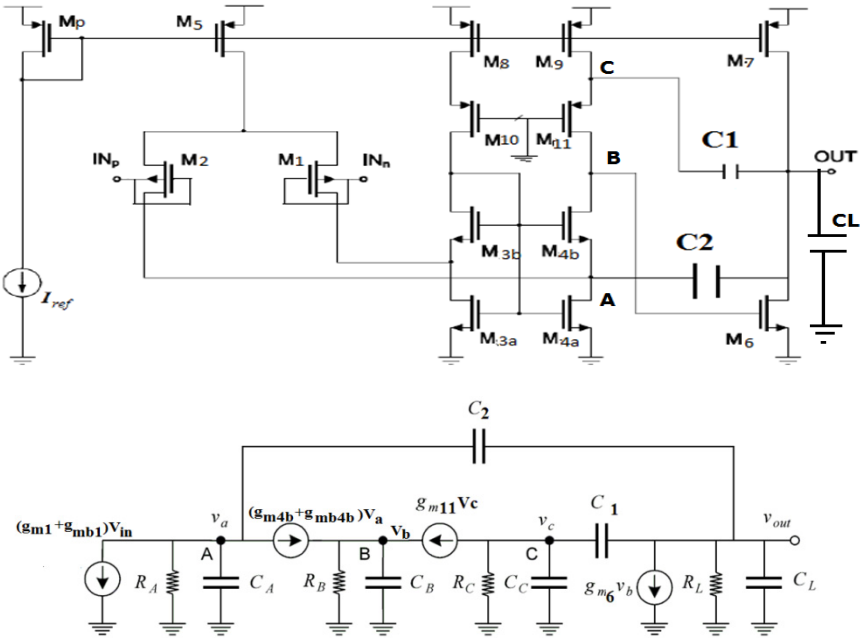

Fig. 1. (a) Schematic of the proposed DTMOS OTA circuit. (b) Small signal equivalent circuit for differential inputs.

thanks to the employed transistor M_{4b}, thus, the DC gain is improved. The unity-gain bandwidth is also enhanced using two gain-stages (common-gate) in the Miller capacitor feedback path. Consequently, the gain-bandwidth product (GBW) is considerably enhanced.

Fig. 1 (a) shows a two-stage OTA composed of folded-cascode as the first stage and the common-source amplifier as the second stage that employs hybrid cascode compensation. As shown in Fig. 1 (a), two separate capacitors, C_2 and C_1, have been used for compensation of the opamp where C_2 is used in a signal path and C_1 in a non-signal path. The small signal equations of the circuit shown in Fig. 1 (b) can be calculated as follows:

$$(g_{m1}+g_{mb1})v_{in}+\frac{v_a}{R_A}+sC_Av_a+(g_{m4b}+g_{mb4b})v_a+sC_2(v_a-v_{out})=0 \tag{6}$$

$$\frac{v_b}{R_B}+sC_Bv_b-(g_{m4b}+g_{mb4b})v_a-g_{m11}v_c=0 \tag{7}$$

$$\frac{v_c}{R_C}+sC_Cv_c+g_{m11}v_c+sC_1(v_c-v_{out})=0 \tag{8}$$

$$g_{m6}v_b+sC_1(v_{out}-v_c)+\frac{v_{out}}{R_L}+sC_Lv_{out}+sC_2(v_{out}-v_a)=0 \tag{9}$$

Where R_A, R_B, R_C, R_L and C_A, C_B, C_C, C_L are the resistances and capacitances which can be seen at the nodes A, B, C, and output, respectively.

After lengthy calculations, the system has three zeros and four poles. The zeros are obtained as follows:

$$s_{z1}=-\frac{g_{m11}}{C_2+C_c} \tag{10}$$

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$$s_{z2,3} \approx \pm\sqrt{\frac{(g_{m4b}+g_{mb4b})g_{m6}}{C_1C_B}} \tag{11}$$

Two zeros are located at the left half plane, and one is located at the right half plane. But, since the right half plane zero is at a high frequency, it does not affect the system stability.

To obtain the dominant real pole, it is assumed that its value is much smaller than the other poles. The poles are obtained as follows:

$$s_{p1} \approx -\frac{1}{(g_{m4b}+g_{mb4b})(C_2+C_1)R_LR_B} \tag{12}$$

$$s_{p2} \approx -\frac{(g_{m4b}+g_{mb4b})g_{m11}(C_2+C_1)}{C_2C_1((g_{m4b}+g_{mb4b})+g_{m11})} \tag{13}$$

$$s_{p3,4} = -\frac{(g_{m4b}+g_{mb4b})C_1(C_2+C_L)+g_{m11}C_2(C_1+C_L)}{2C_LC_2C_1} \pm j\sqrt{\frac{g_{m6}((g_{m4b}+g_{mb4b})+g_{m11})}{C_BC_L}} \tag{14}$$

3 Simulation results

The proposed OTAs are simulated in HSPICE with BSIM3 model based on a standard 0.18 μm CMOS process. Figure 2 (a) shows the simulated open loop gain. The simulation results show a considerable increase in unity-gain bandwidth to the value of 135 kHz, the improved DC gain of 92 dB, and a phase margin of 45°. The presented topology employing DTMOS and weak inversion transistors is capable of working at 400 mV of power supply and consuming only 386 nW. The flicker input referred noise spectral density is 10 nV/$\sqrt{Hz}$.at 10 mHz .The designed system demonstrates relatively suitable response in different process corners. Table I shows a comparison between bulk driven, gate driven and DTMOS operational amplifiers. To evaluate the overall performance of the amplifier, a figure of merit (FOM) can be calculated as follows [1]:

$$\text{FoM} = \frac{(\text{Gain})(\text{Unity gain freq.})}{(\text{Power supply})(\text{Power consumption})}. \tag{15}$$

The proposed architecture shows a noticeable FOM while operating with ultra low supply voltage of 400 mV.

4 Conclusion

Design of a new ultra-low power ultra-low voltage operational transconductance amplifier was presented in this paper. The proposed OTA utilizes DTMOS technique. Simulation results have been presented to confirm the considerable improvement in unity-gain bandwidth and also DC gain, when compared to the bulk driven input differential pair OTA. The simulation results show that the open loop gain of the presented amplifier is equal to 92 dB while achieving unity gain bandwidth of 135 kHz. The total power consumption of the OTA is as low as 386 nW which is much lower

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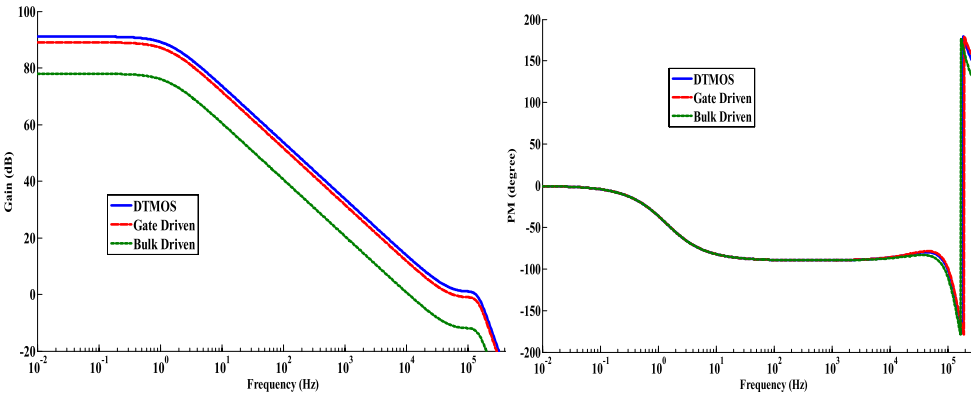

Fig. 2. (a) Simulated open loop gain. (b) Phase margin.

Table I: Comparison of the results of the proposed OTA against other OTAs.

	DTMOS	Bulk Driven	Gate Driven	[1]	[4]	[5]	[6]
Technology (µm)	0.18	0.18	0.18	0.18	0.18	0.35	0.35
V_{dd}(mV)	400	400	400	400	500	600	900
P_{dc}(nW)	386	386	386	386	1020	550	9900
Gain(dB)	92	78	89	92	88.5	73.5	62
UGB(kHz)	135	11	56	114	83.88	13.02	540
Slew Rate(V/ms)	21	20	20.5	21	52	14.7	N/A
C_{Load}(pF)	15	15	15	15	15	15	2.5
FOM(dB.KHz/mV.uW)	80.44	5.55	32.28	66.66	14.47	2.89	3.76
Simulation/Measurement	S	S	S	S	S	S	S

compared to the other existing works. This ultra-low power ultra-low voltage architecture is very useful in bio-medical applications in which the power budget is limited.

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