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# Reconfigurable pseudo-NMOS-like logic with hybrid MOS and single-electron transistors

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**Abstract:** A novel reconfigurable hybrid single electron transistor/MOSFET (SETMOS) circuit architecture, namely, reconfigurable pseudo-NMOS-like logic is proposed. Based on the hybrid SETMOS inverter/buffer circuit cell, reconfigurable pseudo-NMOS-like logics that can work normally at room temperature are constructed. This kind of reconfigurable logic can implement up to $2^n$ sorts of functions at n inputs with different configurations. It only consumes 1 PMOS transistor, 1 NMOS transistor and n SETs, which reduces logic-gate density and power consumption significantly.

**Keywords:** reconfigurable pseudo-NMOS-like logic, hybrid SET and MOSFET element, single-electron transistor, room-temperature

**Classification:** Electron devices, circuits, and systems

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## 1 Introduction

Single-electron transistor (SET) has become one of the promising candidates for very-large-scale-integrated (VLSI) circuits in the post-CMOS period of near future due to their ultra-low power consumption and ultra-small size [1]. However, because the SET fabricated by the current Si nanotechnology still suffered from thermal fluctuation at room temperature [2], a hybrid solution based on SET and MOSFET (SETMOS) becomes a trend for the practical application of the SET [3, 4]. Compared to conventional MOSFETs, the hybrid SETMOS logic circuit have some different characteristics such as the properties of programmable [5] and reconfigurable. The reconfigurable logic based on the hybrid SETMOS has attracted a variety of research groups and many logics have emerged [6, 7]. Nevertheless, most of them concern the simple logic cell, few focus on more complicated universal architecture such as the pseudo-NMOS-like logic based on the hybrid SETMOS, which is similar to the pseudo-NMOS logic based on the pure MOSFETs. Moreover, among the community of the reconfigurable inverter/buffer cell, most of them pay attention to pure SET, few use the hybrid SETMOS cell, which is perhaps an obstacle to the development of the reconfigurable hybrid SETMOS logic circuit.

## 2 Reconfigurable pseudo-NMOS-like architecture

Similar to the pseudo-NMOS logic [8] as shown in Fig. 1 (a), the hybrid SETMOS logic is composed of serial PMOS&NMOS load and pull-down network (PDN) formed by pure SETs. Fig. 1 (b) illustrates the generic structure of an n-input hybrid SETMOS logic element, which is composed of 1 PMOS, 1 NMOS and n SETs. The PMOS connects the NMOS serially, which plays the role of a pull-up load like the PMOS load of the pseudo-NMOS logic and acts as the supply current and voltage. Like H. Inokawa's circuits [9], the NMOS with a fixed gate bias of $V_{ng}$ is used here to keep the SET drain voltage almost constant at $V_{ng}$-$V_{th}$, where $V_{th}$ is the NMOS threshold voltage. The PMOS and the NMOS are set with $W < L$ to attain enough low $V_{ng}$-$V_{th}$ to sustain the Coulomb blockade condition. The n SETs connect in serial or parallel ways with each other and form a PDN to carry out the corresponding function. It is shown that the hybrid SETMOS logic is much like


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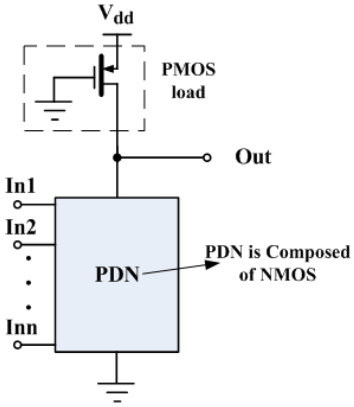
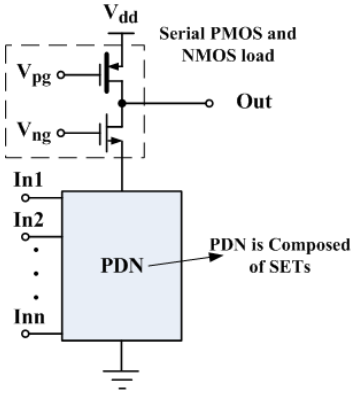
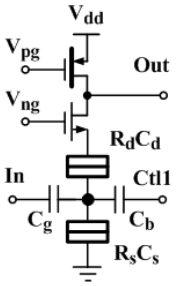


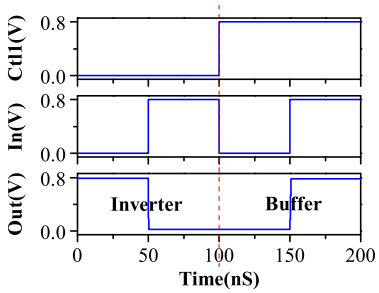

(a) Schematic of Pseudo-NMOS Logic Gate [8]



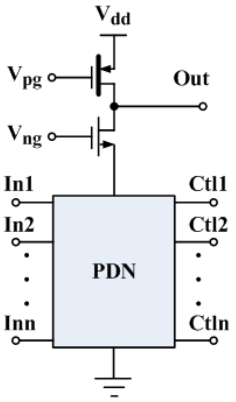

(b) Schematic of Pseudo-NMOS-like Logic Gate Based on Hybrid SETMOS



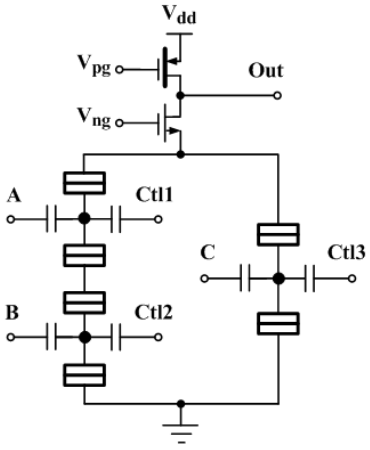

(c) Structure of Reconfigurable Inverter/Buffer Cell




(d) Simulation Results of Reconfigurable Inverter/Buffer Cell




(e) Generic Reconfigurable Pseudo-NMOS-like Logic Architecture: N-input Network




(f) Example: 3-input Parallel&Serial Reconfigurable Logic Element

**Fig. 1.** Reconfigurable Pseudo-NMOS-like Logic Architecture Based on Hybrid SETMOS and Usual Pseudo-NMOS-like Logic Circuits

to the pseudo-NMOS logic not only in form but also in function it performs, therefore, the hybrid SETMOS logic is named pseudo-NMOS-like logic in this letter.

Because of the body-bias ($V_b$) effect [6] of the SET, the phase of Coulomb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oscillation of the SET will shift, especially, the phase will shift apropos a half cycle by adjusting the parameters of the SET. Based on this principle, a hybrid SETMOS reconfigurable inverter/buffer cell is proposed in Fig. 1 (c). The cell is composed of 1 PMOS, 1 NMOS and 1 SET. The PMOS connects the NMOS serially, which plays the role of a pull-up load and acts as the supply current and voltage. The drain node of the SET connects the NMOS, the source node of the SET connects ground directly. The input $In$ connects the gate capacitor $C_g$ of the SET, the control signal $Ctl1$ connects the bias capacitor $C_{ctl}$ of the SET as body-bias voltage, the output $Out$ pulls out from the source node of the PMOS. The parameters of the PMOS are $W = 16\,\text{nm}$, $L = 48\,\text{nm}$, $V_{pg} = 0.4\,\text{V}$ and $V_{dd} = 0.8\,\text{V}$. The parameters of the NMOS are $W = 16\,\text{nm}$, $L = 32\,\text{nm}$ and $V_{ng} = 0.4\,\text{V}$. The parameters of the SET are where $C_d = C_s = 0.05\,\text{aF}$, $C_g = C_b = 0.1\,\text{aF}$, $R_d = R_s = 150\,\text{k}\Omega$. The simulation model and circumstance are exactly the same to the ones in section 3, and the simulation temperature is 300K. Especially, according to the temperature and the parameters of the SET, $E_c = \frac{e^2}{C_\Sigma} = 533\,\text{meV} = 20.5k_BT > 10k_BT \gg k_BT$, where $C_\Sigma$ is the overall capacitance of the SET and $k_B$ is the Boltzmann's constant, namely, the charge energy of the SET is much larger than the available thermal energy to avoid disturbance of the external heat source on the entire the SET at room temperature. It indicates that our proposed circuits accord with the requirements [1] of the SET for working normally and the macromodel [10] completely, i.e., our proposed circuits can work normally at room temperature.

Fig. 1 (d) shows the detailed timing diagram of the reconfigurable inverter/buffer cell, the time variations of the control signal $Ctl1$, the input signal $In$ and the output signal $Out$ are given by the first, second and third panel, respectively. According to the body-bias effect, if control signal $Ctl1$ is biased with 0 V ($gnd$), namely, $Ctl1$ = "0", the SET in the cell is in Coulomb blockade and the cell switch is off when $In$ is "0", and then $Out$ is "1"; the SET in the cell is in the conduction state and the cell switch is on when $In$ is "1", and then $Out$ is "0"; in such circumstances, the cell operates as a inverter. If control signal $Ctl1$ is biased with 0.8 V ($V_{dd}$), namely, $Ctl1$ = "1", the SET in the cell is in the conduction state and the whole cell switch is on when $In$ is "0", and then $Out$ is "0"; the SET in the cell is located Coulomb blockade and the cell switch is off when $In$ is "1", and then $Out$ is "1"; in such circumstances, the cell operates as a buffer. In conclusion, this cell can be configured as a inverter or buffer by just adjusting the voltage of $Ctl1$.

Based on pseudo-NMOS-like logic and the reconfigurable inverter/bffer cell, we propose a reconfigurable pseudo-NMOS-like logic architecture which includes n-input any parallel&serial hybrid logic as shown in Fig. 1 (e) and Fig. 1 (f). Fig. 1 (e) illustrates the generic structure of n-input reconfigurable pseudo-NMOS-like logic element, which is only added n control lines based on pseudo-NMOS-like logic element to obtain more functions in the same circuit, and it can obtain up to $2^n$ functions in a circuit and will reduce area enormously. Fig. 1 (f) shows a concrete example of the generic structure, namely, a 3-input reconfigurable parallel&serial hybrid pseudo-NMOS-like


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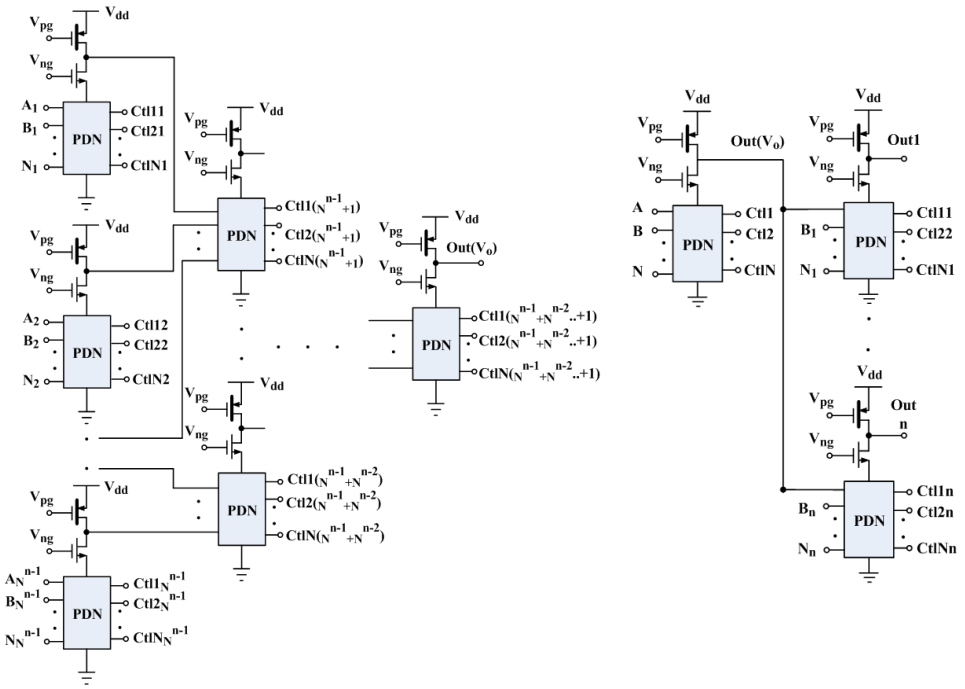
logic element. In this element, the PDN comprises 3 SETs, two of them connect each other serially, and then connect the third one in parallel, which can represent any form of a n-input network. The structures and parameters of PMOS, NMOS and SET are exactly the same to the inverter/buffer cell. According to the theory of the pseudo-NMOS logic, the outputs of this 3-input reconfigurable element should be as follows:

if "$Ctl1\ Ctl2\ Ctl3$"="000", $Out=\overline{A\cdot B+C}$;
if "$Ctl1\ Ctl2\ Ctl3$"="001", $Out=\overline{A\cdot B+\overline{C}}=\overline{A\cdot B}\cdot C$;
if "$Ctl1\ Ctl2\ Ctl3$"="010", $Out=\overline{A\cdot \overline{B}+C}=(\overline{A}+B)\cdot\overline{C}$;
if "$Ctl1\ Ctl2\ Ctl3$"="011", $Out=\overline{A\cdot \overline{B}+\overline{C}}=(\overline{A}+B)\cdot C$;
if "$Ctl1\ Ctl2\ Ctl3$"="100", $Out=\overline{\overline{A}\cdot B+C}=(A+\overline{B})\cdot\overline{C}$;
if "$Ctl1\ Ctl2\ Ctl3$"="101", $Out=\overline{\overline{A}\cdot B+\overline{C}}=(A+\overline{B})\cdot C$;
if "$Ctl1\ Ctl2\ Ctl3$"="110", $Out=\overline{\overline{A}\cdot \overline{B}+C}=(A+B)\cdot\overline{C}$;
if "$Ctl1\ Ctl2\ Ctl3$"="111", $Out=\overline{\overline{A}\cdot \overline{B}+\overline{C}}=(A+B)\cdot C$.

In addition, driving capability is a key parameter of a logic device and should be considered. Generally, driving capability have two aspects, one is the driving capability of multi-level structure, the other is the driving capability of multi-fan-out structure. For investigating the driving capability of the reconfigurable pseudo-NMOS-like logic, we design multi-level and multi-fan-out structures. Fig. 2 (a) shows the n-level reconfigurable pseudo-NMOS-like logic element based on the representative N-input reconfigurable pseudo-NMOS-like logic gate, which is comprised of $(N^{n-1}+N^{n-2}+\cdots+1)$ N-input reconfigurable pseudo-NMOS-like logic gates. The first level have




(a) Multi-level Reconfigurable Pseudo-NMOS-like Circuit

(b) Multi-fan-out Reconfigurable Pseudo-NMOS-like Circuit

**Fig. 2.** Two Typical Reconfigurable Pseudo-NMOS-like Circuits for Testing The Driving Capability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$N^{n-1}$ N-input reconfigurable pseudo-NMOS-like logic gates, $N^n$ inputs and $N^{n-1}$ outputs, then the outputs of the first level act as the inputs of the second level, and so on. Finally, the $(N^{n-1} + N^{n-2} + \cdots + 1)$ N-input reconfigurable pseudo-NMOS-like logic gates form the n-level reconfigurable pseudo-NMOS-like logic element. Fig. 2 (b) shows a N-input reconfigurable pseudo-NMOS-like logic gate with n fan-out N-input reconfigurable pseudo-NMOS-like logic gates. The structures and parameters of PMOS, NMOS and SET in the multi-level and multi-fan-out circuits are exactly the same to the inverter/buffer cell.

## 3 Experiments and discussion

SET-based circuits are normally simulated using the Monte Carlo-based method such as SIMON [11] and SECS [12], however, these simulators are extremely time consuming for large circuit simulations and does not offer a cosimulation environment with MOSFET devices. A compact macromodel [10] based on SPICE method, whose correctness and precision have been verified by both Monte Carlo simulator SIMON [11] and other simulation experiments [13], can be used to co-simulate the hybrid SETMOS circuit effectively. Thus, throughout this letter, the compact macromodel is used for SETs and the BSIM4.0 model is used for MOSFETs, and all simulations are conducted using SPICE simulator of Synopsys Inc based on the 16-nm CMOS technology.

Fig. 3 shows the detailed timing diagram of this 3-input reconfigurable

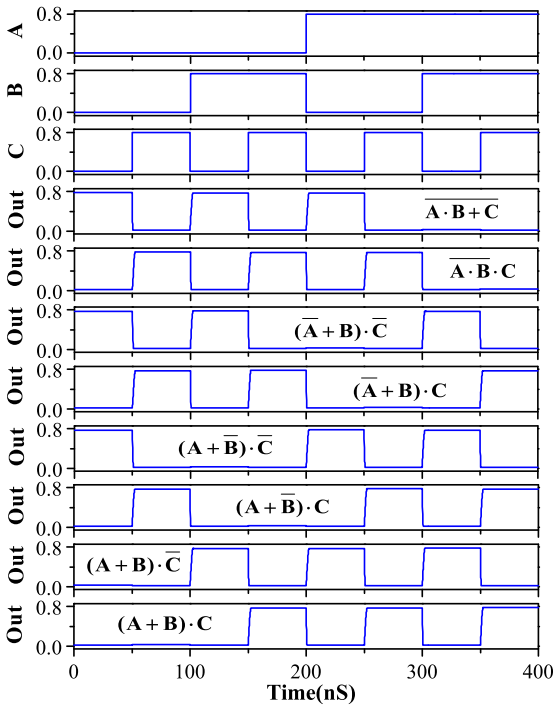


**Fig. 3.** Simulation Results of the 3-input Reconfigurable Parallel&Serial Hybrid Pseudo-NMOS-like Logic Element. The Simulation Temperature Is 300K


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pseudo-NMOS-like logic element, the top three panels indicate time variation of the input signals $A$, $B$ and $C$. From the 4th to the 11th panel, the element achieve the functions of "$\overline{A \cdot B + C}$", "$\overline{A \cdot B} \cdot C$", "$(\overline{A}+B) \cdot \overline{C}$", "$(\overline{A}+B) \cdot C$", "$(A+\overline{B}) \cdot \overline{C}$", "$(A+\overline{B}) \cdot C$", "$(A+B) \cdot \overline{C}$" and "$(A+B) \cdot C$" when "$Ctl1$ $Ctl2$ $Ctl3$" is set to "000", "001", "010", "011", "100", "101", "110" and "111", respectively. From Fig. 3, it is obvious that the simulation results are consistent with the analysis in section 2.

To evaluate the reconfigurable logic elements, we investigate several intrinsic parameters such as function, power, delay and voltage swing of these cells, and the effect of temperature ($T$) variation, simulation results are shown in Table I (a). The delay is calculated by $t_p = (t_{pLH}+t_{pHL})/2$ [8], the power is calculated using $P_{total} = P_{static}+P_{dynamic} = V_{dd}I_{total}+C_L V_{dd}^2 f_{0\to1}+\sum\{(V_d - V_s)I_{static}+[(-V_s \int_0^{3\tau} i_{bottom}dt - \frac{1}{2}C_{Ls}V_{sout}^2)|_{t=3\tau}+(V_d \int_0^{3\tau} i_{top}dt - \frac{1}{2}C_{Ls}V_{sout}^2)|_{t=3\tau}] f_{0\to1}\}$ [8, 14], and the frequency is set to 10 MHz. These elements may have longer delay than that of a common MOSFET circuit, however, it is more area&power efficient, and significantly increases the number of functions. Thus, this longer delay is acceptable. Generally, the circuits based on the pure MOSFETs can work normally at 233∼358K, which is the range of industrial standard temperature. We investigate the effect of 2 limit temperatures such as 240K and 360K to guarantee the reconfigurable pseudo-NMOS-like circuits we propose can work normally at the range of industrial standard temperature and will be compatible with the existing MOSFETs technology. As shown in Table I (a), the voltage swing will decrease when the temperature increases, and the delay will increase when the temperature increases. Especially, the power dissipation will decrease when the temperature increases, which contradicts to the usual CMOS circuits. However, it is consistent with the trend of the power of the pseudo-NMOS circuits because our proposal circuits and pseudo-NMOS circuits are the same type ones.

We simulate and analyze the voltage swings of the 1, 2, 3 and 8 level logic circuits as shown in Fig. 2 (a) which are made up of the 3-input reconfigurable parallel&serial hybrid pseudo-NMOS-like logic element as shown in Fig. 1 (f) when it implements different functions such as "$\overline{A \cdot B + C}$", "$\overline{A \cdot B} \cdot C$", "$(\overline{A}+B) \cdot \overline{C}$", "$(\overline{A}+B) \cdot C$", "$(A+\overline{B}) \cdot \overline{C}$", "$(A+\overline{B}) \cdot C$", "$(A+B) \cdot \overline{C}$" and "$(A+B) \cdot C$", respectively. Table I (b) shows the voltage swings of the 1, 2, 3 and 8 level reconfigurable pseudo-NMOS-like circuits, which demonstrates that the voltage swing of every level keep constant. In the same way, we simulate and analyze the voltage swings of the 1, 2, 3 and 8 fan-out logic circuits as shown in Fig. 2 (b) which are made up of the same 3-input reconfigurable parallel&serial hybrid pseudo-NMOS-like logic element when it implements the eight different functions. Table I (c) shows the voltage swings of the 1, 2, 3 and 8 fan-out reconfigurable pseudo-NMOS-like circuits, which demonstrates that the voltage swing of the 1, 2, 3 and 8 fan-out logic gates keep constant. The reason is that the on or off state of the reconfigurable pseudo-NMOS-like logic is decided by the input signals, while the voltage swing is decided by the Corresponding PMOS, NMOS, SET in the reconfigurable pseudo-NMOS-like


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**Table I.** Evaluation of Reconfigurable Pseudo-NMOS-like Logic Gates, and The Comparisons with Other Different Technology

(a) Performance of Reconfigurable Inverter/buffer Cell, 3-input Reconfigurable Parallel&Serial Element, and The Effect of Temperature ($T$) Variation

| Type | Ctl1 | Ctl2 | Ctl3 | Function | $T$ = 300K | | | $T$ = 240K | | | $T$ = 360K | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Power (nW) | Delay (nS) | $V_o/V_i$ (%) | Power (nW) | Delay (nS) | $V_o/V_i$ (%) | Power (nW) | Delay (nS) | $V_o/V_i$ (%) |
| Inverter /Buffer | 0 | - | - | $\overline{IN}$ | 8.12 | 0.53 | 96.38 | 12.78 | 0.32 | 96.75 | 7.80 | 0.66 | 95.00 |
| | $V_{dd}$ | - | - | $IN$ | 8.15 | 0.53 | | 12.82 | 0.32 | | 7.83 | 0.66 | |
| 3-input reconfigurable hybrid logic element | 0 | 0 | 0 | $\overline{A \cdot B + C}$ | 9.86 | 0.53 | 94.25 | 15.71 | 0.32 | 94.63 | 9.25 | 0.70 | 93.13 |
| | 0 | 0 | $V_{dd}$ | $\overline{A \cdot B} \cdot C$ | 9.91 | 0.53 | | 15.76 | 0.32 | | 9.28 | 0.68 | |
| | 0 | $V_{dd}$ | 0 | $(\overline{A} + B) \cdot \overline{C}$ | 9.86 | 0.53 | | 15.71 | 0.31 | | 9.24 | 0.67 | |
| | 0 | $V_{dd}$ | $V_{dd}$ | $(\overline{A} + B) \cdot C$ | 9.89 | 0.53 | | 15.75 | 0.32 | | 9.27 | 0.70 | |
| | $V_{dd}$ | 0 | 0 | $(A + \overline{B}) \cdot \overline{C}$ | 9.87 | 0.54 | | 15.71 | 0.32 | | 9.25 | 0.68 | |
| | $V_{dd}$ | 0 | $V_{dd}$ | $(A + \overline{B}) \cdot C$ | 9.89 | 0.50 | | 15.74 | 0.28 | | 9.27 | 0.67 | |
| | $V_{dd}$ | $V_{dd}$ | 0 | $(A + B) \cdot \overline{C}$ | 9.90 | 0.54 | | 15.75 | 0.32 | | 9.28 | 0.70 | |
| | $V_{dd}$ | $V_{dd}$ | $V_{dd}$ | $(A + B) \cdot C$ | 9.91 | 0.53 | | 15.75 | 0.32 | | 9.28 | 0.70 | |

(b) Voltage Swings of Multi-level Reconfigurable Pseudo-NMOS-like Circuits

| Function | $V_o/V_i$ of N Levels | | | |
|---|---|---|---|---|
| | 1 | 2 | 3 | 8 |
| $\overline{A \cdot B + C}$ | 94.25 | | | |
| $\overline{A \cdot B} \cdot C$ | | | | |
| $(\overline{A} + B) \cdot \overline{C}$ | | | | |
| $(\overline{A} + B) \cdot C$ | | | | |
| $(A + \overline{B}) \cdot \overline{C}$ | | | | |
| $(A + \overline{B}) \cdot C$ | | | | |
| $(A + B) \cdot \overline{C}$ | | | | |
| $(A + B) \cdot C$ | | | | |

(c) Voltage Swings of Multi-fan-out Reconfigurable Pseudo-NMOS-like circuits

| Function | $V_o/V_i$ of N Fan-out | | | |
|---|---|---|---|---|
| | 1 | 2 | 3 | 8 |
| $\overline{A \cdot B + C}$ | 94.25 | | | |
| $\overline{A \cdot B} \cdot C$ | | | | |
| $(\overline{A} + B) \cdot \overline{C}$ | | | | |
| $(\overline{A} + B) \cdot C$ | | | | |
| $(A + \overline{B}) \cdot \overline{C}$ | | | | |
| $(A + \overline{B}) \cdot C$ | | | | |
| $(A + B) \cdot \overline{C}$ | | | | |
| $(A + B) \cdot C$ | | | | |

(d) Comparison of Power, Delay and Area of 3-input Logic Element Based on Different Technology, The Simulation Temperature Is 300K

| Function | Power (nW) | | | Delay (nS) | | | Area | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | No. of MOSFETs | | | No. of SETs and control line | | |
| | CMOS | Pseudo-NMOS | This work | CMOS | Pseudo-NMOS | This work | CMOS | Pseudo-NMOS | This work | CMOS | Pseudo-NMOS | This work |
| $\overline{A \cdot B + C}$ | 18.18 | 689.70 | 9.86 | 0.001 | 0.005 | 0.53 | 6 | 4 | 2 | 0 | 0 | 3 |
| $\overline{A \cdot B} \cdot C$ | 39.47 | 710.80 | 9.91 | 0.002 | 0.004 | 0.53 | 8 | 6 | | | | |
| $(\overline{A} + B) \cdot \overline{C}$ | 39.22 | 710.70 | 9.86 | 0.001 | 0.004 | 0.53 | 8 | 6 | | | | |
| $(\overline{A} + B) \cdot C$ | 63.57 | 464.40 | 9.89 | 0.005 | 0.023 | 0.53 | 10 | 8 | | | | |
| $(A + \overline{B}) \cdot \overline{C}$ | 39.14 | 710.70 | 9.87 | 0.001 | 0.006 | 0.54 | 8 | 6 | | | | |
| $(A + \overline{B}) \cdot C$ | 63.65 | 464.40 | 9.89 | 0.003 | 0.012 | 0.50 | 10 | 8 | | | | |
| $(A + B) \cdot \overline{C}$ | 64.01 | 464.70 | 9.90 | 0.005 | 0.024 | 0.54 | 10 | 8 | | | | |
| $(A + B) \cdot C$ | 42.60 | 443.50 | 9.91 | 0.004 | 0.019 | 0.53 | 8 | 6 | | | | |
| Total area | | | | | | | 68 | 52 | 2 | 0 | 0 | 3 |

(e) Comparison of Devices, Control Lines and Functions of N-input Logic Element Based on Different Technology (No Consideration for *NOT* Signal)

| Type | No. of MOSFETs | No. of SETs | No. of control line | No. of function |
|---|---|---|---|---|
| Non-Reconfigurable element with CMOS [8] | 2n | 0 | 0 | 1 |
| Non-Reconfigurable element with pseudo-NMOS [8] | n+1 | 0 | 0 | 1 |
| Non-Reconfigurable element with hybrid SETMOS [15] | 1 | n | 0 | 1 |
| Reconfigurable element with pure MOS (Programmable Array Logic) [16] | 26n | 0 | 2n | n |
| Reconfigurable element with hybrid SETMOS (This work) | 2 | n | n | $2^n$ |


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logic element and the $V_{dd}$. It means that the voltage swing of the element is constant when the parameters of the PMOS, NMOS and SET and the $V_{dd}$ are determined. In all, it indicates that the reconfigurable pseudo-NMOS-like logic we propose has outstanding driving capability, which can be used in very large scale integration without side-effect of driving capability and doesn't need additional amplifier.

To compare our work with the CMOS logic and the pseudo-NMOS logic based on pure MOSFET, we investigate the key performance parameters in terms of power dissipation and area. We use the same technology, namely, a 16-nm MOSFET transistor to simulate the behavior of the MOSFET transistors with eight kinds of logics such as "$\overline{A \cdot B + C}$", "$\overline{A \cdot B} \cdot C$", "$(\overline{A} + B) \cdot \overline{C}$", "$(\overline{A} + B) \cdot C$", "$(A + \overline{B}) \cdot \overline{C}$", "$(A + \overline{B}) \cdot C$", "$(A + B) \cdot \overline{C}$" and "$(A + B) \cdot C$". All logic gates are simulated at the same condition as foregoing mention in this section. For better comparison, the parameters of the PMOS are $W = 32\,\text{nm}$, $L = 16\,\text{nm}$ and the parameters of the NMOS are $W = 16\,\text{nm}$, $L = 16\,\text{nm}$ in all CMOS logics. The parameters of the PMOS are $W = 16\,\text{nm}$, $L = 48\,\text{nm}$ and the parameters of the NMOS are $W = 16\,\text{nm}$, $L = 16\,\text{nm}$ in all pseudo-NMOS logics. The parameters of PMOS, NMOS and SET in the pseudo-NMOS-like logics are exactly the same to the inverter/buffer cell described in section 2. The power dissipation and the area are simulated as shown in Table I (d).

As far as power dissipation is concerned, it can be seen that the value of the reconfigurable pseudo-NMOS-like logic we propose is about 1/5 of the CMOS logic and about 1/59 of the pseudo-NMOS logic when implementing the same function. With regard to the area, to implement all the 8 functions, the CMOS logic uses up 68 MOSFETs, the number for the pseudo-NMOS logic is 52, while our logic only consumes 2 MOSFETs, 3 SETs, and 3 control lines.

Obviously, our proposed reconfigurable pseudo-NMOS-like logic architecture can be extended to any n-input reconfigurable pseudo-NMOS-like logic circuit, which can achieves $2^n$ functions by only using 1 PMOS, 1 NMOS and n SETs. Table I (e) shows comparison of devices, control lines and functions of such logic element based on different technologies. One can see that our hybrid SETMOS structure is more area&power efficient.

## 4 Conclusion

In this letter, a novel reconfigurable pseudo-NMOS-like logic architecture based on hybrid SETMOS is proposed. A representative 3-input logic element on the basis of this architecture is illustrated at room temperature, and its power, delay and voltage swing are evaluated. This architecture can be extended to any n-input reconfigurable pseudo-NMOS-like logic, and each logic element can implement up to $2^n$ kinds of functions with different configurations by only using 1 PMOS, 1 NMOS and n SETs, which significantly reduces area and power consumption. The reconfigurable pseudo-NMOS-like architecture can be applied to applications such as functional memory


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systems, FPGAs, etc.

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