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A MASH 1-1-1 ΔΣ time-to-digital converter based on two-stage time quantization

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Abstract: A MASH 1-1-1 ΔΣ time-to-digital converter (TDC), based on two-stage time quantization, was designed with a 0.13 μm CMOS process and a 1.2 V supply. A classical delay line and a Vernier delay line were used for coarse and fine quantization, respectively. Third-order noise-shaping was achieved using the proposed MASH 1-1-1 ΔΣ modulator. Simulation results showed that a resolution of up to 5.5 ps and a measurement range of 38.4 ns could be achieved. The proposed TDC consumes 4.9 mW and occupies 0.28 mm^2.

Keywords: time-to-digital converter, MASH sigma-delta modulator, noise shaping, high resolution

Classification: Integrated circuits

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1 Introduction

High-resolution time-to-digital converters (TDCs) have recently become the focus of research because they are critical building blocks in digital phase-locked loops (DPLLs). Replacing the phase detector (PD) and charge pump (CP) used in a conventional phase-locked loop (PLL), TDCs measure and digitize the phase difference between a reference clock and a feedback clock. Similar to other sampling circuits, TDCs inevitably generate quantization errors while digitizing the phase differences or time intervals. Quantization errors caused by limited TDC resolution cause the deterioration of the in-band DPLL noise [1].

For a TDC used in a DPLL, higher resolution gives the benefits of

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decreased quantization errors and in-band noise [1]. TDCs based on a Vernier delay line (VDL) [2] and time amplifiers (TAs) [3, 4] are usually used to achieve sub-gate resolution. However, limited TDC resolution still causes quantization errors using both of the methods described above. Measurement methods based on a gated ring oscillator (GRO) [1] and a ΔΣ modulator [5] have some attraction in that they can allow noise shaping using difference operations on the quantization error. The quantization noise can be pushed from a low frequency to a high frequency and then filtered using a low-pass filter. In-band noise performance is thereby largely improved. The methods described in references [1] and [5] use an oscillator to digitize the input time interval and use capacitors to hold the oscillator phase between measurements. Large capacitors cannot be used in the method described here because a large capacitance lowers the oscillator frequency and worsens the TDC resolution, while smaller capacitors are susceptible to parasitics, debasing the precision. The mismatch between capacitors in a differential pair and the mismatch between the comparator delays both reduce the accuracy. Additionally, the Vernier method has the advantages of simplicity and first-order tolerance to the process, voltage, and temperature (PVT) variances, which the methods described in references [1] and [5] do not have.

Here we present a MASH 1-1-1ΔΣTDC based on two-stage time quantization. A classical delay line and a Vernier delay line were respectively used for coarse and fine quantization. A MASH 1-1-1ΔΣ modulator was used to compensate for quantization errors. High resolution and third-order noise-shaping were achieved simultaneously.

2 Proposed MASH 1-1-1ΔΣTDC

2.1 Structure of the ΔΣ TDC

Fig. 1 shows the proposed MASH 1-1-1ΔΣTDC, which uses a two-stage TDC for time measurement, an error selection circuit to amplify the correct quantization error, a MASH 1-1-1ΔΣmodulator to achieve third-order noise shaping, and an encoder to output the digitized time interval. The first-stage delay-line TDC comprises 512 delay units, with a coarse resolution of 75 ps, and the second-stage VDL-TDC has 16 delay units, giving a fine resolution of up to 5.5 ps. According to the VDL-TDC outputs, the error selection circuit searches for the first zero–one transition and outputs the corresponding quantization error that has been amplified by the TA [3]. The proposed ΔΣ modulator uses a PD, a CP, and a capacitor to convert the quantization error Δt into a corresponding voltage, and to achieve error compensation. The VDL-TDC outputs are encoded in binary and added to the ΔΣ modulator output to form the TDC output Dout.

2.2 Analysis of the proposed ΔΣ modulator

The first-order error-compensation modulator is shown in Fig. 2a. The PD senses the quantization error Δt caused by the two-stage TDC, and controls CP1 to charge the capacitor. Δt is thus converted into a corresponding voltage. The comparator output takes a value of one when the error integral is beyond Vref, otherwise the output is zero. The comparator output Derror1, which is also the error-compensation modulator output, controls a buffer and a PD, for discharging the capacitor.

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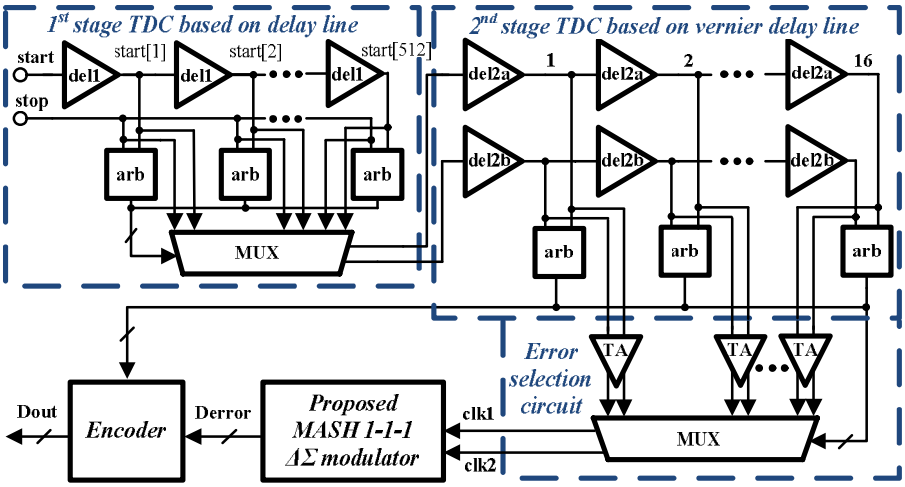

Fig. 1. Structure of the proposed MASH 1-1-1 ΔΣ TDC

The error integral will be decreased by a voltage of Vref after one discharge. The reference voltage Vref is generated by converting the amplified VDL-TDC time resolution using the same PD and CP, as shown in Fig. 2a. In this design, all the CPs have the same current, 80 μA, and all the TAs have a gain of 70. The capacitance is up to 1 pF, to reduce the influence of parasitics.

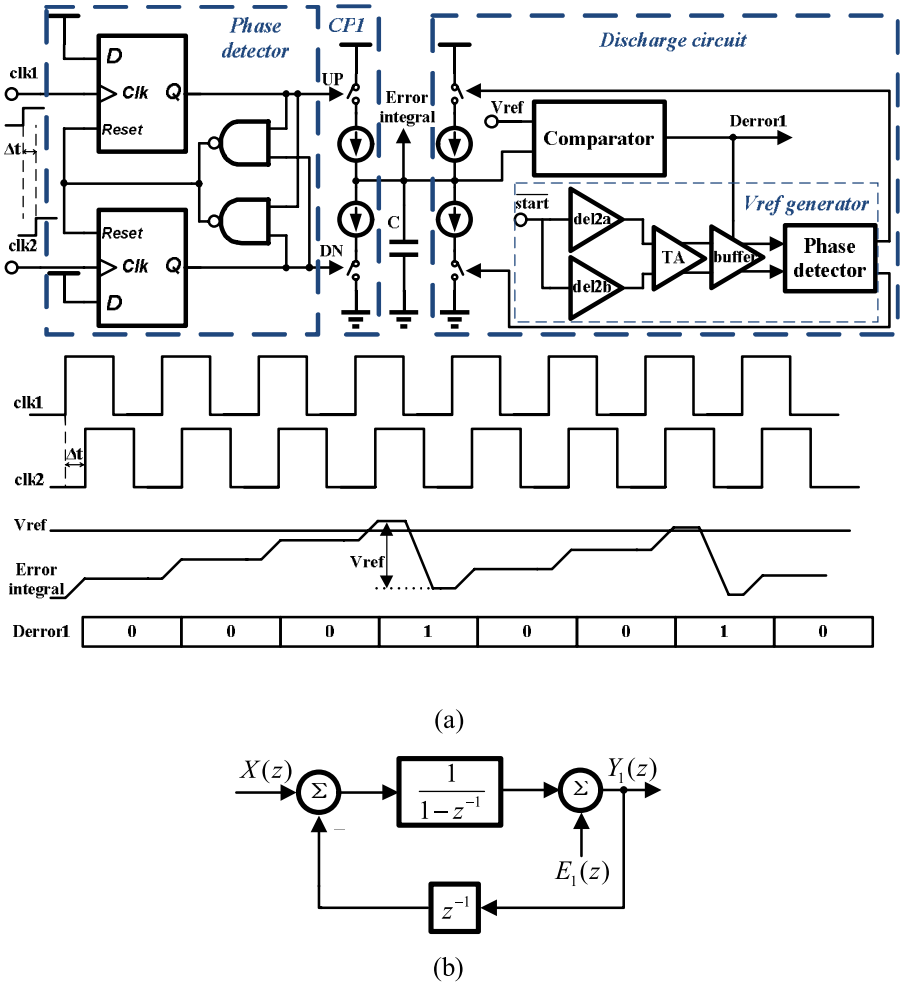

Fig. 2. (a) Structure and timing diagram of the first-order error-compensation modulator, and (b) a model of the first-order error-compensation modulator

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The error-compensation modulator model is shown in Fig. 2b, and this is also a first-order ΔΣ modulator. The output of the modulator is

$$Y_1(z) = X(z) + E_1(z)(1 - z^{-1}), \tag{1}$$

where $E_1(z)$ is the quantization error. In this design, $E_1(z)$ is the difference between the error integral and Vref. First-order noise shaping is therefore achieved through a first-order differential operation on the quantization error.

A MASH 1-1-1ΔΣ modulator that gives higher order noise shaping can be formed by cascading two identical ΔΣ modulators that are part of a first-order error-compensation modulator, as shown in Fig. 3a. Unity-gain buffers are used in the second and third stages to isolate the capacitors in the different stages. The capacitors and discharge circuit are the same as that used in first stage, shown in Fig. 2a. An error neutralization block in

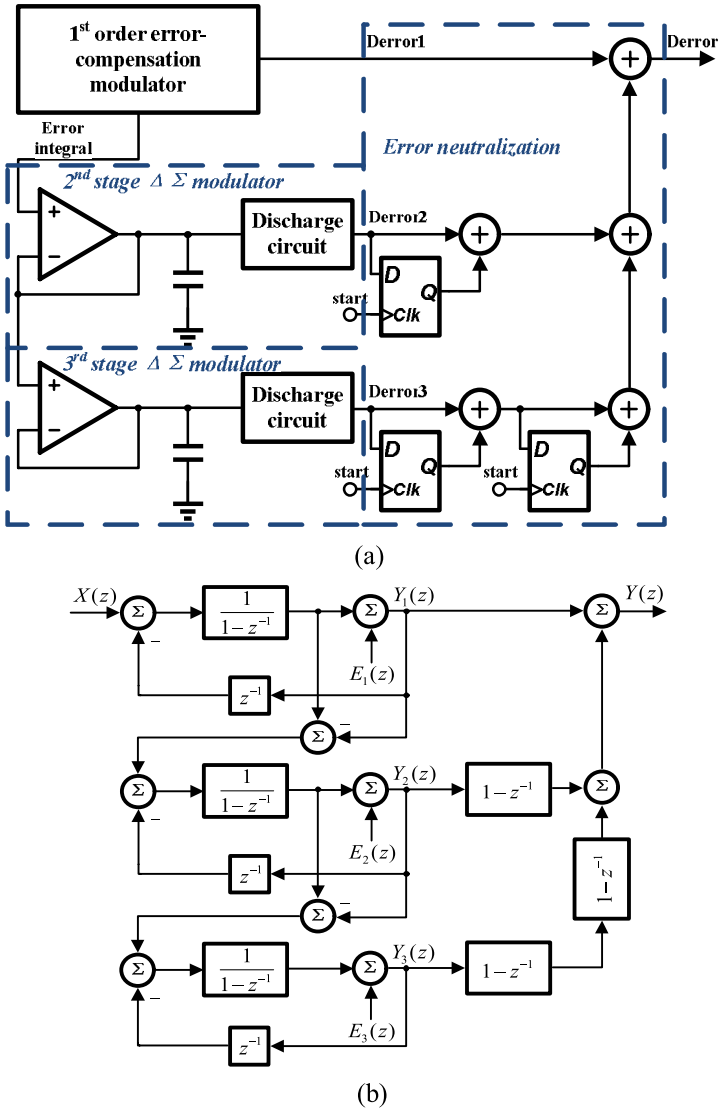

Fig. 3. (a) Structure of the proposed MASH 1-1-1 ΔΣ modulator, and (b) a model of the proposed MASH 1-1-1 ΔΣ modulator

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the digital circuit follows the three stages. The proposed MASH 1-1-1 ΔΣ modulator model is shown in Fig. 3b. The signal that contains the quantization error from the previous stage is fed into the next stage and the error is neutralized by digital processing. The MASH 1-1-1 ΔΣ modulator output is

$$Y(z) = X(z) + E_3(z)\left(1 - z^{-1}\right)^3, \tag{2}$$

where $E_3(z)$ is the quantization error in the third stage. The output only depends on the input and third-order quantization error. In addition, a higher (or lower) order modulator can be formed by cascading more (or fewer) of the same ΔΣ modulators.

3 Simulation results

The proposed MASH 1-1-1 ΔΣ TDC was designed in a TSMC 0.13 μm CMOS process with a 1.2 V supply. The TDC transfer characteristics are shown in Fig. 4. The TDC achieved a resolution of up to 5.5 ps and a measurement range of up to 38.4 ns. The error between the simulation and post simulation was less than 7%, which indicates that the circuit had good immunity to parasitic effects. A 41 kHz sinusoidal signal with a 0.55 ps peak–peak amplitude (corresponding to 0.1 LSB, as shown in Fig. 5b) was added to a DC level of about 110.7 ps, as the input, and the sampling rate was 41 MS/s. A 65,536-point FFT was performed with a Hanning window, and this is shown in Fig. 5a.The simulation results agreed well with third-order noise shaping. The time domain TDC output, after being digitally low-pass filtered with a 400 kHz bandwidth, is shown in Fig. 5b. The input signal with third-order noise shaping was resolved after filtering, and an oversampling ratio of 51 was achieved. The proposed TDC is applicable to PLLs with<2 MHz loop band widths. The circuit consumes 4.9 mW and occupies 0.28 mm^2. The performance of the proposed TDC is summarized and compared with the performance of other systems in Table I.

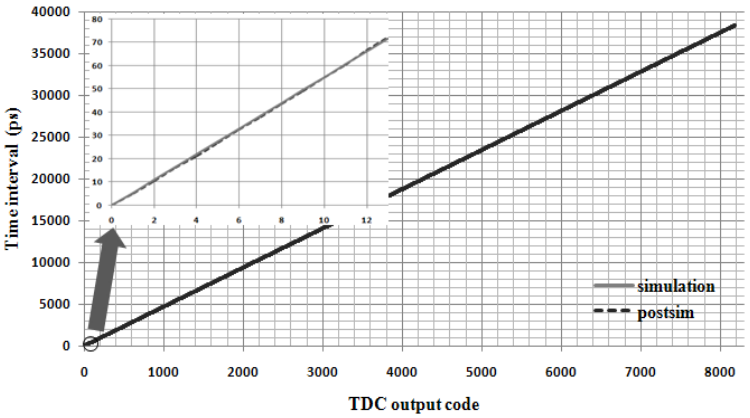

Fig. 4. The proposed time-to-digital converter (TDC) transfer characteristics

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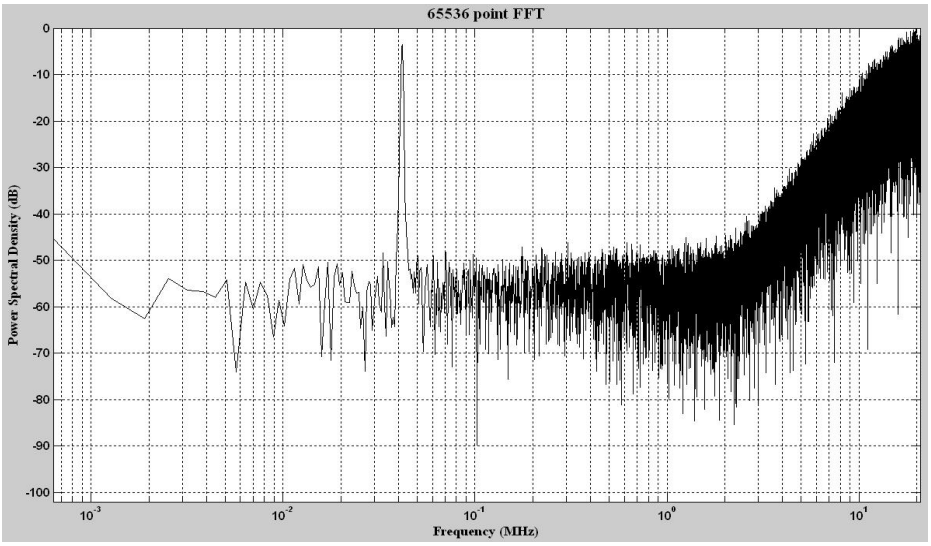
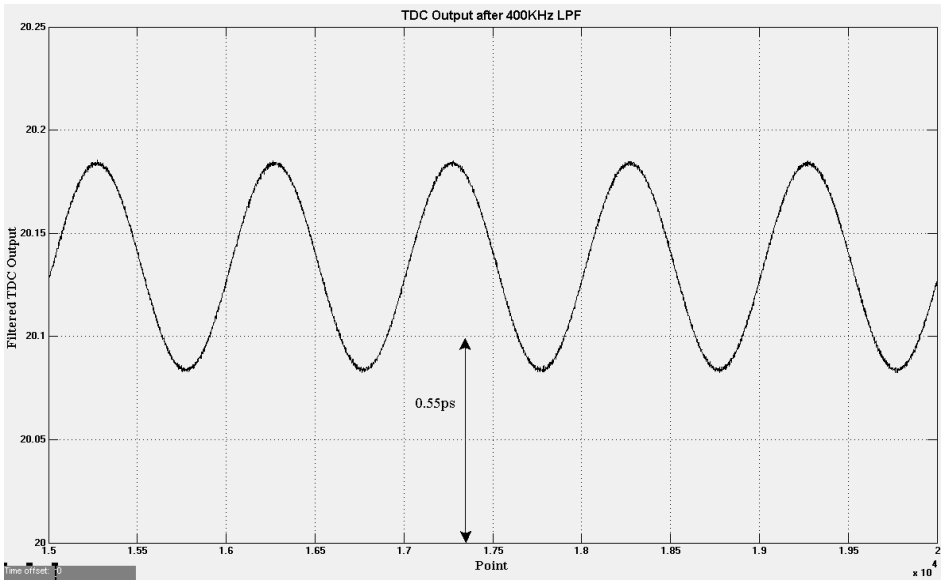


(a)



(b)

Fig. 5. (a) The time-to-digital converter (TDC) output spectrum, and (b) the TDC output waveform

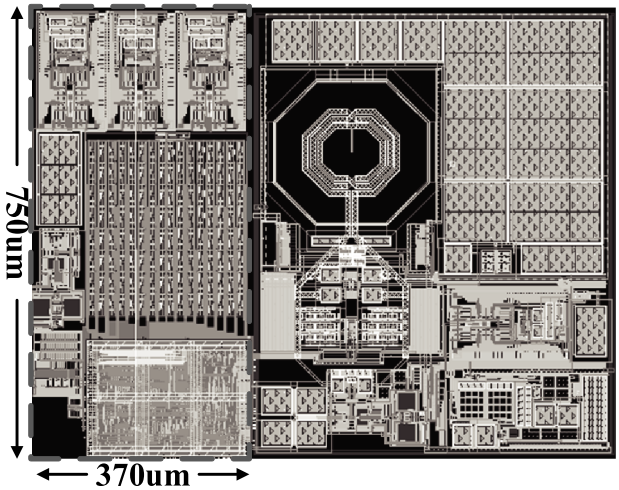


Fig. 6. Layout of the proposed MASH 1-1-1 ΔΣ modulator

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Table I. Comparison of time-to-digital converters (TDCs) with similar specifications

	[1]	[2]	[3]	[4]	[5]	This work
Method	GRO	TA	TA	VDL	MASH ΔΣ	MASH ΔΣ
Resolution (ps)	6	1.25	1.89	8	5.6	5.5
Bits	11	9	8	12	11	13
Meas. Range (ns)	12	0.64	0.5	32	20	38.4
Noise shaping	1st order	N/A	N/A	N/A	3rd order	3rd order
Power (mW)	2.2-21	3	N/A	7.5	1.7	4.9
Area (mm^2)	0.04	0.6	1.4	0.26	0.11	0.28
Process(μm)	0.13	0.09	0.18	0.13	0.13	0.13

4 Conclusions

An 11 bit MASH 1-1-1ΔΣTDC with two-stage time quantization is presented here. A classical delay line and a Vernier delay line were used for coarse and fine quantization, respectively. The resolution was 5.5 ps and the measurement range was 38.4 ns. Third-order noise-shaping was achieved using the MASH 1-1-1 ΔΣ modulator. Increasing (or decreasing) the order of this TDC structure can easily be achieved by cascading more (or fewer) ΔΣ modulators with the same structure.

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