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A resistance matching based self-testable current-mode R-2R digital-to-analog converter

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Abstract: This paper presents a resistance matching based self-testable current-mode R-2R Digital-to-Analog Converter (DAC). The Built-In Self-Test (BIST) circuits are employed to observe the current redistributions in the resistance matching branches converted from the R-2R network in the DAC, and then the redistributed currents are transformed to voltages to detect the R-2R network with extra Design For Testability (DFT) circuits. The circuit-level simulation of the proposed BIST system are presented to demonstrate the feasibility with fault coverage of 96% for R-2R network and 82.6% for the Operational Amplifier (OpAmp), and area overhead of approximately 6%.

Keywords: built-in self-test, resistance matching, design for testability, digital-to-analog converter

Classification: Integrated circuits

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1 Introduction

In analog BIST applications, analog stimuli like sine wave and ramp signal,

are commonly employed to excite the faulty circuit under test. Due to high fault coverage, more than one stimulus is always required in many cases, as a result the high test cost caused by the analog multi-stimulus generator would limit the analog BIST application. In addition, the on-chip generators should also be tested to make sure they can generate the expected test stimuli.

DAC can generate different analog output as stimuli, but it should also be tested. Conventionally, the characteristics like DNL and INL were measured to test DAC, but the extra response-processing circuits and complex on-chip stimulus generator caused large area overhead. Thus, these specification-oriented testing of the analog circuits results in high costs and doesn't ensure detection of all defects, causing potential reliability problems [1]. Therefore, several fault-based BIST schemes have been proposed as an alternative testing method, targeted here for the detection of manufacturing defects. In [2], a fault-based testing strategy was investigated by observing the power supply current in the digital section of the DAC-Under-Test (DUT), and the voltage and bias current in the analog section. However, it is not suitable for self-test. The presented fault-based BIST scheme in [3] employed a pattern counter to continuously generate stimulus patterns feeding to the DUT, and a comparator to compare the responses with the gold reference generated by an adaptive ramp generator. The output binary combination of pattern counter would increase exponentially with resolution increase. Therefore, a fully testable current-mode R-2R DAC is presented as an analog stimuli generator for analog BIST application base on the resistance matching based BIST technique.

2 The resistance matching based test strategy

Figure 1 shows an N-bit current-mode R-2R network, which is constituted by the vertical resistors R_{N-1}~R_0 and the related equivalent resistors $R_{r(N-1)}$~R_{r0} looking toward the right-hand end of the ladder. For node N_i, the vertical resistance including R_i and the RON of S_i, should be equal to R_{ri}, so the binary-weighted R-2R network can be constituted to convert the binary input "$d_{(N-1)}$~d_0" to an equivalent analog signal by controlling the switches $S_{(N-1)}$~S_0. The two branches connected to each node are called resistance matching branches in this work.

When test current I_T is fed to the binary-weighted R-2R network through the node $N_{(N-1)}$ shown in Fig. 1, the currents flowing through R_{N-1}~R_0 can be written as

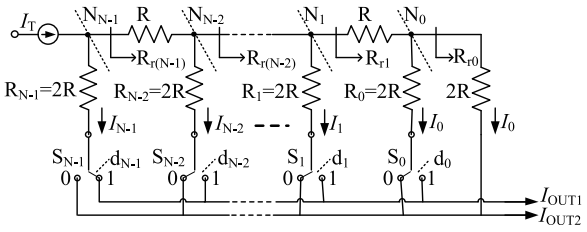

Fig. 1. The general R-2R network.

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$$I_{N-1} = \frac{I_T}{2}, I_{N-2} = \frac{I_T}{4}, \cdots, I_0 = \frac{I_T}{2^N} \quad (1)$$

If d_i is logic '1', the current I_i flows into I_{OUT1}, otherwise I_{OUT2}. When "d_{N-1}~d_0" is set to "10~0", the currents flowing into $I_{OUT1}$and I_{OUT2} should be equal. Once a physical defect happened, the equivalent resistances of the resistance matching branches would become unequal, so the redistributed currents flowing into I_{OUT1} and I_{OUT2} can be monitored to detect the possible defects in the R-2R network by setting "d_{N-1}~d_0" to "10~0".

In order to intuitively explain the resistance matching test strategy, the OpAmp in the DAC is not shown in Fig. 1 and tested by checking the stable output of the transient response [4] through converting the DUT into a voltage follower.

3 The implementation of the resistance matching based BIST technique

3.1 The testable current-mode R-2R DAC with DFT circuits

Figure 2 shows the circuit configuration of an 8-bit current-mode R-2R DAC and its DFT circuits, DFT_1~DFT_4 were designed to implement the resistance matching based test strategy. I_T is the test current, and V_T is the test voltage reference.

Compared with the general R-2R network shown in Fig. 1, the horizontal R resistors were replaced by a parallel combination of two $2R$ resistors, which were separately connected to an analog switch. The injected analog switches S_{t7}~S_{t0} could not only improve the resistance matching of the R-2R network, but also further divide the network into 8 pairs of resistance matching branches from node N_7 to N_0.

S_i is composed of two Transmission Gates (TGs), which conduct alternatively depending on d_i, so in order to excite the possible defects in each TG, "$d_{(i-1)}$~d_0" must be alternatively set to "10~0" and "01~1". However, when "$d_{(i-1)}$~d_0" is set to "01~1", the currents flowing into V_{in1} and

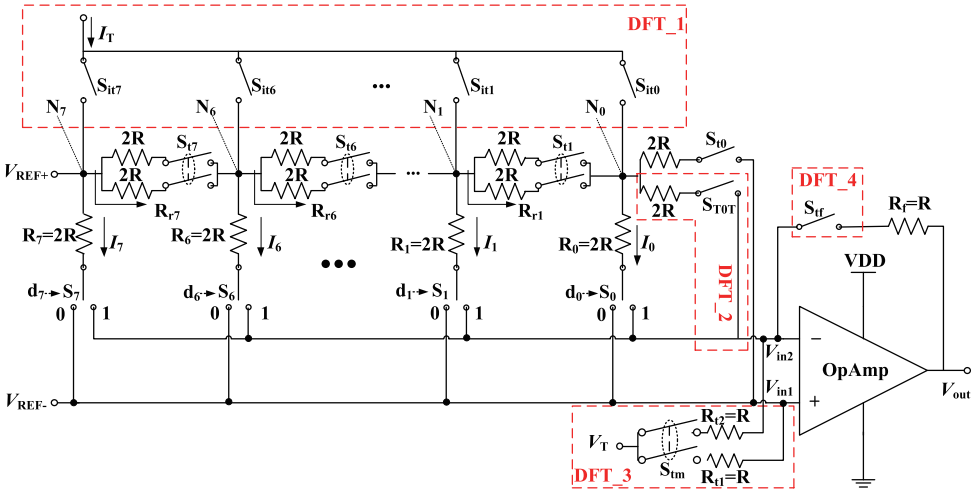

Fig. 2. The circuit configuration of the 8-bit current-mode R-2R DAC with its DFTs.

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V_{in2} become unequal due to the current flowing through S_{t0} could not flow into V_{in2}. Therefore, a parallel branch of a $2R$ resistor connected to S_{T0T} in DFT_2 was added to pass the current to V_{in2}.

When S_{t7}~S_{t0} and S_{it7} are closed, I_T is reduced equally into the resistance matching branches of R_7 and R_{r7} through node N_7. If S_{t7} is turned off, the resistor network is divided into two parts, the left and right parts of node N_6. Then, by closing switch S_{it6}, I_T flows into node N_6 and is equally reduced into the new resistance matching branches of R_6 and R_{r6}. Similarly, by turning S_{ti} off and closing $S_{it(i-1)}$, I_T should flow into the new branches of R_i and R_{ri} through node N_{i-1}. As a result, the possible defects happened in the right-hand of the R-2R network cause larger resistance mismatch, and the enlarged current difference between the two matched branches make the defects be more easily detected in the related lower resistance matching branches. The switches in DFT_1 were design to pass I_T to each test node N_{i-1} based on the dividing of S_{ti}. When the resistor network was divided by turning S_{ti} off, the left part of node N_{i-1} lost its function, only $d_{(i-1)}$~d_0 need be carefully set to force I_T to equally flow into V_{in1} and V_{in2}.

3.2 Test implementation

Owing to the circuit configuration shown in Fig. 2, the currents flowing through the resistance matching branches can not be directly monitored, so the currents are firstly transformed to voltages, and then the voltages are observed to determine the R-2R network test result.

By closing S_{tm} and opening S_{tf}, the DUT is converted into the R-2R network test mode shown in Fig. 3 (a). R_{ib} and R_{ri} represents the two resistance

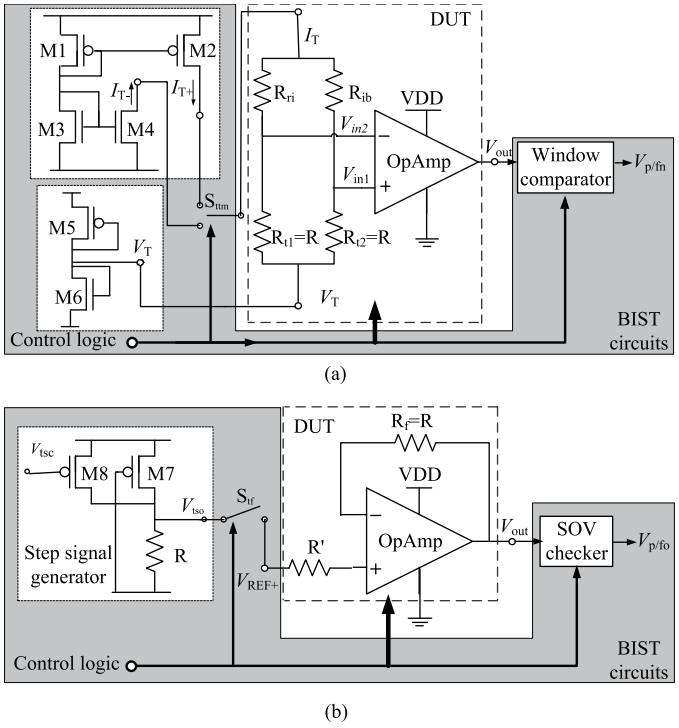

Fig. 3. The proposed test system: (a) The R-2R network test mode. (b) The OpAmp test mode.

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matching branches of node N_i. R_{ib} represents the equivalent resistance of the vertical branch including resistor R_i and the RON of S_i. I_T flows into R_{ib} and R_{ri}, and creates two voltage at V_{in1} and V_{in2} based on the test resistors (R_{t1} and R_{t2}) and V_T. I_T is generated by the complementary test currents generator, which is comprised of the transistors from M1 to M4, and can generate two currents I_{T+} and I_{T-} to excite the possible defects in S_{t7}∼S_{t0}. By switching S_{ttm}, I_{T+} and I_{T-} are alternately passed to I_T to excite the defects in the two transistors of each TG, because the positive/negative test current just flows through one transistor in the TG in some cases. V_T is generated to constrains the voltages at V_{in1} and V_{in2} within the input common-mode range of the OpAmp used in the DUT. Under the R-2R test mode, the OpAmp works as a comparator to recognize the voltage difference between V_{in1} and V_{in2}.

In addition, the proposed R-2R DAC can be reconfigured as a voltage follower shown in Fig. 3 (b) by opening S_{it7}∼S_{it0}, S_{tm} and S_{T0T}, closing S_{tf} and S_{t7}∼S_{t0}, and setting "$d_{(i-1)}$∼d_0" to "0∼0". The possible defects in the OpAmp can be detected by checking the stable output of the transient response. R' represents the equivalent resistance of the R-2R network under the OpAmp test mode.

Figure 3 depicts the system architecture of the proposed test technique for the R-2R DAC. The stimuli generators, the output analyzer including a window comparator and a SOV checker [4], and the control logic were designed to implement the proposed BIST system. The first stage test signatures $V_{p/fn}$ and $V_{p/fo}$ generated by the window comparator and the SOV checker were combined to generate the final test result $V_{p/f}$.

4 Simulation results and discussions

In this work, two classes of device-level faults were considered: catastrophic faults of shorts and opens in MOS transistors, resistors and capacitors, and parametric faults of resistance variation of the R-2R network. Gate-drain short, gate-source short, drain-source short, resistor short and capacitor short, were modeled by connecting a 100 Ω resistor between each pair of terminals. Opens were modeled by inserting a parallel combination of a 100 MΩ resistor and a 10 fF capacitor. Particularly, gate open was modeled by means of grounded parallel combination of resistor and capacitor at the two disconnecting terminals [5].

An 8-bit R-2R DAC has been designed as an example to evaluate the proposed test technique, using Rohm CMOS 0.18-μm technology. The circuit was simulated using HSpice. The resistor R and the aspect ratios of the transistors in the R-2R network shown in Fig. 2, were set to 100 KΩ and 0.54/0.18 μm (W/L), respectively. Particularly, the aspect ratios of the transistors used in S_{tf} were set to 1.2/0.18 μm to optimize the performance of the DAC. S_{tf} must be injected into the left side of R_f to eliminate the RON variation caused by the varying V_{out}. The OpAmp used in the DUT is a buffered OpAmp.

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The complementary test current generator creates a source current I_{T+} of approximately 8.9 μA and a sink current I_{T-} of approximately $-8.9\,\mu$A, and V_T is approximately 0.9 V. If V_{tsc} is logic high, the output V_{tso} is approximately 0.606 V, otherwise 1.202 V.

The designed BIST system can detect 384 faults of the possible 400 catastrophic faults in the R-2R network, resulting in the fault coverage of 96%. The undetected faults are the pMOS gate opens in S_{t7}~S_{t0} and S_{T0T}, because they cause a little resistance change due to the parallel design. Under the OpAmp test mode, 127 catastrophic faults were injected, and 105 faults were finally detected with the fault coverage of approximately 82.6%. The main hard-detected faults exist in the cascode current mirrors, since the current mirrors can still provide an almost constant current even some faults happened. Additionally, the parametric faults of the resistance variation were also considered, and more than 2 KΩ variation in each 100 kΩ resistor could be detected.

The physical layout shows that the DFT and BIST circuits of an 8-bit R-2R DAC caused approximately 6% area overhead of the original DAC.

To research the effects of the DFT and BIST circuits, the integral nonlinearity (INL) and differential nonlinearity (DNL) characteristics are simulated. The injected analog switches in the horizontal branches shown in Fig. 2 reduced the maximum |INL| and |DNL| of the general R-2R DAC from 1.078 LSB to 0.232 LSB, and from 0.334 LSB to 0.206 LSB, respectively. Comparing with the DAC shown in Fig. 2, the inclusion of the BIST circuits of the proposed testable R-2R DAC doesn't degrade the INL and DNL characteristics.

Table I compares the proposed BIST technique with other existing BIST techniques. Most existing techniques employed ramp signals as testing stimulus, and need 2^N digital input codes. The cost test time is $2^N T_{clk}$, and in-

Table I. Comparisons of the proposed test technique with other related BIST techniques, $\star$=Not Reported.

Test strategy	BIST circuits	Test time	Technology\ Area overhead\ Fault coverage
Static testing [6]	N-bit counter, sample-and-hold, and error amplifier	$2^N T_{clk}$	1.2-μm \ 6% \ $\star$
INL calculating [7]	Digital ramp generator and sigma-delta modular	$2^N T_{clk}$	$\star$ \ $\star$ \ $\star$
Parametric testing [2]	Built-in current and voltage sensors	$\star$	$\star$\ $\star$ \ Short faults 96.9%
Performace measuring [3]	Pattern counter, adaptive ramp generator, comparator and so on	$2^N T_{clk}$	0.18-μm, 2.5 V \$\star$\ 96.73%: catastrophic faults
The BIST in this work	Shown in Fig. 3	$(4N+2)T_{clk}$	Rohm 0.18-μm \ 6%\ 96%: R-2R network, 82.6%: OpAmp, and R variation $\geq$2 KΩ

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creases exponentially according to the resolution increase of the DUT. However, the proposed BIST technique in this work needs only $(4N+2)T_{clk}$ for an N-bit R-2R DAC. In addition to catastrophic faults, the parametric faults of resistance variation were also considered. Total 92.8% catastrophic faults and more than 2 kΩ resistance variation of each resistor in the R-2R network were detected. Additionally, the parallel design of the mentioned in Sect. 3.1 improved the resistance matching of the resistance-matching branches. In summary, the proposed BIST technique presents a good compromise between test time, area overhead and fault coverage.

5 Conclusions

The resistance matching based BIST technique for the current-mode R-2R DAC has been presented. With the fault sensitization strategies of dividing the network and feeding the complementary test currents, the proposed technique has offered high fault coverage of 96% for the R-2R network and 82.6% for the OpAmp. Also, the parametric faults of more than 2 kΩ resistance variation in each resistor of the R-2R network were detected. Therefore, the proposed testable R-2R DAC cab be an alterative analog stimulus generator for analog and mixed-signal BIST application.

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