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Low power logic BIST with high test effectiveness

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Abstract: Excessive test power has been a serious concern in BIST techniques. Shift power consumption can be significantly reduced by increasing the correlation among adjacent test data bits. However, this method may cause fault coverage loss. This paper presents a novel low power BIST scheme that reduces toggle probability of the scan input data while only shifting out part of capture responses for fault analysis and using the rest of capture responses as new test data. Using part of capture responses as test data can improve uniform distribution of 1 s and 0 s in test stimulus bits and thus result in high test effectiveness. Experimental results on larger benchmark circuits of ISCSAS89 and ITC99 show that the proposed strategy can reduce significantly test power while suppressing test coverage loss.

Keywords: scan-based BIST, switching activity, low power, test response, fault coverage

Classification: Integrated circuits

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1 Introduction

Logic Build-In Self-Test (BIST) is vital for digital system debug or field test. The power in scan-based test is higher than that in circuits normal operation [1]. In scan-based BIST, the power problem seems worse because of its unmanageable randomness. Excessive peak power dissipation may cause supply voltage droops eventually resulting in undesired yield loss, and excessive average power dissipation may cause hot spots which could damage the circuits under test (CUTs) [2].

Many sophisticated low power methods have been proposed for logic BIST. The approach in [3] clusters the scan chains into several groups and reduces shift power by enabling ineffective ones with mask logics during scan shift. Technique presented in [4] reduces test power by inserting extra logic gates to freeze the outputs of the scan flip-flops during scan operation. These extra logics may increase path delay in CUT. The approaches proposed in [5, 6] insert control logics between scan chain inputs and random test pattern generator to reduce the toggle rate of test stimulus bits. M. Filipek et al. propose a method that delivers constant values into the specified proportion of scan-chains at a time [7]. However, these methods could decrease test coverage for a given test length. The approach in [9] reduces shift-power by eliminating the specified high-frequency parts of vectors and also reduces capture power by using the multi-cycle BIST scheme with partial observation. The paper [10] presents a low power PRTG (Pseudorandom Test Pattern Generator) with programmable features which can reduce switching activity in scan chains significantly while virtually preserving original test coverage. The authors in [11] describe a low power programmable generator capable of producing test patterns with desired toggling levels and enhanced fault coverage gradient. These technologies provide relatively high test coverage, but require complicated control logics. In [8], we proposed a BIST scheme that reduces test power by delivering the same value to the adjacent scan cell. To prevent the decrease of fault coverage, it implements weighted random pattern testing by loading several kinds of different scan input data into scan chains with precalculated probabilities. In this paper we propose a more powerful low power BIST scheme which applies low transition test data and meanwhile uses a small fraction of test responses as part of new test pattern. This scheme enhances test effectiveness more significantly by improving the uniformity of 0 s and 1 s distribution for a low transition test pattern.

2 The proposed test scheme

It is conceivable that, delivering the same value to the adjacent scan cells can reduce the number of transitions at scan inputs during scan shift, and

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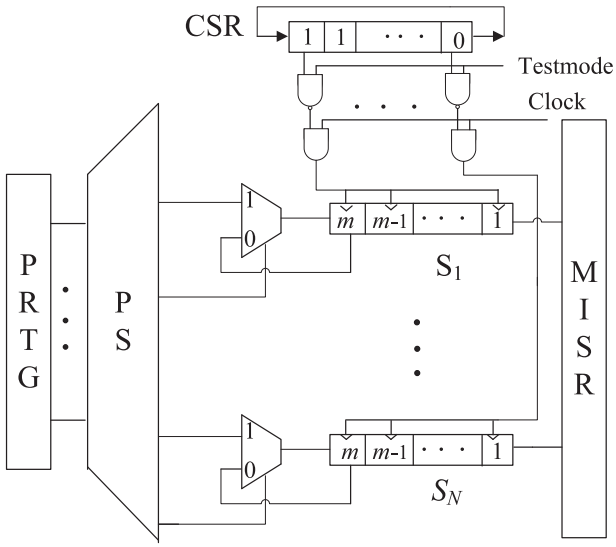

Fig. 1. The architecture of the proposed test scheme

thus reduce the power consumption in entire CUT. However, increasing the correlation among adjacent test stimulus bits degrades the uniformity of 0 s and 1 s distribution. That is to say, the consecutive 1 s or 0 s will appear often, and the state toggle (0→1 or 1→0) will become uncommon. As a result, some detectable faults cannot be detected by such test sequences and this may cause test coverage loss. For improving the uniformity of distribution in test stimulus while reducing switching activity significantly, we consider applying low transition test stimulus into scan inputs, and meanwhile utilizing a small fraction of test response as test data. This is because test responses usually have better uniformity of 0 s and 1 s distribution than low transition test stimulus. The test responses that are selected as a part of next test pattern will keep stationary (i.e, not shift out of scan chains during scan shift).

Based on this idea, we propose a novel BIST scheme depicted in Fig. 1. In this scheme, the scan cells are divided into N scan chains. The 2-input multiplexers are inserted between phase shifter (PS) outputs and scan chain inputs. These multiplexers select either pseudorandom test data directly from PRTG or previous scan value from the first scan cell of each scan chain. Each multiplexer has a 1-bit control signal which is also connected with PS output. When the control signal is 0, the previous scan value is selected and loaded into the scan chain input repetitively. Otherwise, pseudorandom data generated by PRTG is delivered into the scan chain. The output of each scan chain is connected with one bit of the multiple input signature register (MISR). Test responses compacted by MISR will be used for fault analysis. An N-bits cyclic shift register (CSR) is embedded in the CUT. Each bit of CSR controls the clocks of a scan chain via a NAND gate and an AND gate. We call the AND gate inserted between a clock line and the corresponding scan flip-flop clock input as clock gater. If set properly, they prevent clock pulses from reaching some scan chains and force them to hold their states during scan shift. In scan shift operation (testmode=1), if a bit in CSR is 1, the corresponding NAND output is 0 and the corresponding clock gater

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output is also set to 0. This means that the clock of corresponding scan chain is turned off and its state will hold during scan shift. In capture operation (testmode=0), both NAND output and clock gater output are set to 1. Thus, all scan chains can capture test responses regardless of the values in CSR.

If some scan chains hold their states for next test pattern after a capture cycle during scan shift (for conveniences sake, this kind of scan chains are referred to as non-shift scan chains hereinafter), it's predictable that test power in CUT can be reduced further. At the same time, test responses usually have better uniformity of 0 s and 1 s distribution than low transition test stimulus, so fault coverage loss caused by low transition test application can be offset in this sense. However, the test responses in non-shift scan chains won't be helpful to fault detection. In this sense, giving up to observe a fraction of scan chains may have bad impact on test coverage. The factual test coverage is determined by the two conflicting factors jointly. The positive impact on test coverage is predominant when the ratio of non-shift scan chains is small. The bad impact on test coverage may become predominant when the ratio of non-shift scan chains is very large. Therefore, the number of non-shift scan chains should not be large enough if the high test coverage requirement is top-priority.

The test procedure for the scheme is described briefly as follows. At the beginning of test, we initialize the CSR so that only a fraction of bits are 1 s and the other bits are 0 s. For the sake of presentation, let us suppose that two scan chains are selected as non-shifting scan chains in the scheme. For example, if the values in the CSR are 110000...00 at a test cycle, then only the clocks of scan chain S_1 and S_2 are gated during scan shift (testmode=1). The test responses in S_1 and S_2 constitute part of next test pattern. At the moment, test stimulus are shifted in scan chains except for S_1 and S_2 from scan inputs (multiplexer outputs) while shifting out the test responses captured in these scan chains. If the control signal of a multiplexer is 1 at a clock cycle, pseudorandom test data generated by PRTG is shifted in corresponding scan input; otherwise, test data are delivered repetitively. After shifting in a test pattern, CUT goes into normal mode (testmode=0). At this time, all scan chains capture test responses. The CSR is shifted one bit cyclically to the right just before scanning into a new test pattern (thus non-shift scan chains change cyclically). Then, CUT goes into test mode again and a new test pattern is shifted into scan chains (testmode=1). This test procedure is repeated until test terminates.

3 Toggle probability analysis at scan inputs of shifting scan chains

In the section, we analyze certain properties of test patterns generated by the proposed scheme. We define the toggle probability of a scan input s_i as the probability that s_i is assigned value v ($v \in \{0,1\}$) at a clock cycle and the opposite value $\overline{v}$ at next clock cycle. In order to make every possible test pattern appear, the toggle probability of any scan input should be 0.5.

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When a scan chain is driven by a traditional Linear Feedback Shift Register (LFSR), the toggle probability of its input is nearly 0.5. In contrast, applying low transition test stimulus decreases toggle probability of scan inputs.

The probability of a PS output being value 0(or 1) at a clock cycle is 0.5. Hence, the probability of the multiplexer control signal being vaule 0(or 1) is 0.5, written as $P_{con}(0) = P_{con}(1) = 0.5$. The probability of the multiplexer 1-input being value 0(or 1) is also 0.5. Since the input of a scan chain toggles only when control signal of the multiplexer is assigned a 1 and the previous assigned value in 1-input of the multiplexer is assigned a 0(or 1) and the current one is assigned a 1(or 0). The toggle probability of a scan chain input written as $P(toggle)$ can be calculated as follows:

$$\begin{aligned} P(toggle) &= P_{con}(1) \times [P_{pre}(1) \times P_{cur}(0) + P_{pre}(0) \times P_{cur}(1)] \\ &= 0.5 \times (0.5 \times 0.5 + 0.5 \times 0.5) = 0.25, \end{aligned} \tag{1}$$

where $P_{pre}(0/1)$ and $P_{cur}(0/1)$ is the probability that the previous and current values of the multiplexer 1-input are assigned as 0/1 respectively. If we insert a multiple-input AND gate between the control input of multiplexer and PS output, toggle probability will get smaller resulting in more significant test power reduction. To avoid significant fault coverage loss due to applying extremely low toggling patterns, this method isn't recommended.

4 Experimental results

Experiments are performed on several larger ISCAS89 and ITC99 benchmark circuits. The average and peak weighted switching activity (WSA) at a clock cycle in the whole CUT are used to evaluate average and peak shift test power. Stuck-at fault model is targeted.

Table I shows the results for the proposed scheme. Our scheme uses LFSR as PRTG whose size is set as 40 or 50. Columns 2-4 designate the number of scan chains, the number of applied test patterns and the fault coverage obtained by traditional LFSR-based scheme. The columns under the heading *non-shift: 10% (20%, 30%, 40%)* show simulation results obtained by the proposed scheme that with the percentage of non-shift scan chains equal to 10% (20%, 30%, 40%). The subcolumns labeled *FC* show the fault coverage for the given test length. The subcolumns labeled *ave. red* and *peak red* show the savings in average WSA and peak WSA by using the proposed scheme compared with traditional LFSR, respectively. The percentage of area overhead is presented in the last column. Area overhead is estimated based on the cell library class.lib of the Synopsys system [12]. As shown in the table, the amount of WSA reduction increases as the percentage of non-shift scan chains increases. Meanwhile, the proposed scheme suppresses the fault coverage loss effectively. The additional logics are very trivial in relation to the circuit size.

Table II presents comparison of average WSA and test coverage between the proposed scheme and two other effective low power schemes [5, 8] for the cases with most efficient power reduction. (Peak WSA is not presented in [5]

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Table I. Experimental results for the proposed scheme

Circuit	# sc	length	Lfsr	non-shift: 10%			non-shift: 20%			non-shift: 30%			non-shift: 40%			ao %
			FC	FC	ave. red	peak red	FC	ave. red	peak red	FC	ave. red	peak red	FC	ave. red	peak red	
S5378	10	65536	98.64	98.72	33.8	24.3	98.61	41.8	34.5	98.24	46.3	41.2	97.52	52.1	44.9	4.2
S9234	10	524288	89.46	93.13	38.1	28.4	92.96	44.2	32.7	92.57	52.6	39.7	92.51	59.7	41.8	2.4
S13207	20	132072	98.02	97.57	41.3	31.5	97.19	47.6	39.8	96.06	54.1	43.6	96.57	62.2	48.9	2.6
S15850	20	132072	92.02	96.24	39.3	23.4	96.23	47.7	32.4	96.19	53.7	36.0	96.14	62.3	40.9	2.4
S35932	20	128	87.80	89.44	38.0	21.2	89.51	45.1	25.7	89.34	54.4	30.5	89.05	59.8	38.8	1.0
S38417	20	132072	96.61	95.73	40.6	29.1	96.00	47.9	34.9	95.68	54.1	41.6	95.63	60.0	50.2	1.0
S38584	20	132072	94.40	95.58	42.3	20.3	95.44	49.7	26.9	95.40	57.8	31.2	95.41	64.8	37.5	0.9
B20	10	132072	91.57	93.88	35.8	19.6	93.76	40.9	23.3	93.65	47.1	28.7	93.44	53.9	34.1	0.6
B21	10	132072	90.55	93.23	35.6	17.4	93.09	40.5	22.8	93.00	48.5	25.4	92.55	54.4	29.3	0.6
B22	10	132072	92.86	94.97	37.3	20.7	94.96	43.0	25.6	94.66	49.1	29.1	94.67	56.3	36.5	0.4
AVG	-	-	93.19	94.85	38.2	23.6	94.78	44.8	29.8	94.48	51.8	34.7	94.35	58.6	40.3	1.6

Table II. Experimental result comparison with low power schemes in [5, 8]

Circuit	LT-RTPG [5]		Low power [8]		Proposed scheme	
	FC	ave. red	FC	ave. red	FC	ave. red
S5378	96.54	43	96.68	45	97.52	52.1
S9234	90.89	62	92.34	63	92.51	59.7
S13207	93.66	45	94.98	53	96.57	62.2
S15850	94.40	58	95.91	57	96.14	62.3
S35932	87.84	56	88.47	56	89.05	59.8
S38417	94.99	56	95.46	58	95.63	60.0
S38584	93.35	59	94.78	59	95.41	64.8
Ave.	93.10	54.1	94.09	55.8	94.69	60.1

and [8].) All the three schemes apply the same number of test patterns for every benchmark circuit as shown in Table I. In the table, all of the power reduction percentages are calculated by taking the power results of traditional BIST scheme as a comparison baseline. It is clear that, the proposed technique can attain higher fault coverage while achieving more significant test power reduction than the methods in [5] and [8] for all benchmark circuits except for S9234.

5 Conclusion

In order to improve the tradeoff between test power reduction and test coverage loss, this paper provides a powerful BIST scheme. The proposed technique applies low transition test stimulus into scan inputs for shift power reduction. On the other hand, it selects a small fraction of scan chain as non-shift ones and uses the test response in them as a part of next test pattern. In this way, the proposed technique reduces the switching activity further and suppresses test coverage loss efficiently. Experiment results show that proposed scheme can achieve good results with little area overhead.

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