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Design of a digital controller for an LED driver with a digital dimming

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Abstract: This letter presents a new digital controller (DCL) with a new dimming method for high power-factor LED driver circuits. The core of proposed digital controller is based on a zero-voltage (ZVD) detection and a digital sine generator (DSG). By using the DSG, an effective dimming can be carried out easily. The proposed DCL was simulated and fabricated using the 1 μm-650 V DMOS process. The results obtained indicate that the inductor current waveform is in phase with the input voltage to gain a high power factor, because the inductor current is synchronized to the zero voltage signal from ZVD as expected. Also, the LED current changes according to the reference voltage, which is controlled by an external switch that adjusts the brightness of the LED.

Keywords: LED driver, digital sine-signal, zero voltage detection, dimming, soft-starter

Classification: Integrated circuits

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1 Introduction

Nowadays, LED lighting is more and more often accepted as a light source in many applications due to the fact that LED lights have high light

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efficiencies, long operating lifetimes, small size, and are environmentally friendly [1, 2]. Technological advancement in recent years enables a high-brightness LED to be used as a best choice. However, LEDs require driver circuits with a considerable complexity when directly driven by commercial AC supplies. The asymmetric I-V characteristic of LED devices as diodes makes the load current profile considerably different from that of the AC offline voltage, which results in significant degradation in the power factor. In order to comply with standards such as IEC61000-3-2 Class C [3] that mandate higher than 85% power factors, most existing LED modules employ power-factor correction (PFC) circuits that function in the continuous-conduction mode (CCM) [5, 6]. These CCM converters usually consist of many external devices that cause degradation of LED modules and the increase in cost; such as bulky electrolytic capacitors (results in a reduction in the LED module's lifetime), voltage dividing resistors (to extract the sine-wave phase reference from the AC line which causes an increase power consumption), and power MOSFETs [4]; also, it is hard to integrate these resistors on an IC.

A dimming system is beneficial for all lighting systems, not only for energy saving purposes but also for electricity demand reduction, visual comfort for the room occupants, and better productivity at the work place. In current CCM LED drivers, the dimming control is quite complicated. Most of them use TRIAC dimming [6], which leads to the complexity in circuit design. In other hand, for general lighting applications, discrete-dimming levels are used instead of the continuous dimming for the simplicity. So that LED drivers that can be implemented totally in integrated circuit with high efficiency are still required.

In this study, we have developed a simple DCL that operates in the discontinuous-conduction mode (DCM) for high PF LED drivers. This DCL owns a simple and effective digital dimming for general LED lighting applications. The DCL can be easily implemented in a single chip without external components and eliminates the shortcomings of conventional converters as mentioned before.

2 Proposed digital controller for LED driver

In a conventional buck-type LED controller, the current from the switching MOSFET is compared with the DC level of the reference signal, and outputs a constant duty cycle. However, the proposed controller uses a sine-wave reference signal, which is in phase with the AC line voltage causing the LED current to also be in phase with the AC line voltage. As a result, the PF becomes very close to unity and the LED current shows a low THD, as outlined in [3].

Fig. 1 shows the proposed, simplified block diagram of the DCL used for LED drivers. Fig. 2 shows the specific block diagram of the proposed DCL. The proposed DCL is composed of three main sub-blocks: a zero voltage detector (ZVD), a digital sine-signal generator (DSG), and a digital dimming control. The operation of the DCL is described as follows. The ZVD circuit generates the ZVD signal, using the transmission gate synchronized with the clock that is used in the inductor current signal generator, comparator, and reference voltage for the ZVD. The ZVD signal is generated by comparing the V_{drain} (the voltage at the drain of the power

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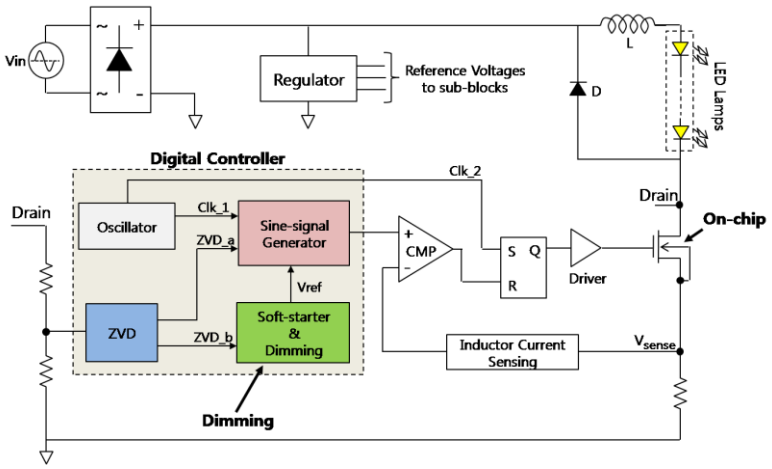

Fig. 1. Block diagram of an LED driver using proposed DCL.

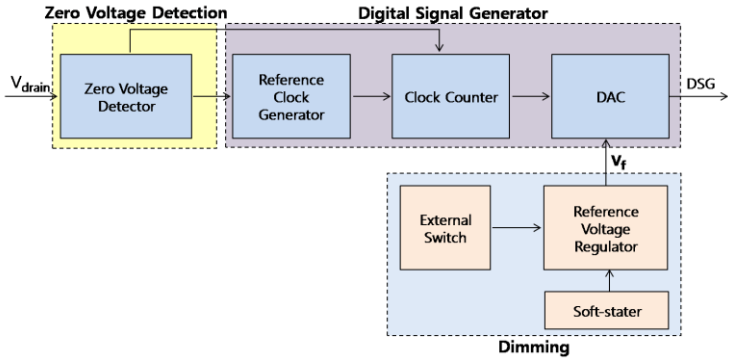

Fig. 2. Block diagram of the proposed DCL for LED driver.

MOSFET) generated by the inductor current with a reference voltage for the ZVD. The ZVD detects when the V_{drain} is close to 0, and it generates a signal synchronized with the input voltage. By determining the start and end of the DSG signal relative to the ZVD signal, it is possible to create a waveform similar to the input voltage. By this way, the DSG design eliminates bulky capacitors or voltage dividing resistors as used in conventional CCM LED drivers.

Adjustment of the brightness is realized via regulating the LED current. The LED current depends on the duty ratio of PWM pulse fed to gate of power MOS. As shown in Fig. 1, the duty ratio which is determined by comparing V_{sense} and the DSG signal. Basing on DSG, an effective dimming can be carried out easily. Fig. 3 shows the proposed digital dimming circuit. The soft-start function is added to the dimming circuit to prevent the inrush current from damaging the power MOSFET and LED string when the external supply is turned on. The soft-starter is composed of D flip-flops that are clocked by the ZVD_b signal comes from ZVD. The main idea of this method is to generate a reference voltage. This reference voltage is used for determining the magnitude of the DSG signal, as used in the brightness adjustment. This reference voltage is generated and divided into 2 phases.

Phase 1 (Soft-start): The a, b, and c outputs become high in turn as the clock advances turning on M6, M7 and M8 in sequence. Therefore, the reference voltage increases gradually. The biggest reference voltage in this

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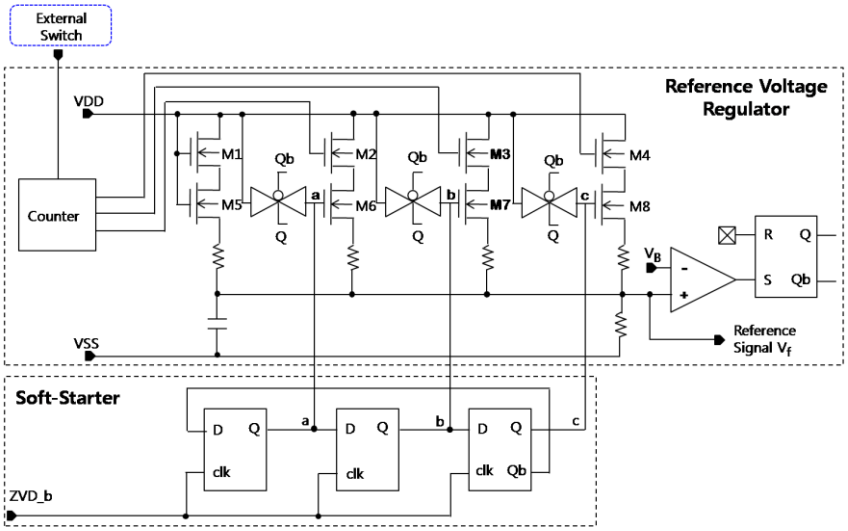

Fig. 3. The proposed digital dimming circuit.

phase is set to be higher than the V_B to ensure that the FFs of the soft-starter will not work anymore in the RS-FF mode. This make the soft-start ends properly and give the control of dimming to external switch in phase 2.

Phase 2 (Dimming from external switch): By using an external switch, an adjustment request signal will be generated and applied to counter. The counter works in the following sequence: 111,011,001,000,100,110,111. This results in turning on/off in the order M2 – M3- M4 then causes the changes the reference signal. Note that it is possible to expand the number of dimming levels if required by using a counter with a higher resolution.

3 Simulation and measurement results

To evaluate the characteristics of the proposed circuit prior to IC fabrication, the circuit was simulated. Fig. 4 shows the simulation results of LED driver using the proposed DCL. A high PFC can be verified on the basis of the relationship between the input voltage and the inductor current. The circuit was simulated and fabricated using the 1 μm-650 V DMOS process that provides double-diffused MOS transistors with a breakdown voltage of 600 V and a diode. This reduces the component count and cost of the circuit as compared with that of a conventional PFC. Fig. 5 shows an image of the photomicrograph of the fabricated chip that occupies an area of $1.11 \times 1.78\,\text{mm}^2$.

As shown in Fig. 4 (a), the ZVD signal is created by detecting when the input voltage is low. The ZVD signal determines the start and end of the DSG causing the DSG signal to be synchronized to the input voltage that makes the LED current waveform is close to a sinusoid synchronized with the input AC voltage as expected as shown in Fig. 4 (b). This indicates that the input impedance is nearly constant and independent as seen from the input voltage. As a result, the PF becomes very close to unity. When the external switch operates, it changes the output states of the counter to change the reference signal amplitude as shown in Fig. 4 (a). Next, it has been found that the magnitude of the inductor current according to the reference voltages changes as shown in Fig. 4 (b). These results confirmed

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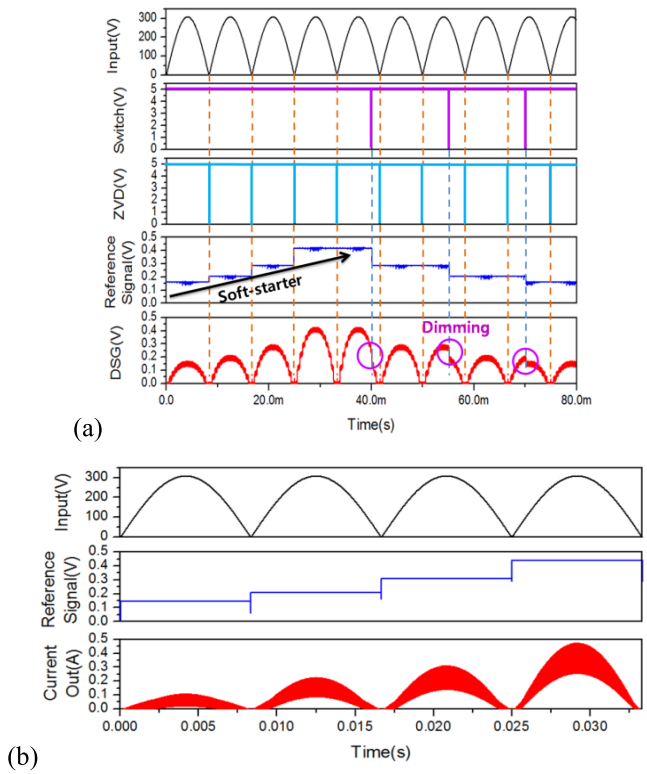

Fig. 4. Simulated results of LED driver using the proposed DCL.

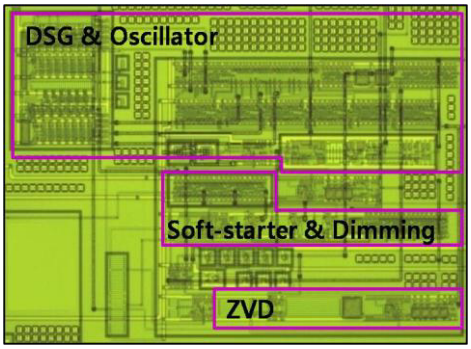

Fig. 5. Microphotograph of the proposed DCL.

the function of the proposed dimming method as expected. Also, the reference signal changes according to the soft-starter's function to prevent damage to the power MOSFET and LED string when the LED driver is turned on.

Fig. 6 shows the measured waveforms of the fabricated chip. As shown in Fig. 6 (a), the oscillator generates a frequency of 120 kHz; Fig. 6 (b) shows the generated ZVD signal, which is synchronized and matched with the input voltage. Figs. 6 (c)–(d) show the DSG according to the reference signal, which can be changed by an external switch for dimming purpose. These results confirm the design functions and the high PF that proposed DCL can be gained. Table I summarizes the measured data of the proposed DCL from the fabricated chip.

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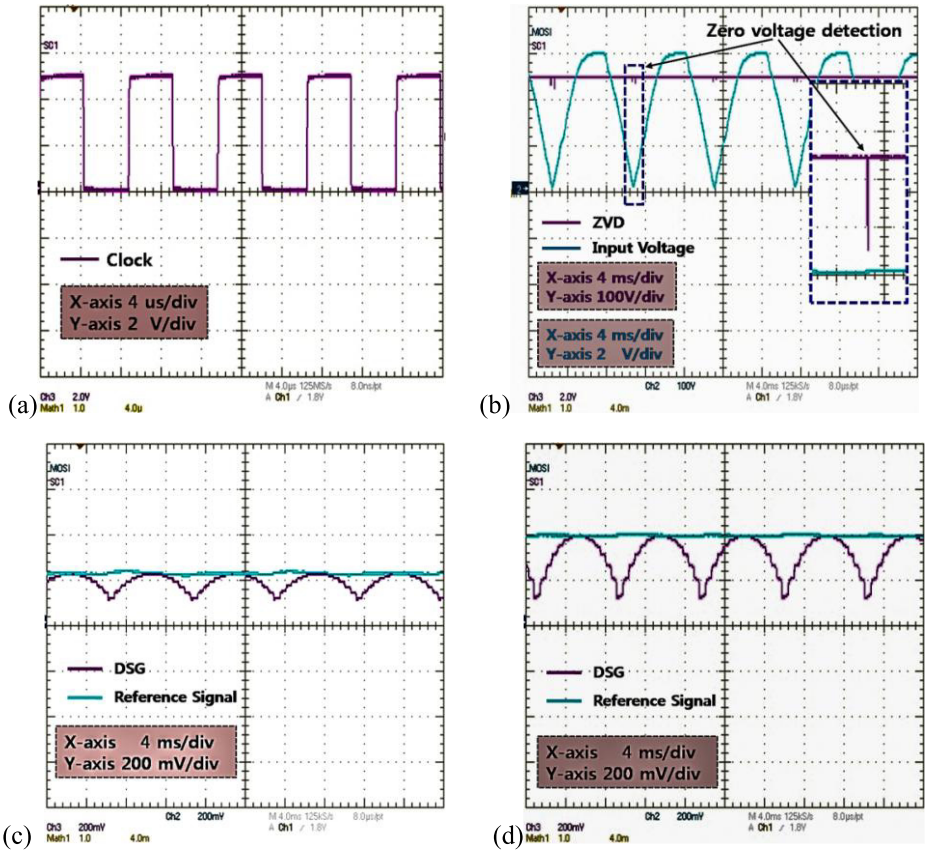

Fig. 6. Measured waveforms of the fabricated chip. (a) Clock signal. (b) ZVD signal. (c)–(d) Reference and DSG signal.

Table I. Summary of the measured data.

Subject		Value	Unit
IC Process		1 μm-650V DMOS process	-
Input Voltage		220 Vrms @ 60 Hz	-
Frequency of Oscillator		120	kHz
Number of Bits of DSG		6	Bit
Number of Bits of Soft-starter		4	Bit
Magnitude of DSG	Max.	440	mV
	Min.	160	mV
Number of brightness steps		4	Step

4 Conclusion

In this letter, we proposed a new digital controller that exhibits a high PF and involves the use of a new dimming method for an LED driver. The proposed controller was simulated and fabricated using the 1-μm-650 V DMOS process. Simulation and experimental results are included to verify the proposed method. The proposed circuit is suitable for a low-cost IC implementation that can mitigate the high costs of the currently solutions.

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