LETTER

IEICE Electronics Express, Vol.11, No.4, 1–6

An SET hardened dual-modular majority voter circuit for TMR system

Xiaopeng Liu, Yan Han[a)], and Bin Zhang

Institute of Microelectronics & Photoelectronics,

Zhejiang University, Hangzhou, China

a) *hany@zju.edu.cn*

Abstract: A Triple-modular redundancy (TMR) system will have a failure if Single Event Transient (SET) faults affect the voter. In this paper, we propose a full SET-tolerance dual-modular majority voter (DMV) circuit for all internal nodes. The DMV consisting of two simplex-modular voters, two inverters, a C-element inverter and a weak keeper is implemented in CMOS 40 nm technology. A novel XOR gate and a multiplexer based voter is also presented and used as a simplex-modular voter so that the whole DMV can be implemented by 40 CMOS transistors. A novel C-element weak keeper is also proposed to reduce power consumption. Monte-Carlo simulation results show that power consumption of DMV only increases by 11.09% compared to that of a single traditional voter.

Keywords: dual-modular majority voter (DMV), SET, triple-modular redundancy (TMR), radiation hardening

Classification: Electron devices, circuits, and systems

References

[1] R. V. Kshirsagar and R. M. Patrikar: Microelectronics Reliability **49** [12] (2009) 1573.

[2] J. Chen, S. Chen, B. Liang, B. Liu and F. Liu: Microelectronics Reliability. **52** [6] (2012) 1227.

[3] J. R. Qin, S. M. Chen and B. W. Liu: SCIENCE CHINA Information Sciences **55** [6] (2012) 1461.

[4] R. Rajaei, M. Tabandeh and M. Fazeli: Microelectronics Reliability **53** [6] (2013) 912.

[5] M. Stanisavljevic, A. Schmid and Y. Leblebici: IEEE Trans. Nanotechnol. **8** [3] (2009) 379.

[6] K. Nikolic, A. Sadek and M. Forshaw: Nanotechnology **13** [3] (2002) 357.

[7] M. Favalli and C. Metra: IEEE Trans. Reliab. **53** [3] (2004) 342.

[8] D. E. Muller and W. S. Bartky: Int. Symp. on Theory of Switching (1959) 204.

[9] F. L. Yang and R. A. Saleh: IEEE J. Solid-State Circuits **27** [3] (1992) 258.

[10] T. Dysart and P. Kogge: IEEE Trans. Nanotechnol. **10** [5] (2011) 1015.

[11] M. D. Krstic, M. K. Stojcev, G. Lj. Djordjevic and I. D. Andrejic: Microelectronics Reliability **45** [3-4] (2005) 733.

DOI: 10.1587/elex.11.20131029
Received December 26, 2013
Accepted January 23, 2014
Publicized January 31, 2014
Copyedited February 25, 2014

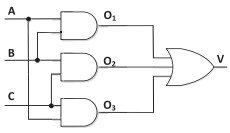
IEICE Electronics Express, Vol.11, No.4, 1–6

1 Introduction

With the rapid technology scaling down, the probability of SET fault in digital integrated circuit (IC) becomes higher and higher [1]. SET has already become one important concern for the radiation effect researchers [2], because SET in combinational logic circuit causes the system soft errors [3, 4]. Nowadays, reliability is emerging as an important parameter in deep submicron electronic technologies. As a consequence, different fault-tolerance techniques [9] also called hardening techniques used to guarantee correct operation even in the presence of faults have been studied over the past years [5]. In system level, we can utilize redundant unreliable components and majority voters [11] to construct a relatively reliable system. TMR [6] and NMR (N-tuple modular redundancy) [10] are known as the benchmark techniques in high reliability applications. TMR system consists of three replicated modules statically connected to a majority voter. It's obvious that a TMR system will have a failure if faults are affecting the voter [7].

There are very few reports on hardened voters used in TMR system in recent years. R. V. Kshirsagar et al. proposed a novel fault-tolerant voter which can be implemented by 22 transistors [1], however, the voter in [1] is not a fault-tolerant voter any more, when the three inputs (A, B, C shown in Fig. 1) of the voter are not "000" or "111".

In this paper, we propose a high reliability DMV which is a full fault-tolerance voter for all internal nodes thanks to the using of C-element inverter [8]. Monte-Carlo simulation results are provided to evaluate and compare the proposed voter and previous voters.



Truth table

C	B	A	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Fig. 1. The traditional voter and its truth table.

2 The traditional voter

As we know, TMR is widely used for SET mitigation [5]. The voter is an essential part in a TMR system. The traditional majority voter and its schematic and truth table are shown in Fig. 1. If input is one of "011", "101", "110" and "111", the voting result is "1", otherwise, the output of voter is "0". We can use a piecewise linear current source (IPWL) as SET model [9] in Cadence Spectre to evaluate the SET-tolerance ability of traditional voter which has been simulated in a SMIC 40 nm CMOS technology. As the Q_{crit} is only about 1.5 fc in 40 nm technology, to get a 0-to-1 SET on the output, the SET injection node is connected to a current source which is turned on just for 0.1 ns and offers a negative current spike whose amplitude is only 30 uA. The output voltage which is 0 V will be pulled up to VDD (1.1 V) due to the instantaneous current provided by the current source. After the current source is turned off, the output will recover to its previous state. To

DOI: 10.1587/elex.11.20131029
Received December 26, 2013
Accepted January 23, 2014
Publicized January 31, 2014
Copyedited February 25, 2014

IEICE Electronics Express, Vol.11, No.4, 1–6

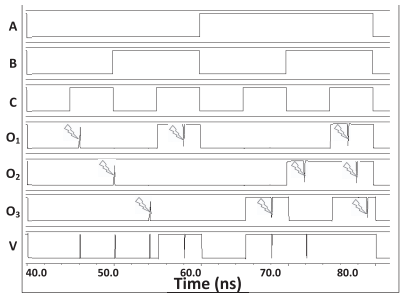


Fig. 2. Waveforms of the traditional voter with SET injections.

get a 1-to-0 SET, the node is connected to a current source which is turned on just for 0.1 ns and offers a positive current spike whose amplitude is also 30 uA. Similarly, three IPWLs are used to inject SETs at O_1, O_2 and O_3 of the traditional voter.

As simulation waveforms shown in Fig. 2, all the SETs at internal nodes O_1, O_2 and O_3 with different inputs (except for "111" input) are propagated to the output. So the traditional voter almost has none ability of SET tolerance. If the voter is used in a high speed TMR system and the propagated SET is sampled by the next module, such as a flip-flop, the whole TMR system will fail.

In case of digital integrated circuit implementation, if the circuit size of voter is similar as that of other module, the reliability of voter is the same as that of other module. TMR system will fail if the voter fails regardless of whether or not other modules fail [1]. R. V. Kshirsagar et al. proposed a fault-tolerant voter which could be implemented by 22 transistors, however, the voter in [1] only prevent partial internal nodes from the influence of SET with three inputs are same ("000" or "111"). When the three inputs are different, the voter is not a SET-tolerant voter any more.

3 The proposed DMV

Therefore, we propose a full SET-tolerance voter for all internal nodes with different inputs in this paper. As shown in Fig. 3, the presented DMV consists of two simplex-modular voters, two inverters, a C-element inverter and a weak keeper. The C-element inverter and its truth table are illustrated in Fig. 4. The output of a two-input C-element inverter will be the inverted value of the inputs after both inputs have reached the same value; otherwise the output remains unchanged if the frequency of input is high (about MHz). Due to

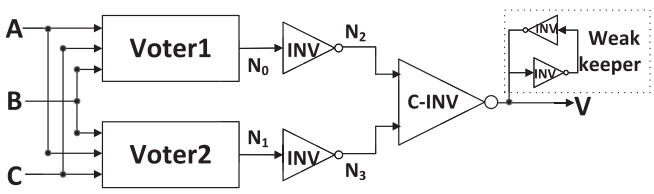
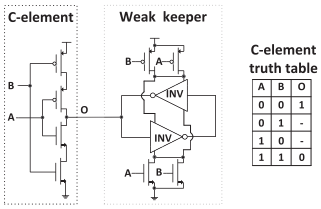


Fig. 3. Block schematic of the proposed DMV.

DOI: 10.1587/elex.11.20131029
Received December 26, 2013
Accepted January 23, 2014
Publicized January 31, 2014
Copyedited February 25, 2014

IEICE Electronics Express, Vol.11, No.4, 1–6



A	B	O
0	0	1
0	1	-
1	0	-
1	1	0

Fig. 4. The C-element inverter and its weak keeper.

the using of a C-element inverter, the proposed DMV can mask any single internal SET fault and get correct output.

Only when single internal SET fault happens, the two states of A and B become different which make the output to be a floating state. So a weak keeper is needed at the output node of C-element. However, the state of A is the same as that of B at most time, if we use the weak keeper shown in Fig. 3, the weak keeper works at all the time. In order to reduce power consumption, we design a novel C-element weak keeper shown in Fig. 4 which only works when the state of A is different from that of B.

3.1 The XOR and multiplexer based voter

The traditional voter needs 26 transistors according to its schematic shown in Fig. 1 directly. In order to reduce the power consumption and have a fair comparison, the traditional voter implemented by NAND gates requires 18 transistors. We analyze the equation of majority voter and find out the equation can be:

$$\begin{aligned} V &= \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC \\ &= (\overline{A}B + A\overline{B})C + AB(\overline{C} + C) = (A \oplus B)C + AB \\ &= (A \oplus B)C + \overline{(A \oplus B)}A \quad or \quad (A \oplus B)C + \overline{(A \oplus B)}B \end{aligned} \tag{1}$$

where, V is the voting result, and A, B, C are three inputs of a majority voter. Consequently, the majority voter can be implemented by an XOR gate and a 2-to-1 multiplexer according to Eq. (1). The output of the XOR gate connects with the selection port of the multiplexer. The number of transistors used in the novel majority voter is only 12. As illustrated in Fig. 5, an XOR gate requires 6 transistors and a 2-to-1 multiplexer requires 6 transistors, so that the whole DMV based on the novel voter only requires 40 transistors and consumes lower power. The inputs of XOR can be any two of the three inputs.

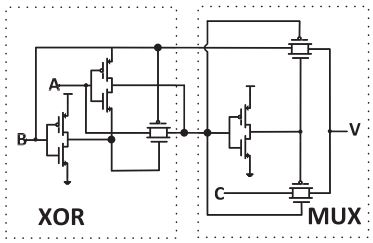


Fig. 5. The schematic of XOR and MUX based voter.

DOI: 10.1587/elex.11.20131029
Received December 26, 2013
Accepted January 23, 2014
Publicized January 31, 2014
Copyedited February 25, 2014

IEICE Electronics Express, Vol.11, No.4, 1–6

4 Simulation and comparison results

4.1 Function simulation of the XOR and multiplexer based voter

The XOR and multiplexer based voter has been implemented in a SMIC 40 nm CMOS technology. The aspect ratio W/L of all NMOS is 120 nm/40 nm and aspect ratio W/L of all PMOS is 240 nm/40 nm. Fig. 6 depicts Spectre simulation waveforms and shows that the XOR and multiplexer based voter has correct voting results and can be used in TMR systems.

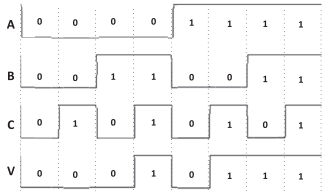


Fig. 6. Waveforms of the XOR and MUX based voter.

4.2 SET injections to the DMV

As mentioned above, the XOR and multiplexer based voter are used as a simplex-modular voter in the DMV to reduce the total power consumption. Similarly, SETs are injected to internal nodes N_0, N_1, N_2 and N_3 using IPWLs in Spectre. In Fig. 7, SETs at N_0 and N_1 are inverted by two inverters, so there were extra glitches at N_2 and N_3. All the single SET at internal nodes N_0, N_1, N_2 and N_3 with different inputs could be masked because the output of a C-element only changes with the same two inputs. Although, there is a internal single SET, the final output of the DMV is correct. As we can see, the proposed DMV is a full SET-tolerance voter which can mask all internal single SET with all 8 kinds of input group.

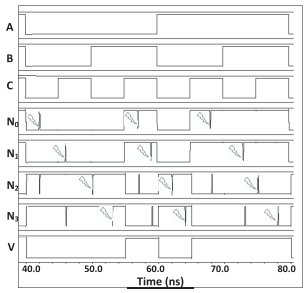


Fig. 7. SET injections to the nodes N_0, N_1, N_2 and N_3.

4.3 Comparison

In order to have a fair comparison, the traditional voter and the voter in [1] are also simulated in a SMIC 40 nm CMOS technology with same aspect ratio W/L as that of the DMV. We run Monte-Carlo simulation with 5000 samples at 1.1 V voltage supply at room temperature. The frequency of A is 250 MHz, the frequency of B is 500 MHz and that of C is 1 GHz. Although the number

DOI: 10.1587/elex.11.20131029
Received December 26, 2013
Accepted January 23, 2014
Publicized January 31, 2014
Copyedited February 25, 2014

IEICE Electronics Express, Vol.11, No.4, 1–6

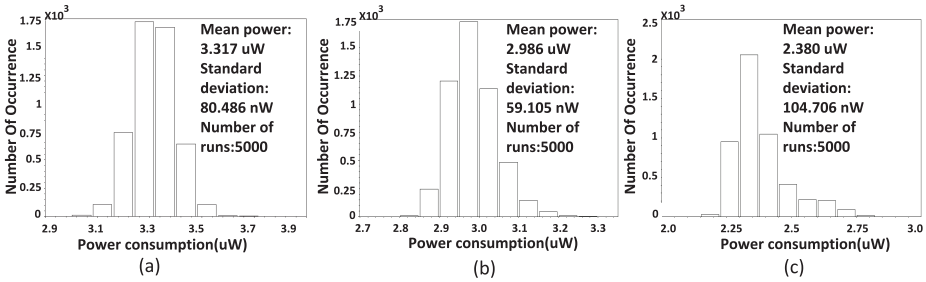


Fig. 8. Monte-Carlo simulation results of power consumption of the three kinds of voters : (a) The proposed DMV (b) The traditional vote (c) The voter in [1].

of transistor of the DMV is more than twice that of the traditional voter (18 transistors), the power consumption of the DMV only increases by 11.09% compared to that of a single traditional voter as shown in Fig. 8. That is because the proposed XOR and multiplexer based voter is transmission gate logic and the proposed C-element keeper is turned off at most time. Although the voter in [1] consumes least power, it is not a full SET-tolerance voter. Monte-Carlo simulation results show that the delay of DMV is 91.09 ps (the delay of traditional voter is 57.47 ps), so the DMV can be applied in the ultra-high speed TMR systems.

5 Conclusion

The proposed DMV which can be implemented by 40 transistors is a full SET-tolerance voter for all internal nodes. Meanwhile, Monte Carlo simulation results are also given to confirm that the power consumption of the proposed DMV doesn't increase sharply. The DMV can also be applied in the ultra high speed TMR systems.

DOI: 10.1587/elex.11.20131029
Received December 26, 2013
Accepted January 23, 2014
Publicized January 31, 2014
Copyedited February 25, 2014