

Settling time optimization technique for binary-weighted digital-to-analog converter

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Abstract: Settling behavior of the binary-weighted switched-capacitor digital-to-analog converter output is analyzed and a design method for fast settling is presented. A calibration circuit that effectively reduces settling time beyond the process limit is also proposed and verified with various simulations.

Keywords: digital to analog converter, analog to digital converter, switched-capacitor circuit, settling time, successive approximation

Classification: Integrated circuits

References

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1 Introduction

Binary-weighted switched-capacitor (SC) digital-to-analog converters (DAC) [1] are widely used in wideband applications. It is also a key building block of the successive approximation register (SAR) analog-to-digital converter (ADC) [2, 3, 4], which has recently gained popularity in high-speed applications. In those applications, settling time of the SCDAC often limits the operation speed or signal bandwidth. It is well known that SCDAC settling is determined by the RC time constant (τ) associated with switch on-resistance (R_{ON}) and capacitance, thus it can be minimized by either reducing R_{ON} , or capacitance. However, capacitor size is mainly determined by either matching requirements or thermal noise. Therefore, increasing the transistor size to reduce R_{ON} has been considered the only option for fast settling. How-

ever, as the transistor size increases, parasitic capacitance of the transistor also gets bigger and increases the total capacitance and τ . Thus, the minimum τ for a given process is almost fixed and there seems to be no other options to further reduce settling time. In this letter, settling behavior of a binary-weighted SCDAC is carefully analyzed and a calibration circuit that can reduce settling time beyond the process limit is proposed and verified with simulations.

2 Analysis and optimization of binary-weighted SCDAC

Fig. 1 (a) shows the simplified schematic of a binary-weighted SCDAC. DAC capacitors are switched to one of the reference voltages (V_{REF} and GND) based on the digital input. For simplicity, the single-ended version is analyzed here, but the analysis can be applied to the fully-differential case. The equivalent circuit when the most significant bit (MSB) capacitor switches from GND to V_{REF} is shown in Fig. 1 (b). C_{MSB} and R_{MSB} are the MSB capacitance and R_{ON} of the MSB switch, respectively. The rest of the capacitors and switches from the second MSB to the least significant bit (LSB) are merged into C_{EQ} and R_{EQ} . C_{EQ} is the total capacitance, which equals C_{MSB} , and R_{EQ} is the parallel combination of R_{ON} from the second MSB to LSB switches. The settling behavior of the MSB capacitor during switching is analyzed here because the MSB largely determines the DAC operation speed. However, LSB switching can also be modeled and analyzed similarly. It is assumed that DAC capacitors have been fully discharged and connected to GND , since initial charge of DAC capacitors won't affect settling behavior. At time $t=0$, the MSB capacitor is switched to V_{REF} and the s-domain equivalent circuit can be drawn as Fig. 1 (b). Current flowing through the capacitor and the output of DAC, V_{DAC} , can be easily found as follows

$$\begin{aligned} I &= \frac{V_{REF}/s}{R_{MSB} + R_{EQ} + 2/sC}, \quad V_{DAC}(s) = \left(\frac{1}{sC} + R_{EQ} \right) \cdot I \\ &= \frac{V_{REF}/2}{s} + \left(\frac{R_{EQ}}{R_{MSB} + R_{EQ}} - \frac{1}{2} \right) \cdot \left(\frac{V_{REF}}{s + 2/((R_{MSB} + R_{EQ}) \cdot C)} \right) \quad (1) \end{aligned}$$

By taking inverse Laplace transform, the time-domain DAC output, $V_{DAC}(t)$ becomes

$$V_{DAC}(t) = \left(V_{REF}/2 + \left(\frac{R_{EQ}}{R_{MSB} + R_{EQ}} - \frac{1}{2} \right) \cdot V_{REF} \cdot e^{-t/\tau} \right) \cdot u(t) \quad (2)$$

, where τ is the time constant, and its value is equal to $(R_{MSB} + R_{EQ}) \cdot C/2$. The first term in Eq. (2), $V_{REF}/2$, is the final value of V_{DAC} to be settled to and the second term, which exponentially decays with τ , is the error term. As expected, with a small τ , the error quickly goes to zero and V_{DAC} settles to $V_{REF}/2$. Notice that there is one more design parameter that determines the initial value of the error, which is $R_{EQ}/(R_{MSB} + R_{EQ})$. If $R_{MSB} = R_{EQ}$, regardless of τ , the initial value of the error equals zero and one can obtain instantaneous settling. This observation can also be explained

intuitively as follows: The moment switching happens, the impedance of the DAC capacitors are almost negligible and the initial value of V_{DAC} is solely determined by resistive division of switch R_{ON} , which is $R_{EQ}/(R_{MSB} + R_{EQ}) \cdot V_{REF}$. However, as V_{DAC} settles, the impedance of the DAC capacitors become dominant over R_{ON} and the final value of V_{DAC} is determined by capacitive division, $C_{MSB}/(C_{MSB} + C_{EQ}) \cdot V_{REF}$. By setting $R_{MSB} = R_{EQ}$, the initial and final values of V_{DAC} are the same and settling time can be zero.

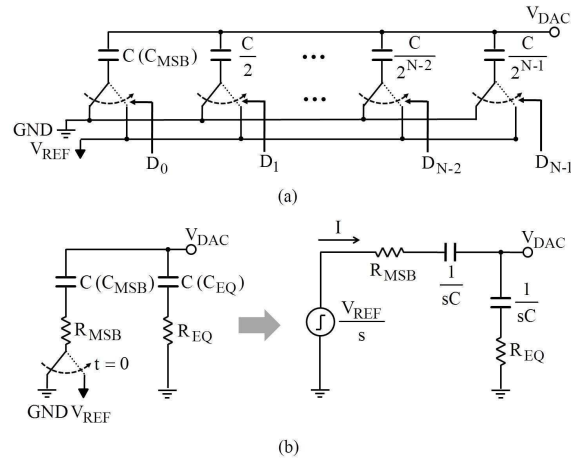


Fig. 1. (a) Simplified schematic of binary-weighted SC-DAC. (b) The equivalent circuit for MSB switching.

Fig. 2 shows the behavioural simulation results of SCDAC settling with mismatches between R_{MSB} and R_{EQ} . The sum of R_{MSB} and R_{EQ} was fixed to a reasonable value for 10-bit settling and the mismatches varied from 0.1% to 10%. As clearly shown in the simulation, settling time increases as the mismatch grows. Table I summarizes 10-bit level settling time with R_{MSB} and R_{EQ} mismatches. Based on the analysis, matching the initial and final values of V_{DAC} is critical for fast settling. This can be achieved by scaling down the switch R_{ON} by half as the size of the series DAC capacitor doubles, that is, the following condition should be met for a binary-weighted SCDAC.

$$R_{ON,MSB} = \frac{R_{ON,MSB-1}}{2} = \frac{R_{ON,MSB-2}}{2^2} = \dots = \frac{R_{ON,LSB}}{2^{N-1}} \quad (3)$$

However, DAC switches are implemented with both PMOS and NMOS transistors and R_{ON} matching between them cannot be guaranteed with process, voltage, and temperature (PVT) variations. The suggested design practice for fast settling is that, for a given time constant which might be determined by switch size and process, one needs to match R_{MSB} and R_{EQ} as much as possible.

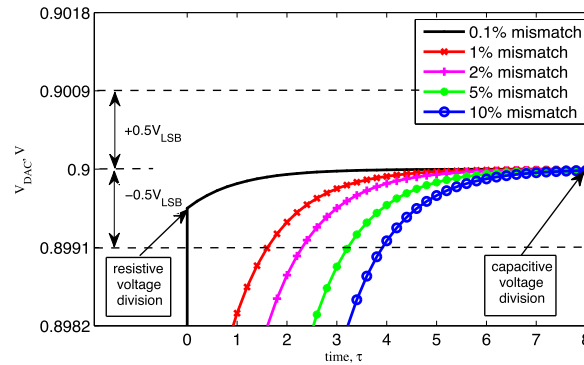


Fig. 2. Behavioural simulation results of DAC settling with R_{MSB} and R_{EQ} mismatches.

Table I. 10-bit level settling time with various mismatches.

Mismatch (%)	Settling time (τ)
less than 0.1957	0
1	1.63
2	2.33
5	3.24
10	3.94
20	4.63

3 Proposed circuit

In a standard CMOS process, the PMOS transistor sits in an N-well where the well potential can be independently controlled. By exploiting the fact that PMOS channel resistance changes with well potential [4] through the body-effect, the well potential can be adjusted to match the channel resistance of PMOS and NMOS transistors. Fig. 3 shows the proposed calibration circuit that improves matching of the channel resistances. It consists of an op-amp, PMOS and NMOS transistors, and four resistors. Transistors M1 and M2 mimic the switches that connect DAC capacitors to V_{REF} and GND , respectively. Assuming all the resistors have the same value, the negative input of the op-amp, V_- , is $VDD/2$ and the positive input, V_+ , is $VDD \cdot (R_{ON2} + R) / (R_{ON1} + 2R + R_{ON2})$, where R_{ON1} and R_{ON2} are the channel resistances of M1 and M2, respectively. If $R_{ON1} = R_{ON2}$, then V_+ should be equal to $VDD/2$ and the op-amp doesn't do anything. However, if $R_{ON1} \neq R_{ON2}$, V_+ deviates from $VDD/2$, the difference signal ($V_+ - V_-$) gets amplified and modifies the well potential of M1 transistor until R_{ON1} equals to R_{ON2} . Since DAC switches are implemented with the same unit transistor of M1 and M2 and the N-well of all PMOS transistors are biased by the op-amp, the resistance of PMOS transistors tracks that of NMOS transistors to compensate for PVT variations.

It should be mentioned that the PMOS transistor in the calibration circuit always operates in linear region, whereas the PMOS transistors in the DAC go through transition in operation from saturation to linear when turned on. Since the mismatch grows while the transistor is working in saturation,

the transistor should be going into the linear operation region as quickly as possible by pulling up the source terminal close to V_{REF} . In order to minimize the transition time, the transistor size has been increased until the parasitic capacitance limits V_{DAC} settling.

Note also that the op-amp only needs to supply a DC bias for the N-well, thus bandwidth requirements of the op-amp can be very relaxed and a simple differential pair, which has a DC gain of $34 \sim 54$ dB and draws only $20 \sim 30 \mu A$ from a $1.8 V$ supply, was used as an op-amp in the simulation. The op-amp output swing should maintain within $0.6 V$ from the $1.8 V$ supply in order to keep a strong reversed-bias between the N-well and substrate, which would otherwise increase the leakage current. This allows up to approximately 10% R_{ON} mismatch correction. The series resistors(R) connected to M1 and M2 are added to put M1 and M2 into the deep triode region just like the switch transistors in the DAC during normal operation. This reduces the systematic mismatch of R_{ON} between M1(M2) and DAC switches and improves matching of PMOS and NMOS channel resistance. The ratio of R to R_{ON} should be chosen with care because there is a tradeoff between the systematic mismatch and the op-amp DC gain. If the ratio is low, the systematic mismatch grows. On the other hand, if the ratio is high, the opamp gain should be increased to amplify a small error voltage at the opamp input. In this design, R was chosen to be approximately 10 times higher than R_{ON} of M1(M2) using simulations.

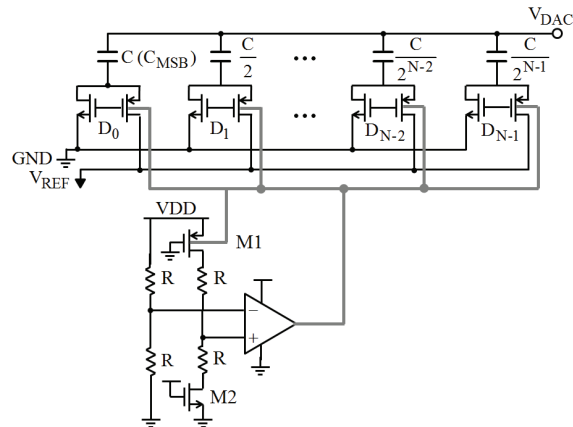


Fig. 3. Proposed mismatch calibration circuit.

4 Simulation results

The spice simulation results are shown in Fig. 4 and summarized in Table II. The circuits were designed with a $0.18 \mu m$ CMOS process and process variations are accounted for by running Monte-Carlo simulations. Supply and temperature were swept from 1.6 to $2.0 V$ and $-30^\circ C$ to $110^\circ C$, respectively. The worst case 3σ mismatch without the calibration circuit between R_{MSB} and R_{EQ} was about 8.23%. By using the calibration circuit, 8.23% mismatch reduces down to 1.19% as the op-amp gain increases from 34 dB to 54 dB. As

a result, the required settling time also improves by 51.6%. Further improvement can be achieved by using a high gain op-amp, but this may increase the power consumption and die area.

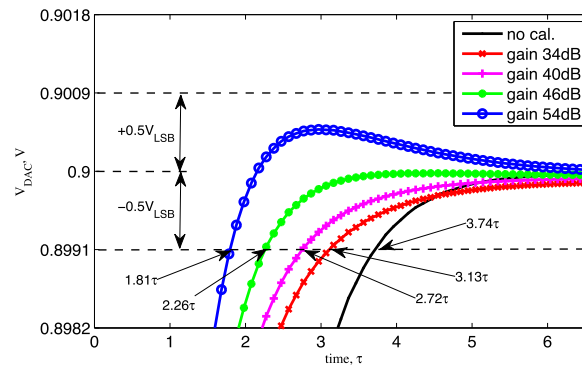


Fig. 4. Spice simulation results of SCDAC settling with various op-amp DC gains.

Table II. Summary of spice simulation results.

DC gain (dB)	mismatch (%)	settling time (τ)	improvement (%)
no calibration	8.23	3.74	—
34	4.47	3.13	16.3
40	2.96	2.72	27.3
46	1.87	2.26	39.6
54	1.19	1.81	51.6

5 Conclusion

Settling behaviour of the binary-weighted SCDAC has been analysed and an optimization technique of DAC settling has been proposed. A calibration circuit that can reduce settling time beyond the process limit by improving R_{ON} matching between PMOS and NMOS switch transistors was also presented and verified with simulations.

Acknowledgments

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