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Reliable and low error dual modular redundancy FIR filter with wide protection window

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Abstract: A reliable and low error dual modular redundancy FIR filter with wide protection window has been proposed in this paper. We improved the feedback mechanism by using a multiplexer to recover the soft error struck module from error immediately. The recovering time of soft error struck module can be shortened 87.18%, and the output error rate can be lowered by 4.5 times.

Keywords: DMR, FIR filter, soft error

Classification: Integrated circuits

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1 Introduction

CMOS technology scaling has continued over the last several decades, the feature size of the transistors have been reduced; decreasing critical charge at the circuit nodes lead to the increasing of soft error rate (SER), results in the reliabilities of the chip are seriously damaged [1]. Soft errors (SEs) would be the fifth major problem following the speed, chip area, power consumption, and yield in large-scale integration (LSI) design [2]. Around 90% of the SE-influenced circuits were memory circuits in the early years, and most of SE issues in memory elements have been discussed and overcome [3]. However, SE issues still exist in arithmetic circuits or digital signal processing (DSP) systems. Such design challenge is more difficult since an SE may turn into series of output errors through the propagation with carry signals in arithmetic circuits. Moreover, the circuit architectures in arithmetic circuits are usually irregular, which would increase the difficulty to solve it.

In order to mitigate the SER of arithmetical circuits, circuit redundancy is a common SE-tolerant strategy in circuit level and system level [4, 5] especially triple modular redundancy (TMR) [4]. However, the drawbacks of TMR are the significantly high overhead both on chip area and power consumption. In order to achieve SE-tolerant with less hardware overhead, dual modular redundancy (DMR) FIR filter was proposed in [6, 7]. The two redundancy FIRs are built with different designed structures, so that the mismatching patterns between their outputs are distinguishing when an SE occurs in each redundancy circuit. The structural DMR FIR [6] saves one redundancy module as compared with TMR and demonstrates superior SE immunity. However, two different types of FIR structures utilized in this design increased the design effort for other applications. Therefore, signal shaping DMR FIR [7] have been proposed designing in same FIR structure. With the distinguishing mismatching patterns, due to the SE exists in the module until the error vanishes by overflow, the error correction may misjudge at this time and would further cause the output error. As an SE occurred in signal shaping DMR FIR, even the circuit can determine the correct output by SE mitigation mechanism, the system requires some clock cycles to be recovered. If unprotected period is longer than the interval between two occurring SEs, the system would be failure. In this paper, we proposed a new SE tolerant DMR FIR with lower SER by restoring the output of SE-struck module by the correct one.

2 The proposed DMR soft error mitigation FIR filter

The proposed reliable and low error FIR filter is based on the design introduced in [7] to have one redundant FIR with the same architecture as the main FIR and with the improved feedback mechanism to construct a robust protection window. As a result, the FIR filters were able to provide more superior reliability. Fig. 1 shows the proposed soft-error tolerant FIR filter with wide protection window. It features the improved feedback mechanism by using multiplexer. First, there are two identical FIR modules on the

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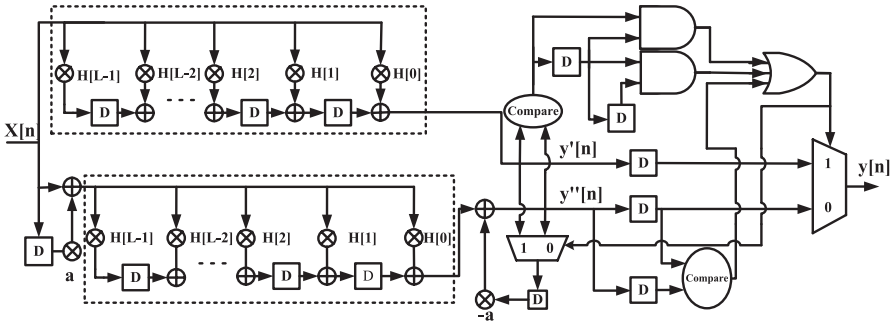

Fig. 1. The proposed soft-error tolerant FIR filter with advanced protection window.

left side in the dotted frames. In order to generate continuous-error output when an SE occurs, a one-tap FIR filter and a one-tap IIR filter are attached at the beginning and the end of the bottom module separately. Otherwise, when there is no error occurs in system, the bottom module retains the same outputs as the top one. The circuit shown in the right hand side is an error detection circuit for determining in which module the SE occurs and for selecting the correct module as the final output of the system.

When the system is in the error-free status, the output of the bottom FIR module is chosen as system output in default. If an SE occurs in the top FIR module, there is only one output error pattern occurred. On the contrary, a string of continuous errors is generated as the SE occurs in the bottom module. When the error detection circuit determined that the top module is in error, the system takes the output of the bottom module as the correct result and vice versa. The output function of the circuit is shown in Eq. (1):

$$y[n] = \begin{cases} y'[n], & for \quad y'[n-1] \neq y''[n-1], y'[n] \neq y''[n] \\ y''[n], & for \quad y'[n-1] \neq y''[n-1], y'[n] = y''[n] \\ & or \quad y'[n-1] = y''[n-1], y'[n] = y''[n] \end{cases} \tag{1}$$

The detection window of the design presented in [7] is relatively narrow because the length of the error string is varied according to the position which significant bit the SE occurs at. In other words, the system will misjudge and send the incorrect pattern to the system output when an SE occurs beyond the protection of the detection window. In order to loosen this limitation of the protection window, a multiplexer is added to select the appropriate feedback value of the bottom module; it imports the correct output from the top FIR module into the bottom one which an SE have occurred in. Hence there are only two continuous output patterns of the bottom FIR module in error before it is recovered from the SE effect. In this way, not only the error detection function remains intact, but also the recovering time of the circuit is considerably shortened, meanwhile.

Fig. 2 shows the operating sequence diagrams of the soft-error tolerant FIR filters proposed in [6, 7] and this paper, respectively. The first row shows the outputs of top FIR module and the second row shows the outputs of bottom module. The last row is the final outputs of the FIR. The outputs in

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error are marked with gray background. In this example, the first SEs occur in both bottom modules of these FIR designs at the $N+1^{th}$ pattern, and the second SEs occur in both top modules at the $N+4^{th}$ pattern. In signal shaping DMR FIR [7], once the SE occurred at $N+1^{th}$ cycle, the error-free output from the top module is chosen as the output of the system. However, before the bottom module is recovered from the continuous error, the SE occurred in the top module at $N+4^{th}$ pattern would lead to misjudgment in DMR FIR and cause a malfunction in its output. In contrast, when the same case occurs on the structural DMR FIR [6] design, the number of continuous error patterns can be restricted in three by using the cascaded structure, therefore the correct output could be chosen from the bottom FIR module when SE occurred at $N+4^{th}$ pattern. In our proposed soft-error tolerant DMR FIR, we further restrict only two continuous error patterns occur in the bottom FIR module by improving the feedback mechanism by using a multiplexer. The bottom FIR module is recovered immediately; therefore, the DMR FIR can behave normally even the SE occurs in the top FIR module at $N+4^{th}$ pattern.

FIR Top	FIR[N]	FIR[N+1]	FIR[N+2]	FIR[N+3]	FIR[N+4]	FIR[N+5]	···	FIR[N+K+1]	···	FIR[M]
FIR Bottom	IIR[N]	IIR[N+1]	IIR[N+2]	IIR[N+3]	IIR[N+4]	IIR[N+5]	···	IIR[N+K+1]	···	IIR[M]
OUT [7]	IIR[N-1]	IIR[N]	FIR[N+1]	FIR[N+2]	FIR[N+3]	FIR[N+4]	···	FIR[N+K]	···	IIR[M-1]

FIR Top	FIR[N]	FIR[N+1]	FIR[N+2]	FIR[N+3]	FIR[N+4]	FIR[N+5]	···	FIR[N+K+1]	···	FIR[M]
FIR Bottom	IIR[N]	IIR[N+1]	IIR[N+2]	IIR[N+3]	IIR[N+4]	IIR[N+5]	···	IIR[N+K+1]	···	IIR[M]
OUT [6]	IIR[N-1]	IIR[N]	FIR[N+1]	FIR[N+2]	IIR[N+3]	IIR[N+4]	···	IIR[N+K]	···	IIR[M-1]

FIR Top	FIR[N]	FIR[N+1]	FIR[N+2]	FIR[N+3]	FIR[N+4]	FIR[N+5]	···	FIR[N+K+1]	···	FIR[M]
FIR Bottom	IIR[N]	IIR[N+1]	IIR[N+2]	IIR[N+3]	IIR[N+4]	IIR[N+5]	···	IIR[N+K+1]	···	IIR[M]
OUT Proposed	IIR[N-1]	IIR[N]	FIR[N+1]	FIR[N+2]	IIR[N+3]	IIR[N+4]	···	IIR[N+K]	···	IIR[M-1]

Fig. 2. The timing diagram of the proposed soft-error tolerant FIR filter.

3 Results and performance comparison

To prove the design concept, we evaluate the performance index in terms of soft-error tolerance, recovering time, hardware overhead, operating speed and power consumption of the proposed circuit in comparison with the prior-art designs while the soft error rates are 0.01%, 0.05%, 0.1%, 1%, and 5%, respectively. The SER comparison results are shown in Fig. 3. At different SERs, the output error rate of the proposed design is approximate 4.5 times less than the design in [7].

To compare the recovering time of the circuit, we developed the DMR FIRs with Matlab and injected the SE into both bottom FIR modules of the two designs separately to generate continuous output errors. As shown in

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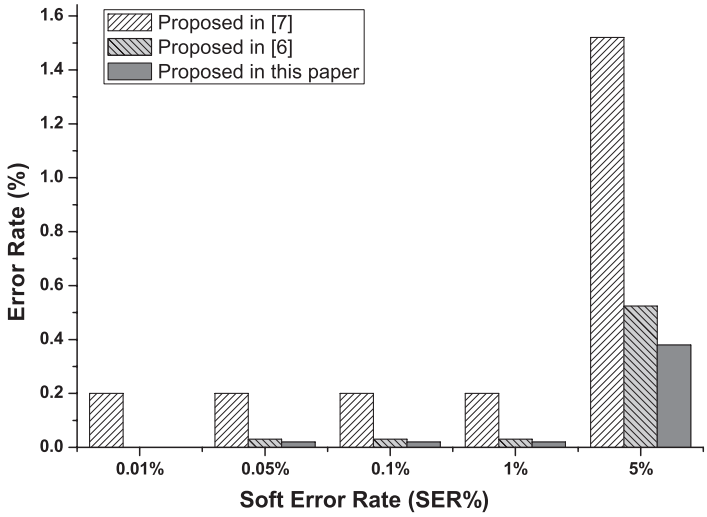

Fig. 3. Comparisons of recovering time for prior DMR FIR designs and proposed design.

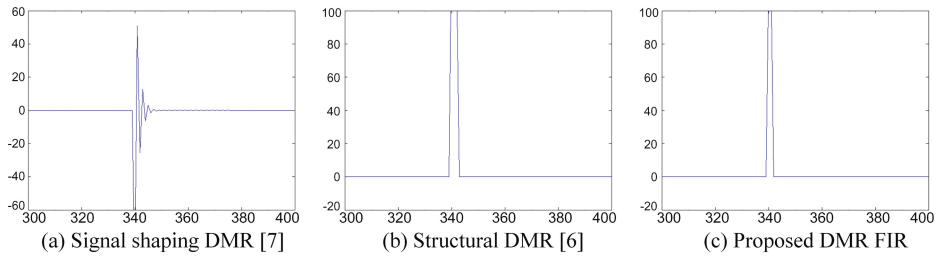

Fig. 4. Comparisons of recovering time for prior DMR FIR designs and proposed design.

Fig. 4(a), the continuous error is produced after SE occurs in the bottom FIR module of the signal shaping DMR FIR design [7]. Once an SE occurs in the prior bottom FIR module, the error will propagate stage by stage in the feedback loop until the error overflows in the bottom FIR module, which would take several clock cycles. In the proposed DMR FIR design, the correct output of the top FIR module is chosen as the feedback value to recover the error output of the bottom FIR module instantly. As shown in Fig. 4(c), the output error can be recovered in two clock cycles. In the proposed design, the average error recovering time is reduced from 15.6 clock cycles to two, which is shortened 87.18% as compared with singal shaping DMR FIR [7]. As compared with and with structral DMR FIR [6], the error recovering time can also be shorten by 33.33%.

We finally implemented the proposed FIR filter in tsmc 0.18 µm CMOS technology. Table I shows the comparison of power, area and normalized error rate between different designs of FIR filters. Under nearly the same power consumption and chip area, the proposed DMR design takes much less SE recover time as compared with signal shaping DMR design [7]. The average SER in the proposed design can be further decreased by 4.5 times. The chip layout of the proposed soft-error tolerant FIR filter is shown in Fig. 5.

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Table I. Comparison of power, area and error rate

	Power (mW)	Area (μm^2)	Error Rate
Conventional FIR	3.76	45521	100%
Structural DMR [6]	9.28	108215	3.71%
Signal Shaping DMR [7]	9.28	108098	15.39%
Proposed in this paper	9.29	109016	3.44%

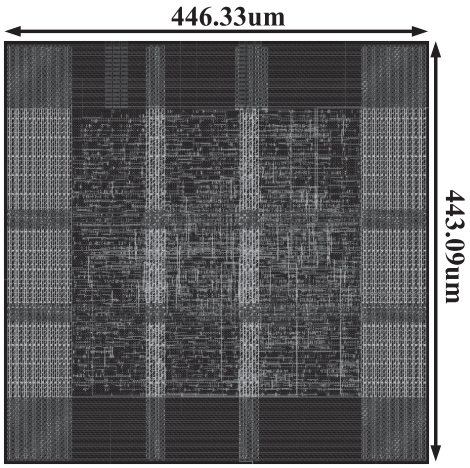

Fig. 5. The layout of the proposed SE tolerant FIR filter.

4 Conclusion

The proposed soft error-tolerant DMR FIR filter can enhance the reliability and lower output error rate as compared with the prior design by introducing the feedback mechanism. The proposed feedback mechanism can restrict the continuous error output in two patterns; therefore the protection window can be enlarged. The proposed design has been implemented in tsmc 0.18 µm process, where 96.56% SEs can be filtered.

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