Skew violation verification in digital interconnect signals based on signal addition

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Abstract: Signal integrity perturbations are unavoidable in current high performance circuits implemented in nanometer technologies. In this paper, a novel methodology based on the signal addition of two digital signals to verify skew violations is proposed. This methodology allows the implementation of a compact sensor for on-chip verification of the skew in digital interconnect signals. The monitor is implemented in a commercial CMOS 65 nm technology. The compact size of the monitor allows its use for verifying several internal nodes with low area penalty. The impact of process, power supply voltage and temperature variations (PVT) on monitor resolution is analyzed. Simulation results show that the monitor is effective for identifying abnormal skews due to signal integrity issues.

Keywords: signal integrity, skew, built-in monitors, process variations

Classification: Integrated circuits

References

[1] A. Attarha and M. Nourani: Int. Test Conf. (2001) 305.
[2] Q. Xu, Y. Zhang and K. Chakrabarty: ACM Trans. Des. Autom. Electron. Syst. **14** [1] (2009) 4. DOI:10.1145/1455229.1455233
[3] M. Becer, R. Vaidyanathan, C. Oh and R. Panda: IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. **23** (2004) 488. DOI:10.1109/TCAD.2004.825855
[4] V. Petrescu, M. Pelgrom, H. Veendrick, P. Pavithran and J. Wieling: IEEE Int. Solid-State Circuits Conf. (2006) 2220. DOI:10.1109/ISSCC.2006.1696283
[5] M. H. Tehranipour, N. Ahmed and M. Nourani: IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. **23** (2004) 800. DOI:10.1109/TCAD.2004.826540
[6] V. Champac, V. Avendano and J. Figueras: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **18** (2010) 256. DOI:10.1109/TVLSI.2008.2010398
[7] C. Metra, M. Favalli and B. Ricco: Int. Test Conf. (1998) 524.
[8] A. Zenteno, V. Champac and J. Figueras: Electron. Lett. **38** (2002) 686. DOI:10.1049/el:20020478

[9] B. P. Wong, A. Mittal, Y. Cao and G. Starr: *Nano-CMOS Circuit and Physical Design* (Wiley-Interscience, 2004) 255.

[10] N. Hernandez and V. Champac: IEEE Computer Society Annual Symp. on VLSI (2008) 151. DOI:10.1109/ISVLSI.2008.93

[11] S. G. Ghosh, S. Bhunia, A. Raychowdhury and K. Roy: IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. **25** (2006) 2934. DOI:10.1109/TCAD.2006.882523

[12] K. A. Jenkins, K. L. Shepard and Z. Xu: IEEE Custom Integr. Circuits Conf. (2007) 157. DOI:10.1109/CICC.2007.4405703

[13] M. Sasaki, N. Ngoc Mai Khanh and K. Asada: IEEE Asian Solid-State Circuits Conf. (2010) 1. DOI:10.1109/ASSCC.2010.5716594

1   Introduction

Continuous advancements in semiconductor technologies have resulted in faster circuits with more integrated functionality. At the same time, interconnect signal integrity perturbations have become more significant with technology scaling [1]. These perturbations affect the voltage noise levels and timing of the interconnect signals. Signal integrity issues are even more severe in core-based system-on-chip (SoC) designs [2]. In order to assure signal quality, designers need to consider circuit layout design, placement and routing, and circuit simulation [3]. All possible operational conditions are unlikely to be taken into account by the present state-of-the-art CAD tools. Consequently, chips may fail although they passed standard test procedures [4]. External at-speed testing may not be possible for the newest technologies, and verification of some internal nodes could de difficult. Hence, built-in methodologies are required to verify signal integrity violations more accurately [1, 5, 6]. Verification of the signal integrity using on-chip monitors appears as a good alternative for present and future nanometric integrated circuits. In [7], the authors proposed a delay detector based on the idea to apply error detecting code concepts to signal transition checking. In [1], a BIST-based test methodology that includes a special sensing cell to detect skew violations on the interconnects is proposed. In [8], the authors proposed a method to detect inter-signal delay violations of two signals X,Y. The method is based in defining the X-Y representation of the non-defective curves. A novel built-in delay sensor has been presented in [5]. This sensor is intended to be used in delay fault testing using test point insertion.

In this paper, a novel methodology to verify the skew, due to signal integrity loss, in digital interconnect signals is proposed. It is based on the signal addition of two opposite digital signals. Their sum is analyzed in order to discriminate between fault-free behavior and faulty behavior. A detailed theoretical analysis of the proposed signal addition methodology is made. A compact skew monitor, based in the signal addition, is proposed. The rest of the paper is organized as follows. Section 2 presents the requirements on signal skew quality. Section 3 presents a theoretical analysis of the proposed skew verification methodology. Section 4 presents a compact monitor imple-

menting the proposed methodology and its behavior is illustrated. In Section 5 the monitor testing procedure is discussed. Section 6 presents the cost analysis and comparison with prior work. Finally, the conclusions are presented in Section 7.

2 Signal skew quality

A signal with good signal integrity quality means a signal arriving at the receiver location at proper tolerable time skews and with adequate voltage levels. Because of the complexity of nanometer interconnect architectures, timing violations due to the interconnect has become an important contributor to the signal integrity loss.

Modern nanometric integrated circuits have a high number of interconnects with different characteristics. Because of this only those interconnect signals more susceptible to suffer signal integrity loss should be considered for signal integrity verification. Global interconnects are good candidates for signal integrity loss [9]. Among them, interconnects communicating cores in SoC systems have signals prone to suffer signal integrity issues [1, 2]. Signals in data/address buses and in clock distribution are also susceptible to signal integrity loss.

3 Proposed skew verification methodology

In this work, a new methodology to verify the timing behavior of digital interconnect signals is proposed. This is based in the addition of two digital signals with opposite transitions [10]. This methodology will be explained for different possibles cases:

3.1 Case I: signals without skew

Let us denote by $X(t)$ and $Y(t)$ the time varying voltages of the signals at nodes X and Y having opposite transitions with equal rise and fall times (See Fig. 1). When there is no skew, the transitions of both signals begin and end at the same time position. Two possible regions of interest exist, *Region 1* and *Region 2* (See Fig. 1). Let us analyze Region 1 where the signals $X(t)$ and $Y(t)$ make negative and positive transitions, respectively. In Region 1 (See Fig. 1), the signals $X(t)$ and $Y(t)$ can be described by

$$X(t) = V_{OH} + \frac{V_{OL} - V_{OH}}{t_{f_x}} t, \tag{1}$$

$$Y(t) = V_{OL} + \frac{V_{OH} - V_{OL}}{t_{r_y}} t. \tag{2}$$

where t_{f_x} and t_{r_y} stand for the fall and rise times of X(t) and Y(t), respectively.

The sum ($\sigma(t)$) of signals X(t) and Y(t) is given by

$$\sigma(t) = X(t) + Y(t) = V_{OH} + V_{OL}. \tag{3}$$

This equations means that the sum of two digital signals having opposite transitions without skew between them gives a constant voltage value in-
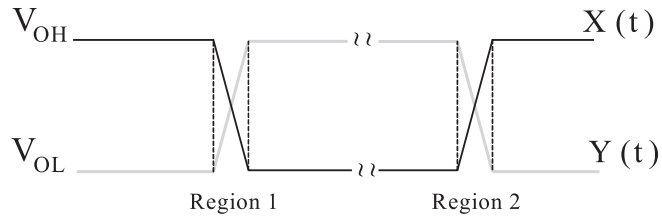
Fig. 1. Two signals with opposite transitions without skew

dependently of the states of the signals. This voltage will be called the *stable sum value*. The analysis is similar for Region 2.

3.2 Case II: positive skew, Δt > 0, *Region 1*

Let us assume that $X(t)$ is our reference signal that does not suffer skew. For a positive skew ($\Delta t > 0$), the $Y(t)$ arrives later with respect to the reference signal X(t). Δt gives the amount skew. Two regions of interest appear, *Region 1* and *Region 2*. In this subsection, *Region 1* is analyzed. *Region 2* can be analyzed in a similar way. Fig. 2a shows a closer view of *Region 1*. The analysis for this region is divided into three sections.

3.2.1 Section A

Signal X(t) changes with time while signal Y(t) is constant at V_{OL} (See Fig. 2). Making the addition of X(t) and Y(t) their sum $\sigma(t)$ gives

$$\sigma(t) = V_{OH} + V_{OL} + \frac{V_{OL} - V_{OH}}{t_{f_x}} t \tag{4}$$

In this case, the sum deviates from the stable sum value according to the rightmost term in Eq. (4). This term represents the voltage deviation $\Delta V(t)$ from the ideal constant value. Because of this the sum decreases linearly with time (See Fig. 2). The maximum value of this deviation (ΔV) occurs at the end of section A where t is equal to Δt. Thus

$$\Delta V = \lim_{t \to \Delta t} \Delta V(t) = \lim_{t \to \Delta t} \frac{|V_{OL} - V_{OH}|}{t_{f_x}} t = \frac{\Delta t}{t_{f_x}} |V_{OL} - V_{OH}| \tag{5}$$

From Eq. (5) it can be stated that ΔV has a linear dependence with Δt whereas it is inversely proportional to the duration of the falling edge of the reference signal X(t).

3.2.2 Section B

Both signals X(t) and Y(t) change with time (See Fig. 2). Signal X(t) is described by

$$X(t) = V_{OH} - \Delta V + \frac{V_{OL} - V_{OH}}{t_{f_x}} t \tag{6}$$

and the signal Y(t) is described by equation 2.

Making the addition of X(t) and Y(t), and using the fact that the fall and rise time of X(t) and Y(t) are equal, their sum gives
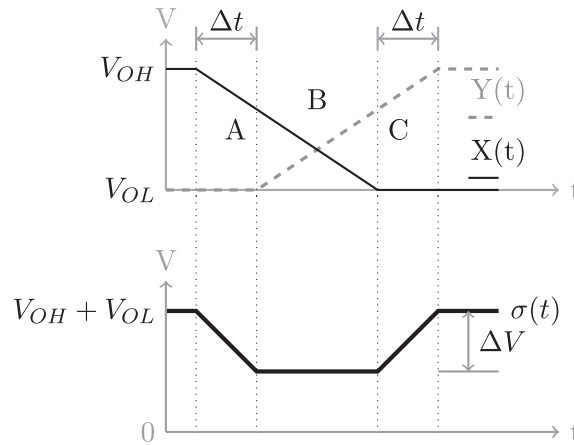
$$\sigma(t) = V_{OH} + V_{OL} - \Delta V \tag{7}$$

Fig. 2. Sum behavior of $X(t)$ and $Y(t)$ in *Region 1*

From this equation, it can be stated that the sum is a constant voltage level in Section B (See Fig. 2).

3.2.3 Section C
Signal X(t) is constant at V_{OL} while signal Y(t) changes with time (See Fig. 2). Making the addition of X(t) and Y(t) their sum gives

$$\sigma(t) = V_{OH} + V_{OL} - \Delta V + \frac{V_{OH} - V_{OL}}{t_{r_y}} t \qquad (8)$$

From this equation it can be stated that the sum of the addition increases with time in Section C as illustrated in Fig. 2. The stable sum value occurs when the signal $Y(t)$ arrives at its stable state $(V_{OH} + V_{OL})$.

3.3 Case III: positive skew, Δt > 0, Region 2
The analysis for a positive skew in *Region 2* can also be divided in three sections (A, B and C). A similar behavior to *Region 1* occurs but in this case an overshoot above $(V_{OH} + V_{OL})$ appears.

4   Proposed skew monitor

4.1   Verification schema
The monitor verifies the signals of two internal nodes having opposite transitions (See Fig. 3). The patterns applied at the inputs of the circuit under verification should maximize signal integrity loss [1]. In our verification methodology, signal propagation is not required because on-chip delay monitors are used to observe the internal signals.

The verification architecture to read-out the information at the output monitor cells can be adapted from [1]. Each output of the monitors goes to a flip-flop. The flip-flop outputs are inputs to an AND function. Inverter gates can be added to assure a 0 logic state at the AND output when there is no signal integrity violation. A violation is identified when the AND output goes to 1 logic.
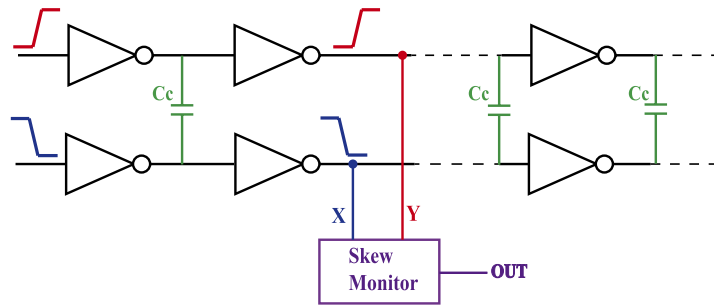
Fig. 3. Schematic diagram of the verification method.

4.2 Skew monitor behavior

The schematic of a novel skew monitor, based in the addition operation of two digital signals having opposite transitions, is shown in Fig. 4. M1 and M2 are the sensing transistors, M3 is the control transistor, INV1 is the feedback inverter that works as an amplifier, INV2 is the discriminating inverter and INV3 is the level-restoring inverter. The monitor is able to verify both positive and negative skews. The addition of signals X and Y is reflected at node-σ. For stable values of X and Y, node-σ has a voltage value called the stable sum value. This is below the threshold voltage of INV2. Because of this node-OUT is at a low logic state.
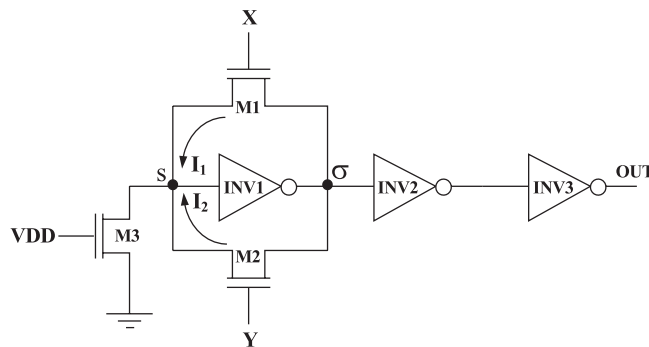

Fig. 4. Schematic of the skew monitor.

Let us consider the case of without skew between the input signals. During the transition of the input signals, sensing transistor M1 (M2) is turning OFF (ON) while transistor M2 (M1) is turning ON (OFF). The decrement (increment) of current $I1$ ($I2$) is compensated by the increment (decrement) in current $I2$ ($I1$). Because of this the current supplied to node S essentially remains constant, and the voltages at node-S and node-σ remain at the stable sum value. V_{OUT} remains at a low logic level. When there is a positive skew between the input signals, transistor M1 is turning OFF while transistor M2 is still OFF. Because of this less current is supplied to node-S, and an undershoot occurs at node-S. The feedback loop is also broken as a consequence of the skew. In other words, both M1 and M2 sensing transistors are turned OFF at the same time. Because of this the undershoot voltage at node-S is amplified by the feedback inverter INV1. If the overshoot at node-σ has

sufficient energy (height and width), a pulse appears at node-OUT indicating that a skew violation has occurred. Otherwise, node-OUT remains at a low logic state.

4.3 Performance evaluation of the skew monitor

The monitor has been designed with a commercial CMOS 65 nm technology to verify positive and negative skews for Region 1 and Region 2 (See Fig. 1) respectively. The minimum detectable skew (resolution) has been set to 20 ps. Table I shows the transistor channel widths for the skew monitor (See Fig. 4). The channel length (L) for INV1 is twice the minimum allowed by the technology, while for the rest of transistors, L is the minimum. The control transistor has a reference voltage of $V_{DD} = 1.2\,\text{V}$ at its input. Without loss of generality, it is assumed that the signal at node-Y is the one suffering skew.

Table I. Monitor transistors sizes.

Device	M1	M2	M3	β_{INV1}	β_{INV2}	β_{INV3}
W (nm)	700	700	210	3	2.2	2.2

Fig. 5 shows the monitor behavior without and with positive skew. For the case without skew, a small undershoot occurs at node-S which is not amplified by the feedback inverter. The voltage at node-σ is below the threshold voltage of the INV2. Hence, no changes occur at the monitor output. For the case of a positive skew (See Region 1 in Fig. 5), a more significant undershoot occurs at node-S which is amplified by INV1. The overshoot at node-σ has sufficient energy to produce a state change at the output of inverter INV2, and a pulse appears at node-OUT. Hence, a skew violation is detected.

The monitor does not detect the positive skew for Region 2 (See Fig. 5). While only transistor M2 is ON, it supplies all the current to node-S. As a consequence, the voltage at node-S does not change. Then, transistor M1 turns ON while transistor M2 is still ON. Because of this the loop does not break, and non significant voltage change appears at node-S and node-σ.

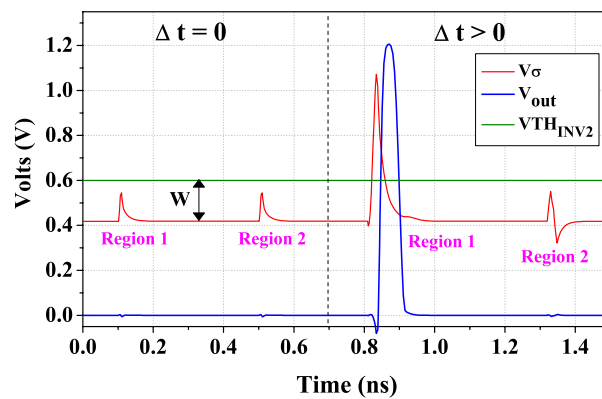### 4.4 Monitor characterization

The acceptable/non acceptable skew between the two signals under analysis can be modified varying the sizes of INV1, INV2, M1, M2 and M3.

4.4.1 Feedback inverter

The beta ratio of the feedback inverter (β_{INV1}) significantly influences the stable sum value at node-S. It defines the amplification of the signal at node-S. INV1 can be sized for a higher stable sum value allowing detection of smaller delays but at the same time it must be assured that the overshoot that appears for an acceptable skew will not detected. Fig. 6a shows the monitor minimum detectable delay as a function of β_{INV1}. It is observed that the minimum detectable delay decreases as β_{INV1} increases, improving the monitor resolution.
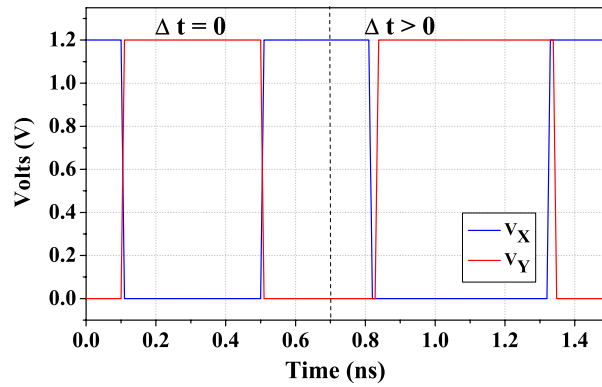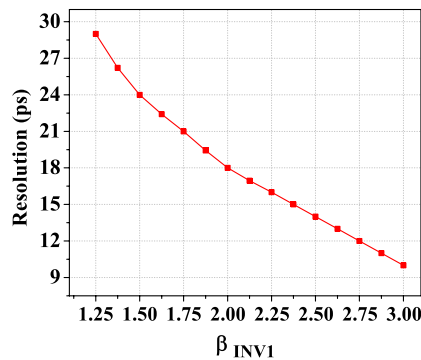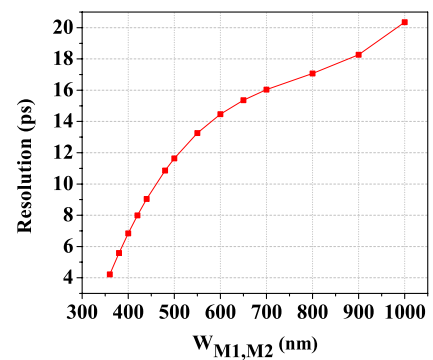
(a) Input Signals.

(b) Monitor response.

Fig. 5. Monitor behavior for the cases without skew and with a positive skew violation.

(a) Discriminating Inverter   (b) Sensing Transistors

Fig. 6. Monitor characterization.

4.4.2   Sensing transistors

The size of the sensing transistors $M1$ and $M2$ (See Fig. 4) significantly influences the value of the minimum detectable skew. Fig. 6b shows a plot of the minimum detectable skew as a function of the channel width of M1 and

M2 ($W_{M1,M2}$). It is observed that as $W_{M1,M2}$ increases the minimum detectable skew increases. Furthermore, for $W_{M1,M2}$ less than 400 nm, is possible to detect delays less than 6 ps.

4.4.3 Discriminating inverter and control transistor

Sizing of the discriminating inverter INV2 and the control transistor M_3 also influences the monitor behavior. The threshold voltage of the discriminating inverter (V_{TH}^{INV2}) and the stable sum value at node-σ defines the *critical window* of size **W** (See Fig. 5). A skew violation is detected when the overshoot above the stable sum value has sufficient energy to cross this window and to change the output logic state of INV2. The monitor resolution improves as the size of this window is decreased. Thus, the monitor resolution depends on the beta ratio of INV2 (β_{INV2}). As β_{INV2} decreases, the V_{TH}^{INV2} also decreases reducing the size of W. Hence, the monitor resolution improves as β_{INV2} decreases. On the other hand, the high resistance of the control transistor M_3 works as an active load and allows proper biasing of the feedback inverter.

4.5 Impact of PVT variations

The behavior of the proposed monitor has been evaluated for process, power supply voltage (V_{DD}) and temperature variations. The V_{DD} was varied $+/-16\%$ of the nominal V_{DD} and the temperature was varied from $-125\,°C$ to $150\,°C$. Process parameter variations due to the manufacturing process also may cause departure of the monitor behavior from the nominal values. Variations in channel length and width, gate oxide thickness and random doping fluctuations of threshold voltage affects circuit performance. According to the information supplied by the foundry a normal distribution is used with the following tolerances: 10% for the gate oxide thickness, 20% for threshold voltage, and 15% for channel length and channel width. To analyze the impact of process parameter variations on the monitor minimum detectable delay, the effect of local and global variations of parameters have been considered concurrently (See Eq. 9). The global variation component is generated for each Monte Carlo simulation for all monitor's transistors while the local variation component is generated for each transistor.

$$P_{ij} = P_{nominal} + \Delta P_{global,j} + \Delta P_{local,ij} \tag{9}$$

P_{ij} is the parameter value for the ith transistor during the jth Monte Carlo simulation. $P_{nominal}$ is the nominal parameter value, $\Delta P_{global,j}$ is the global variation component, and $\Delta P_{local,ij}$ is the local variation component. Using Analysis of Variance (ANOVA), a Pareto Chart of effects has been constructed to observe which component of the monitor has a major impact on the mean (See Fig. 7a) and variance (See Fig. 7b) of the resolution distribution. It can be observed that variations of the parameters of the feedback inverter (INV1) have a major effect on the monitor resolution. Fig. 8 shows the minimum detectable delay of the monitor as a function of V_{DD} and temperature. It is observed that the minimum detectable delay increases as V_{DD}

decreases lowering monitor resolution (See Fig. 8a). The minimum detectable delay increases as the operating temperature increases (See Fig. 8b). Table II shows the overall impact of process, power supply voltage and temperature on the monitor resolution distribution. It is observed that V_{DD} not only impacts the mean (μ_{Reso}) of the monitor resolution, but also it impacts the standard deviation (σ_{Reso}). In other words, as V_{DD} decreases, the variability of the monitor detectable delay increases. On the other hand, the standard deviation of the minimum detectable delay also increases as temperature increases. However, the impact of the temperature on the variability of the monitor resolution is lower than the impact of V_{DD}. From this results, the monitor should be designed for a minimum desired detectable skew under worst case conditions. This allows to have a compact monitor to be used to verify several nodes.

5 Monitor testing

Three test vector pairs are required for fault detection in all the components of the monitor. The test vectors are applied to X and Y inputs (See Fig. 4) while the gate input of M3 is connected to V_{DD}. For all the three test vector pairs, the same same initializing first vector ($XY = 11$) is applied to establish the operating voltages at nodes S and σ (See Fig. 4) below V_{TH}^{INV2} which sets the monitor output (OUT) at logic '0'. If OUT is not set at logic '0', there is a fault. This initializing vector allows to test correct behavior of the analog components (M3 and INV1) of the sensor, and stuck-off (stuck-on) faults at the Pmos (Nmos) and Nmos (Pmos) transistors of INV2 and INV3, respectively. For the first test vector pair, a second vector $XY = 00$ is applied to produce a transition $0 \rightarrow 1$ at OUT. If the monitor output remains at logic 0, there is a fault. This vector allows to test stuck-on faults at M1 and M2, and stuck-off (stuck-on) faults at Nmos (Pmos) and Pmos (Nmos) transistors of INV2 and INV3, respectively. For the second test vector pair, a second vector $XY = 10$ is applied. OUT should remain at logic '0' for the fault-free case. This vector allows to test a stuck-off fault at M2. Finally, for the third test vector pair, a second vector $XY = 01$ is applied to allow to test a stuck-off fault at M1.
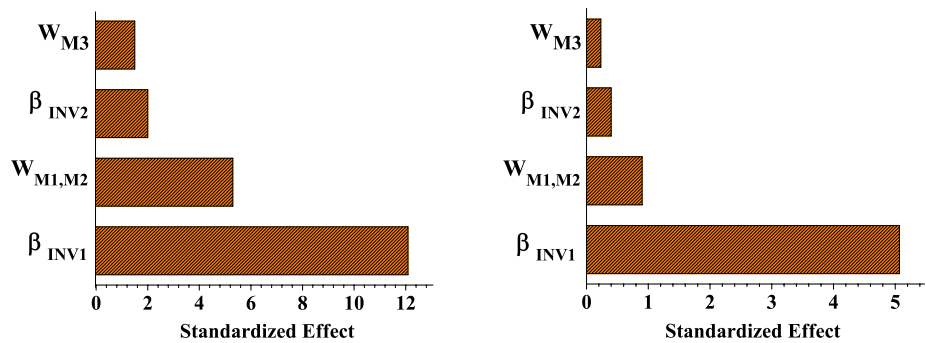
(a) ANOVA of the resolution mean. (b) ANOVA of the resolution variance

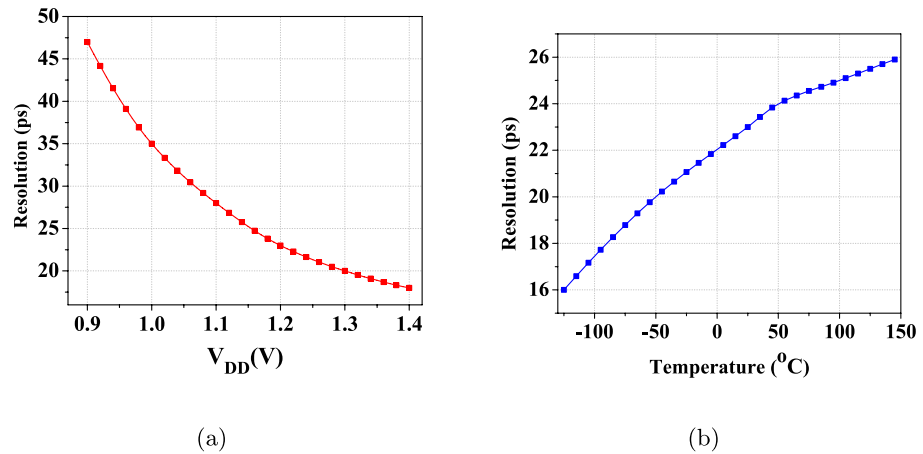**Fig. 7.** Pareto chart of effect of the monitor resolution.

(a)   (b)

Fig. 8.   Influence of V_{DD} and temperature variations.

Table II.   Impact of PVT variations on monitor resolution.

Temp (°C)	−125 °C			25 °C			100 °C		
V_{DD} (V)	1.4	1.2	1	1.4	1.2	1	1.4	1.2	1
μ_{Reso} (ps)	10.2	14.2	24.4	15.2	20.1	31	16.7	24.9	34.1
σ_{Reso} (ps)	1.01	2.3	5.3	2.04	3.1	6.13	2.2	3.35	6.2

6   Cost and comparison with prior work

6.1   Cost

The cost of the proposed skew monitor estimated in terms of area and delay penalization. Using a commercial CMOS 65 nm technology, the estimated area for the skew monitor is $16\,\mu m^2$. The added capacitance to each sensing line due to the gate capacitance of the monitor sensing transistors is $1.1\,fF$. The delay penalization due to monitor loading for different interconnect lengths is given in Table III. The delay penalization decreases for longer interconnects.

Table III.   Delay cost due to monitor loading

Length (mm)	1	2	3	4	5
Delay Cost (%)	0.16%	0.14%	0.11%	0.10%	0.08%

6.2   Comparison with prior work

Our proposal is compared with other related work. Attarha et al. [1] presented a skew detector cell based in a NOR gate and a delay generator circuit. Detection is based in the skew (delay) comparison of the signal under analysis with the reference signal generated with the delay generator circuit. Zenteno et al. [8] proposed a method to detect inter-signal delay violations based in the analysis of the shape of the X-Y representation of the signals under analysis. The sensor cell proposed by Tehranipour et al. [5] is based in transmission gates input stage and a XNOR gate implemented in dynamic precharged

logic. The test clock is used to create a window which determines the acceptable skew region. A delay-sensor logic to be used in a delay fault testing methodology was proposed [11]. This delay-logic sensor is suited for delay testing in external (ATE-based) and scan-based BIST. In [12] and [13] used a jitter measurement circuit to measure clock skew. There are a D-FF, a constant inverter delay chain, and an error latch counter for each test point of interest of the clock tree. Our work presents a novel methodology for verifying the skew of digital signals based in the addition of the digital signals at two internal nodes X and Y. This methodology has allowed the implementation of a compact sensor for on-chip verification of the skew in digital interconnect signals. The compact size of the monitor allows its use for verifying several internal nodes with low area penalty.

7 Conclusion

A novel methodology to verify skew violations in digital interconnect signals, due to signal integrity perturbations, has been proposed. The method is based on the signal addition of two digital signals having opposite transitions. A compact skew sensor has been implemented using the proposed methodology. The same monitor is able to verify both positive and negative skews. The cost of the proposed strategy is analyzed in terms of area overhead and delay penalization. The delay and area penalization are small. The behavior of the monitor in the presence of power supply voltage, temperature and process variations has been analyzed. The simulation results show that the skew monitor is able to detect small skews.