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# A design methodology for SAR ADC optimal redundancy bit

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**Abstract:** This paper presents a design method of SAR ADC (Successive Approximation Register Analog-to-Digital Converter ADC) utilizing redundancy bits. In general, binary search algorithm is used as a conventional SAR ADC operation algorithm. It's possible to realize a high-speed SAR ADC by using non-binary search algorithm which is realized by adding redundancy bits. However, the A/D conversion time varies depending on the number of redundancy bits. Therefore, in order that the conversion time is the shortest, it's necessary that an appropriate amount of redundancy be added. We show a methodology of finding the appropriate number of redundancy bits.

**Keywords:** SAR ADC, non-binary algorithm, redundancy, optimization

**Classification:** Electron devices, circuits, and systems

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## 1 Introduction

In recent year, due to the development of the mixed signal systems-on-chip, analog-to-digital converters (ADCs), which are used between the RF front-



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end and the baseband, are demanded for high performance. However, because of the progress of complementary metal-oxide semiconductor (CMOS) nano-fabrication technologies, the interest in successive approximation register (SAR) ADCs is increasing. The reason is that SAR ADCs can operate without an operational amplifier (op-amp) and at low power consumption.

As shown in Fig. 1, a SAR ADC consists of a sample and hold (S/H) circuit, a comparator, a digital-to-analog converter (DAC), and a SAR logic circuit. It generally operates according to binary search algorithm which realizes $N$-bit resolution by $N$ comparisons. In order to realize high-speed SAR ADC, several papers propose operation systems which are realized by non-binary search algorithm [1, 2, 3]. This algorithm is realized by adding redundancy bits to the resolution. In other words, the algorithm realizes $N$-bit resolution by $M$ comparisons ($N \leq M$) and the value to be obtained by subtracting $N$ from $M$ indicates the number of redundancy bits. For improving the A/D conversion time further, we proposed a design technique and built an optimization system [4]. However, it is difficult to find the appropriate number of redundancy bits for getting the shortest SAR ADC conversion time because the conversion time varies depending on the number of redundancy bits and there are vast amounts of data. Therefore, it is necessary that the redundancy bits should be appropriately added in order that the conversion time is the shortest. In this paper, we proposed a methodology of searching the optimal number of redundancy bits.

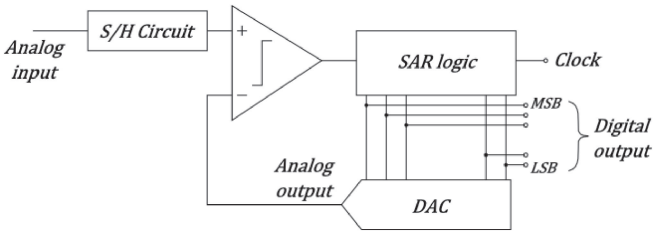


**Fig. 1.** Block diagram of a conventional SAR ADC.

## 2 Methodology

We propose a methodology to find the appropriate number of redundancy bits.

$q(k)$ is define as a tolerance range of a $k$-th phase. This range indicates the maximum value of the allowable error between the voltage output of DAC and the reference voltage of $k$-th phase, in the $k$-th comparison. In other words, in order to obtain correct SAR ADC output, the following equation should be satisfied when the $k$-th comparison is performed as shown Fig. 2.

$$|V_{DAC} - V_{ref}(k)| < q(k)\ [LSB]. \tag{1}$$

where $V_{DAC}$ is the voltage output of DAC and $V_{ref}(k)$ is the reference voltage of $k$-th phase [1].

If $N$ is defined as the resolution and $M$ is defined as the number of phases, the following equation is formed [1].


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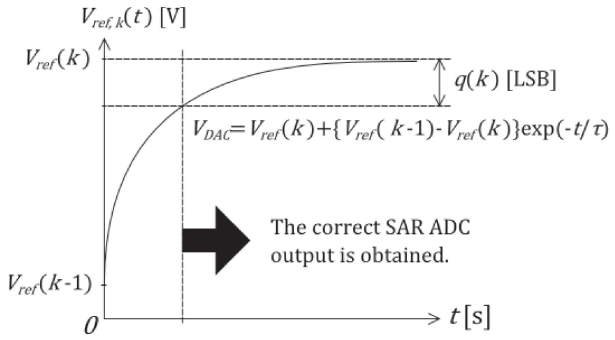


**Fig. 2.** An example of DAC voltage change.

$$\begin{aligned}\sum_{i=1}^{M-1} 2^i q(i) &= 2^M - 2^N \\ &= (2^{M-1} + 2^{M-1}) - 2^N \\ &= 2^{M-1} + (2^{M-2} + 2^{M-2}) - 2^N \\ &\vdots \\ &= 2^{M-1} + 2^{M-2} + \cdots + (2^N + 2^N) - 2^N \\ &= \sum_{i=N}^{M-1} 2^i. \end{aligned} \tag{2}$$

When $q(k) \neq 0$ $\{k = 1, 2, 3, \ldots, s$ $(s \leq N)\}$ and $q(k) = 0$ $(k = s+1, s+2, s+3, \ldots, M-1)$, Eq. (2) is given as

$$\sum_{i=1}^{s} 2^i q(i) = \sum_{i=N}^{M-1} 2^i. \tag{3}$$

$s$ in Eq. (3) indicates the number of phase with redundancy. We define the number of redundancy bits which are added to the resolution as $x$ $(M = N + x)$ and Eq. (3) is expanded as the following equation.

$$2^1 q(1) + 2^2 q(2) + \cdots + 2^s q(s) = 2^N + 2^{N+1} + \cdots + 2^{N+x-1}. \tag{4}$$

In Eq. (4), the right side indicates all amount of redundancy which are distributed as each tolerance range $q(k)$. When we add 1 bit to the redundancy bits,

$$2^1 q(1) + 2^2 q(2) + \cdots + 2^s q(s) = 2^N + 2^{N+1} + \cdots + 2^{N+x-1} + 2^{N+x}. \tag{5}$$

Because all amount of redundancy in Eq. (5) are more $2^{N+x}$ than that in Eq. (4), more redundancy are distributed as tolerance range and tolerance range of Eq. (5) can be wider than that of Eq. (4). As shown Fig. 3, the width of the tolerance range affect the DAC change time which is needed to obtain the correct SAR ADC output, $T_{settling}$. In other words, the tolerance range affect the A/D conversion time.

For example, when the tolerance range gets wide, the DAC change time can get short and the A/D conversion time can get short. However, when all $q(k)$ are already maximum, even though the redundancy bit increases, the conversion time cannot get short because the tolerance range is not spread


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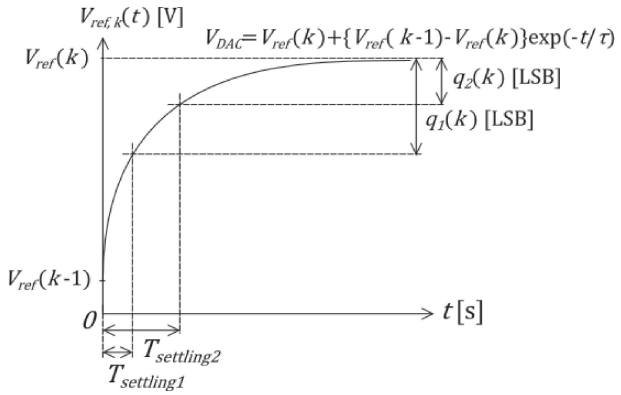


**Fig. 3.** Relationship between $q(k)$ and $T_{settling}$.

any more. Thus, the optimal redundancy bit is determined in the range satisfying the following equation.

$$\sum_{i=1}^{s}[2^i \times Max\{q(i)\}] \geq \sum_{i=N}^{N+x-1} 2^i. \tag{6}$$

## 3 Maximum tolerance range

In this section, we describe the maximum tolerance range.

Eq. (3) is expanded as the following equation.

$$\sum_{i=1}^{k-1} 2^i q(i) + 2^k q(k) + \sum_{i=k+1}^{s} 2^i q(i) = \sum_{i=N}^{M-1} 2^i. \tag{7}$$

Thus, the tolerance range of $k$-th phase $q(k)$ is defined by

$$q(k) = 2^{-k}\left\{\sum_{i=N}^{M-1} 2^i - \sum_{i=1}^{k-1} 2^i q(i) - \sum_{i=k+1}^{s} 2^i q(i)\right\}. \tag{8}$$

For $q(k) \geq 0$, the following equation is formed.

$$\begin{aligned} Max\{q(k)\} &= 2^{-k}\sum_{i=N}^{M-1} 2^i \\ &= 2^{-k}(2^M - 2^N). \end{aligned} \tag{9}$$

From Eq. (9), the smaller $k$ is, the more maximum tolerance range spreads when $N$ and $M$ are defined. However, $q(k)$ is not more than $2^{N-1}$ which is half of resolution $2^N$. Thus, the maximum range varies depending on the condition.

(i). When $k = x - 1$,

$$2^{N-1} - 2^{-(x-1)}(2^M - 2^N) = 2^{N-(x-1)}\{(-3) \times 2^{x-2} + 1\} < 0. \tag{10}$$

Thus, $Max\{q(k)\} = 2^{N-1}$.

(ii). When $k = x$,

$$2^{N-1} - 2^{-x}(2^M - 2^N) = 2^{N-x}\{(-1) \times 2^{x-1} + 1\} \leq 0. \tag{11}$$

Thus, $Max\{q(k)\} = 2^{N-1}$.


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(iii). When $k = x + 1$,

$$2^{N-1} - 2^{-(x+1)}(2^M - 2^N) = 2^{N-(x+1)} > 0. \tag{12}$$

Thus, $Max\{q(k)\} = 2^{N-k}(2^x - 1)$.

From (i), (ii), and (iii),

$$Max\{q(k)\} = \begin{cases} 2^{N-1} & (k = 1, 2, \ldots, x) \\ 2^{N-k}(2^x - 1) & (k = x+1, x+2, \ldots, s) \end{cases}. \tag{13}$$

## 4 Optimal redundancy bit

In this section, we describe the optimal number of redundancy bits to be satisfying Eq. (6).

(I). When $x \leq s - 1 \leq N - 1$,

$$Max\{q(k)\} = \begin{cases} 2^{N-1} & (k = 1, 2, \ldots, x) \\ 2^{N-k}(2^x - 1) & (k = x+1, x+2, \ldots, s) \end{cases}. \tag{14}$$

$$\text{Thus, } \sum_{i=1}^{s}[2^i \times Max\{q(i)\}] - \sum_{i=N}^{N+x-1} 2^i = (s - x)\{2^N(2^x - 1)\} > 0. \tag{15}$$

Consequently, Eq. (6) is satisfied.

(II). When $s \leq x \leq N$,

$$Max\{q(k)\} = 2^{N-1} \quad (k = 1, 2, \ldots, s). \tag{16}$$

$$\text{Thus, } \sum_{i=1}^{s}[2^i \times Max\{q(i)\}] - \sum_{i=N}^{N+x-1} 2^i = \sum_{i=N}^{N+s-1} 2^i - \sum_{i=N}^{N+x-1} 2^i. \tag{17}$$

When $x = s$, Eq. (6) is satisfied and when $x > s$, Eq. (6) is not satisfied.

(III). When $s + 1 \leq N + 1 \leq x$,

$$Max\{q(k)\} = 2^{N-1} \quad (k = 1, 2, \ldots, s). \tag{18}$$

Thus,

$$\sum_{i=1}^{s}[2^i \times Max\{q(i)\}] - \sum_{i=N}^{N+x-1} 2^i = \sum_{i=N}^{N+s-1} 2^i - \sum_{i=N}^{N+x-1} 2^i < 0. \tag{19}$$

Consequently, Eq. (6) is not satisfied.

From (I), (II), and (III), the optimal number of redundancy bits ($x$) satisfying Eq. (6) is in the range from 1 to $s$.

## 5 Example

In this section, we describe some examples. When $N = 4$ [bit], 8 [bit] and 10 [bit], optimal each tolerance ranges and optimal redundancy bits are determined as shown in Table I and II. Other parameters [4] are set as follows.

(a). $V_{dd} = 1.8$ [V], $R_{ON} = 5.0$ [kΩ], $C_{min} = 20$ [fF], $T_{CLK} = 20$ [ps], $T_{comp} = 10$ [ps], $q(k) \neq 0$ $(k = 1, 2, 3, 4, 5)$, and $q(k) = 0$ $(k = 6, 7, \ldots, M)$.

(b). $V_{dd} = 1.8$ [V], $R_{ON} = 5.0$ [kΩ], $C_{min} = 20$ [fF], $T_{CLK} = 2.0$ [ns], $T_{comp} = 1.0$ [ns], $q(k) \neq 0$ $(k = 1, 2)$, and $q(k) = 0$ $(k = 3, 4, \ldots, M)$.


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**Table I.** Example of (a)

| $N$ [bit] | Optimal tolerance ranges [LSB] | | | | | Optimal redundancy bits [bit] | Optimal $M$ [bit] |
|---|---|---|---|---|---|---|---|
| | $q(1)$ | $q(2)$ | $q(3)$ | $q(4)$ | $q(5)$ | | |
| 6 | 16 | 8 | 8 | 2 | 1 | 2 | 8 |

**Table II.** Example of (b)

| $N$ [bit] | Optimal tolerance ranges [LSB] | | Optimal redundancy bits [bit] | Optimal $M$ [bit] |
|---|---|---|---|---|
| | $q(1)$ | $q(2)$ | | |
| 8 | 64 | 32 | 1 | 9 |
| 10 | 192 | 160 | 1 | 11 |

## 6 Conclusion

We proposed a methodology of searching the optimal number of redundancy bits of SAR ADC in order that the A/D conversion time is minimized. In this paper, we proved that there is the optimal redundancy bit in range from 1 to $s$. Therefore, we don't need to examine vast amounts of data and the high-speed SAR ADC can be realized.

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